FRED

- Frequency Deputy Unit

User Manual

Version 002

Innovation with Integrity

NMR

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1 About

1.1 This Manual

This manual enables safe and efficient handling of the device.

This manual is an integral part of the device, and must be kept in close proximity to the device where it is permanently accessible to personnel.

Before starting any work, the personnel must have read the manual thoroughly and understood its contents. Compliance with all specified safety instructions and operating instructions is vital to ensure safe operation.

In addition, local accident prevention regulations and general safety instructions must be observed for the operational area of the device.

Illustrations in this manual are intended to facilitate basic understanding, and may differ from the actual design.

In addition to the user manual, instructions concerning local labor protection laws, operator regulations, and tools and supplies must be available and adhered to.

1.2 Policy Statement

It is the policy of Bruker to improve products as new techniques and components become available. Bruker reserves the right to change specifications at any time.

Every effort has been made to avoid errors in text and figure presentation in this publication. In order to produce useful and appropriate documentation, we welcome your comments on this publication. Support engineers are advised to regularly check with Bruker for updated information.

Bruker is committed to providing customers with inventive, high quality products and services that are environmentally sound.

1.3 Symbols and Conventions

Safety instructions in this manual are marked with symbols. The safety instructions are introduced using indicative words which express the extent of the hazard.

In order to avoid accidents, personal injury or damage to property, always observe safety instructions and proceed with care.

DANGER

This combination of symbol and signal word indicates an immediately hazardous situation which could result in death or serious injury unless avoided.

⚠ WARNING

This combination of symbol and signal word indicates a potentially hazardous situation which could result in death or serious injury unless avoided.

⚠ CAUTION

This combination of symbol and signal word indicates a possibly hazardous situation which could result in minor or slight injury unless avoided.

NOTICE

This combination of symbol and signal word indicates a possibly hazardous situation which could result in damage to property or the environment unless avoided.

This symbol highlights useful tips and recommendations as well as information designed to ensure efficient and smooth operation.

Special Safety Instructions

The following symbols are used in the safety instructions to draw attention to specific danger:

⚠ DANGER

This combination of symbol and signal word indicates dangers posed by electric power. If the safety instructions are not observed, there is a danger of serious or fatal injuries.

2 Introduction

The Frequency Deputy (FRED) unit is used in MRI **AVANCE III** spectrometers to receive frequency and phase information from frequency offset devices, and integrate phase and frequency offset commands into the data flow from Frequency Controllers (FCTRL) to Signal Generation Units (SGU).

2.1 Concept

The FRED unit receives frequency and phase information from frequency offset devices (B0 term of cross-preemphasis from the DPP and the software lock from the RT-client) and integrates phase and frequency offset commands into the data flow of from 1 to 3 FCTRL‘s to 1, 2 or 3 SGU‘s respectively.

The FRED calculates a global frequency and phase offset from the B0 data coming from the DPP, via the LVDS, and from values coming from the RT-Client via PCI. The result is then scaled according to the scaling factors (SCF_1, SCF_2 and SCF_3) for each frequency channel, then the frequency or phase offset values are transferred to the connected SGU(s).

Special MRI applications use the FRED unit to correct the offset of the spectrometer B0 field by switching the frequency offset at the SGU.

Refer to "Design and Function" on page 13 for more information.

Figure 2.1 The Frequency Deputy Unit

2.2 Limitations of Liability

All specifications and instructions in this manual have been compiled taking account of applicable standards and regulations, the current state of technology and the experience and insights we have gained over the years.

The manufacturer accepts no liability for damage due to:

- Failure to observe this manual.
- Improper use.
- Deployment of untrained personnel.
- Unauthorized modifications.
- Technical modifications.
- Use of unauthorized spare parts.

The actual scope of supply may differ from the explanations and depictions in this manual in the case of special designs, take-up of additional ordering options, or as a result of the latest technical modifications.

The undertakings agreed in the supply contract as well as the manufacturer‘s Terms and Conditions, Terms of Delivery, and the legal regulations applicable at the time of conclusion of the contract shall apply.

2.3 Spare Parts

Spare parts may be obtained from authorized dealers or directly from the manufacturer. See "Contact" on page 51 for the address.

2.4 Warranty Terms

The warranty terms are included in the manufacturer‘s Terms and Conditions.

2.5 Customer Service

Our customer service division is available to provide technical information. See for "Contact" on page 51 contact details.

In addition, our employees are always interested in acquiring new information and experience gained from practical applications; such information and experience may help improve our products.

3 Safety

This chapter provides an overview of all the main safety aspects involved in ensuring optimal personnel protection and safe and smooth operation.

Non-compliance with the action guidelines and safety instructions contained in this manual may result in serious hazards. Before starting any work, personnel must read this chapter thoroughly and understand its contents.

3.1 Intended Use

The unit has been designed and constructed solely for the intended use described here.

The FRED units must only be used for the limited purpose of controlling the spectrometer B0 field by switching the frequency and phase offset of the SGU in Bruker AVANCE III spectrometers.

Intended use also includes compliance with all specifications in this manual.

Any use which exceeds or differs from the intended use shall be considered improper use.

No claims of any kind for damage will be entertained if such claims result from improper use.

3.2 General Safety Instructions

The FRED can be damaged by inappropriate usage. In this case the equipment must not be used until it has been checked by service personnel.

The user should re-check the equipment at regular intervals for any damage or wear and is expected to inform the service immediately of any abnormality.

Do not operate the equipment in the presence of flammable gases or fumes.

⚠ WARNING

Material or personnel damage from worn or damaged parts.

Damaged or worn parts may result if one or the following circumstances occurs:

- The power cord, power plug or power supply are cracked, brittle or damaged.
- Signs of excessive heat appear.
- There is evidence or suspicion that a liquid has intruded into any enclosure.
- The power cord or the power supply have been in contact with any liquid.
- The FRED has been dropped or damaged in any way.
- The equipment does not work correctly

In the unlikely event one of the above occurs:

- Stop using the equipment.
- Disconnect the power supply.
- Inform service and ask for instructions.

Only trained service personnel are allowed to mount, retrofit, repair, adjust and dismantle the FRED unit. Do not try to service the equipment unless you are specifically asked to do so and are given instructions by the service staff. In case of questions or problems, please contact your nearest Bruker office or representative.

Before maintenance, repair or shipment, the FRED unit must be completely disconnected from the power supply and dismounted from its rack.

4 Technical Data

4.1 General Information

Specification	Value	Unit
Weight	2.5	kg
Length	46.2	cm
Width	29.0	cm
Height	4.3	cm

Table 4.1 Technical Data: General Information

4.2 Utility Requirements

Ingress Protection Class:	IP 20, secured against touching dangerous points inside, not secured against ingress of water.
Over-voltage Protection Category:	CAT II, according to EN61010–1or IEC60664–1 safe against over-voltage by switching, not safe against lightning. Surge immunity of PSU is level 3, according to IEC61000–4–5.
IEC Protection Class:	Class I, according the IEC 61140, connected to mains by phase, neutral and protective earth.
Input Voltage Range:	208 V to 230 V.
Frequency:	50/60 Hz.
Input Power:	30 VA.
Fuse On Mains Input:	250 VAC 2 A.
Connection:	Socket outlet with phase, neutral and protective–earth according to VDE 0620–1.

Table 4.2 Technical Data: Utility Requirements

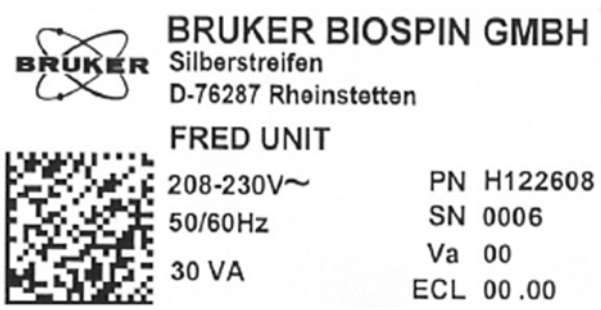
4.3 Operating Conditions

4.3.1 Operating Environment

Permissible ambient temperature:	5°C to 40°C.
Permissible altitude:	Up to 2000 meters above sea level.
Relative humidity:	Maximum of 80% for temperatures up to 31°C, linearly decreasing to 50% at a temperature of 40°C.
Permissible storage temperature:	5°C to 40°C.
Pollution degree:	The acceptable pollution degree is 2. According to EN 61010-1 or IEC 60664-1. Any pollution is non-conductive, except condensed moisture.

Table 4.3 Operating Environment

4.4 Rating Plates



The rating plate is located at the power input and includes the following information:

- Manufacturer
- Type
- Voltage
- Frequency
- Apparent power consumption, maximum
- PN: Part Number
- SN: Serial Number
- Va: Variant
- ECL: Engineering Change Level

5 Design and Function

5.1 Product and Manufacturer

Product:	FRED Unit P/N H122608 FRED Board P/N H12607 Power Supply P/N 88873 LVDS Cable 1m P/N 86868 PCI Express Cable P/N 1805036		
Manufacturer:	Bruker BioSpin GmbH Silberstreifen 4 76287 Rheinstetten Germany		
Conformity:	EN 61010-1	2010-06	Safety requirements for electrical equipment for measurement, control, and laboratory use - Part 1: General requirements

5.2 General Description

The Frequency Deputy (FRED) is a device that receives frequency and phase information from frequency offset devices (B0 term of cross-preemphasis from the DPP and software lock from RT-client) and integrates phase and frequency offset commands into the data flow of 1 to 3 FCTRL‘s to 1, 2 or 3 SGU‘s respectively.

The FRED board is integrated in a 1HE 19“ chassis which includes the power supply. On the front of the chassis are the connector pairs for the three FCTRL to SGU LVDS channels (IN/OUT), the LVDS IN/OUT from the DPP to the gradient amplifier, and the PCIe port to the IPSO unit. The unit can be turned on using the power switch on the front of the chassis. The power state is indicated by an indicator light. An indicator light also indicates that the PCI link is functioning.

The FRED unit is a part of the IPSO AQS system and is installed in the same AQS rack.

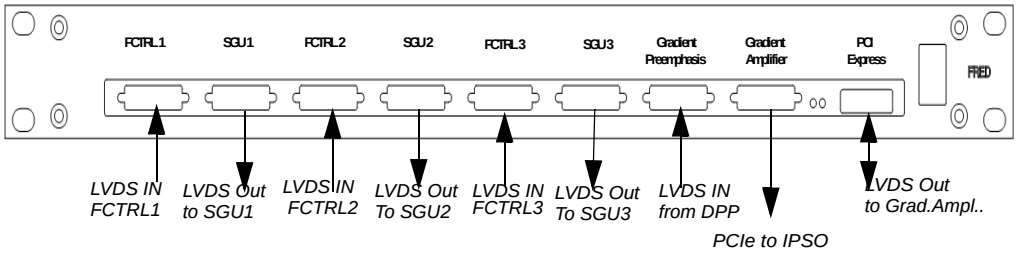


Figure 5.1 Front View of the External Connections

The FRED calculates a global frequency and phase offset from B0 data, coming from the DPP via the LVDS, and from values coming from the RT-Client via the PCI bus. The result is then scaled according to the scaling factors (SCF_1, SCF_2 and SCF_3) for each frequency channel prior to transferring frequency or phase offset values to the connected SGU(s). A scaling factor with a value 0 disables the corresponding channel for B0 offset correction. Frequency and phase offset values are only embedded in the FCTRL to SGU data path if a new offset values is activated. The LVDS inputs are all checked for parity error. In case of a parity error an interrupt to the RT-client is generated.

All register and RAM buffers must be initialized before the start of the experiment.

Special MRI applications use the FRED unit to correct the offset of spectrometer B0 field by switching the frequency offset at the SGU.

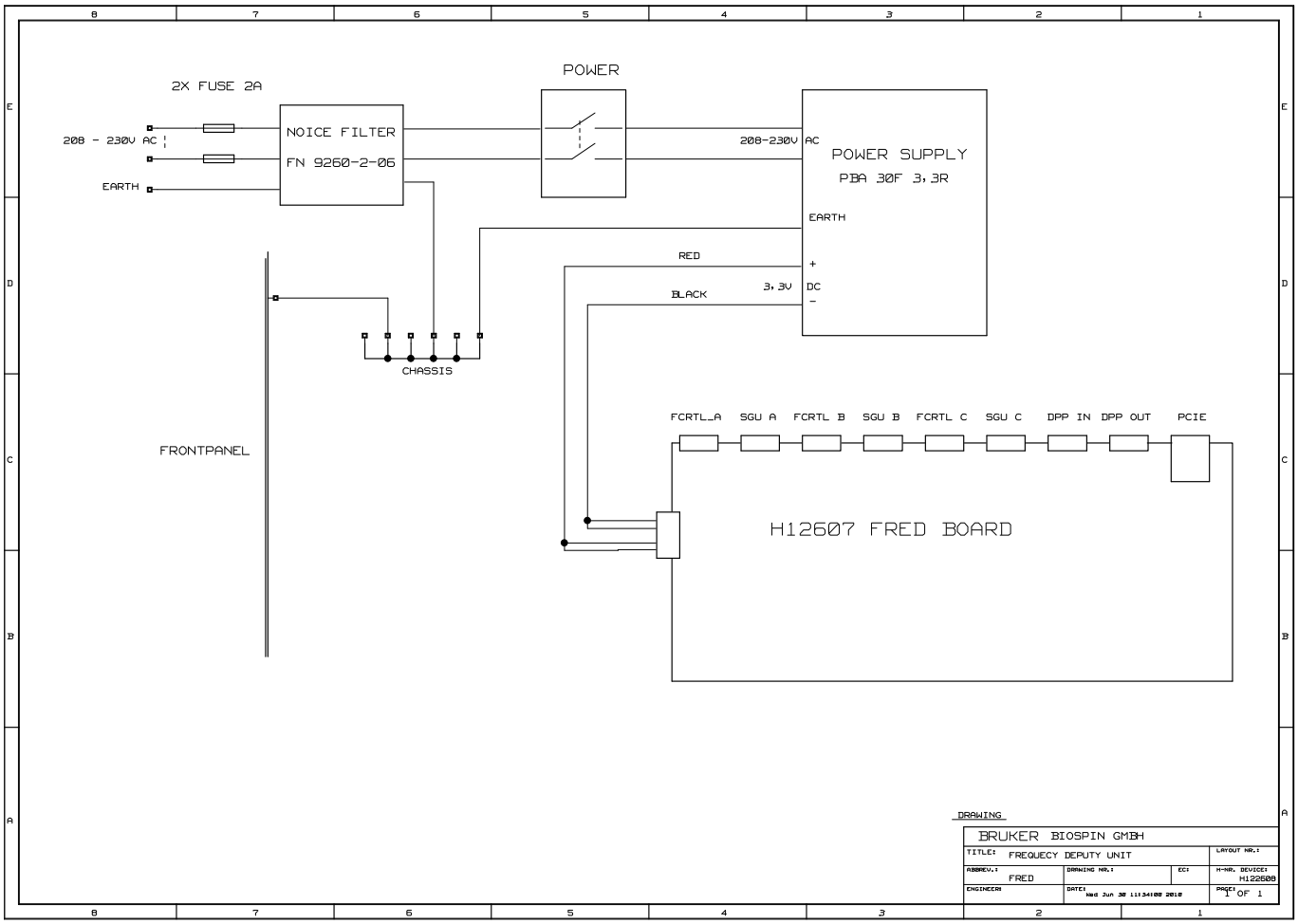


Figure 5.2 The FRED Unit Wiring

5.3 Features

- A 48-bit LVDS interface to connect the FCTRL, DPP and SGU.
- PCI express generation 1 interface to connect the RT-client (IPSO host) via cable.
- Simultaneous frequency (B0) and phase offset control of up to 3 channels at 80 MHz speed.
- Pulse program controlled synchronous update of the frequency and phase offsets from DPP.
- Asynchronous frequency and phase offset switching via PCIe bus (RT-Client).
- Programmable delay register to adjust the update of the B0 offset to the gradient switching time.
- JTAG test and programming interface.

5.4 Functional Description

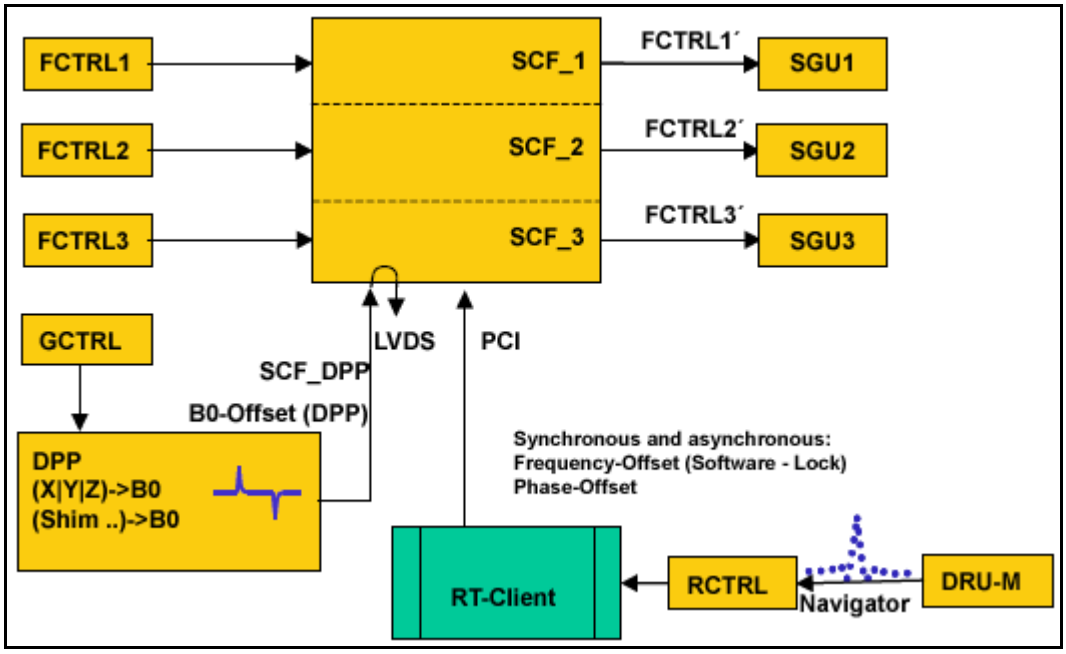


Figure 5.3 Block Diagram for the FRED

5.4.1 The PCI Interface

The PCI interface for the FRED is implemented by the PCIe to PCI bridge (PEX 8112 controller) and the PCI to local bus controller (PCI9030 PLX Technologies) to translate the PCI bus to the local bus.

The PCI 9030 controller translates external PCI accesses to internal local bus accesses and vice versa.

The local bus for the controller is connected to the FPGA to access the various registers inside the chip. To communicate with the FPGA over the PCIe Interface, the 80 MHz clock signal must be provided at the LVDS Input „Gradient Pre-emphasis“ from the DPP. The PCI controller “PCI 9030” from “PLX Technology” provides the interface between the PCI bus and the internal local bus to the FPGA. The controller configures itself after a reset or power-up by reading the content of a dedicated serial EEPROM. Some values of the configuration registers are read directly out of the PROM and some are generated from the PROM content.

The address map for this EEPROM and its contents are listed below.

The EEPROM of the PCI 9030 controller is programmed using the CASCON JTAG software.

5.4.2 PCI Software Interface

The PCI address map of the internal FRED addresses at the local bus is built by the BIOS after power-up using the contents in the configuration registers “Base address 0...5”. The results are the PCI base addresses of the local bus chip selects, which are written by the BIOS in the same configuration registers.

EEPROM Offset	Register Offset Configuration Space Address	Register Description	Affected Bits	Register Values	Value Description
00 h	02	Device ID	PCIDR[31:16]	9030 h	
02 h	00 h	Vendor ID	PCIIDR [15:0]	10B5 h	
04 h	06 h	PCI Status	PCISR [15:0]	0290 h	
06 h	04 h	PCI Command		0000 h	Reserved
08 h	0A h	Class Code	PCICCR [15:8]	0680 h	
0A h	08 h	Class Code / Revision	PCICCR [7:0/ PCIREV [7:0]	000A h	
0C h	2E h	Subsystem ID	PCISID [15:0]	0300 h	
0E h	2C h	Subsystem Vendor ID	PCIVSID [15:0]	0000 h	
10 h	36 h	MSB New Capability Pointer		0000 h	Reserved
12 h	34 h	LSB New Capability Pointer	CAP_PTR[7:0]	0040 h	
14 h	3E h	Maximum Latency & minimum Grant can‘t be loaded		0000 h	Reserved
16 h	3C h	Interrupt Pin	PCIIPR [7:0]/ PCIILR [7:0]	01FF h	
18 h	42 h	MSW of Power Management Capabilities	PMC[15:11, 5, 3:0]	4801 h	

1A h	40 h	LSW of Power Management Next Capability pointer	PMNEXT [7:0] / PMCCAPID[7:0]	4801 h	
1C h	46 h	MSW of Power Management data		0000 h	Reserved
1E h	44 h	LSW of Power Management Control / Status	PMCSR [14:8]/ PCIILR [7:0]	0000 h	
20 h	4A h	MSW of Hot Swap/Control		0000 h	Reserved
22 h	48 h	LSW of Hot Swap Next Capability Pointer / Control	HS_NEXT[7:0]/ HS_CNTL[7:0]	4C06	
24 h	4E h	PCI Vital Product Data Address		0000 h	Reserved
26 h	4C h	PCI Vital Product Data Next Capability Pointer/Control	PVPD_NEXT[7:0] PVPDCNTL[7:0]	0003 h	
Content of Local Register					
28 h	02 h	MSW of Local Address Space 0 Range	LAS0RR[31:16]	0FFF h	2 KB Local Address Space non-prefetch FPGA Dev.
2A h	00	LSW of Local Address Space 0 Range	LAS0RR[15:0]	F000 h	
2C h	06 h	MSW of Local Address Space 1 Range	LAS1RR[31:16]	0FF0 h	1 MB Local Address Space unused default value
2E h	04 h	LSW of Local Address Space 1 Range	LAS1RR[15:0]	0000 h	
30 h	0A h	MSW of Local Address Space 2 Range	LAS1RR[31:16]	0FF0 h	1 MB Local Address Space unused default value
32 h	08 h	LSW of Local Address Space 2 Range	LAS1RR[15:0]	0000 h	
34 h	0E h	MSW of Local Address Space 3 Range	LAS1RR[31:16]	0FF0 h	64 KB Local Address Space non-prefetch BIS FLASH
36 h	0C h	LSW of Local Address Space 3 Range	LAS1RR[15:0]	0000 h	
38 h	12 h	MSW of Expansion ROM Range	EROMRR[31:16]	0000 h	Disable
3A h	10 h	LSW of Expansion ROM Range	EROMRR[15:0]	0000 h	
3C h	16 h	MSW of Local Address Space 0 Local Base Address (Remap)	LAS0BA[31:16]	0001 h	enable CE 0
3E h	14 h	LSW of Local Address Space 0 Local Base Address (Remap)	LAS0BA[15:0]	0001 h	

40 h	1A h	MSW of Local Address Space 1 Local Base Address (Remap)	LAS1BA[31:16]	0000 h	enable CE 1
42 h	18 h	LSW of Local Address Space 1 Local Base Address (Remap)	LAS1BA[15:0]	0000 h	
44 h	1E h	MSW of Local Address Space 2 Local Base Address (Remap)	LAS2BA[31:16]	0000 h	enable CE 2
46 h	1C h	LSW of Local Address Space 2 Local Base Address (Remap)	LAS2BA[15:0]	0000 h	
48 h	22 h	MSW of Local Address Space 3 Local Base Address (Remap)	LAS3BA[31:16]	0000 h	Enable CE 3
4A h	20 h	LSW of Local Address Space 3 Local Base Address (Remap)	LAS3BA[15:0]	0001 h	
4C h	26 h	MSW of Expansion ROM Local Base Address (Remap)	EROMBA[31:16]	0001 h	Disable
4E h	24 h	LSW of Expansion ROM Local Base Address (Remap) EROMBA[15:0] 0000 h	EROMBA[15:0]	0000 h	
50 h	2A h	MSW of Local Address Space 0 Bus Region Descriptor	LAS0BRD[31:16]	0081 h	Enable 32Bit Local Bus Width Not ready NRAD 3 NWAD 3 NXDA 1
52 h	28 h	LSW of Local Address Space 0 Bus Region Descriptor	LAS0BRD[15:0]	A0C0 h	
54 h	2E h	MSW of Local Address Space 1 Bus Region Descriptor	LAS1BRD[31:16]	0000 h	Default value 8 Bit Local Bus Width, NXDA, NWAD 0,
56 h	2C h	LSW of Local Address Space 1 Bus Region Descriptor	LAS1BRD[15:0]	0000 h	

58 h	32 h	MSW of Local Address Space 2 Bus Region Descriptor	LAS2BRD[31:16]	0000 h	default value 8 Bit Local Bus Width, NXDA,0 NWAD 0,
5A h	30 h	LSW of Local Address Space 2 Bus Region Descriptor	LAS2BRD[15:0]	0000h	
5C h	36 h	MSW of Local Address Space 3 Bus Region Descriptor	LAS2BRD[31:16]	0014 h	8 Bit Local Bus Width, no ready NRAD 8 NRDD 0, NWAD 8, NXDA 1
5E h	34 h	LSW of Local Address Space 3 Bus Region Descriptor	LAS2BRD[15:0]	2200 h	
60 h	3A h	MSW of Expansion Rom Region Descriptor	EROMBRD[31:16]	0000 h	
62 h	38 h	LSW of Expansion Rom Region Descriptor	EROMBRD[15:0]	0000 h	
64 h	3E h	MSW of Chip Select 0 Base Address	CS0BASE[31:16]	0000 h	CS0 enabled ADD=0XXXh Range 2KB FPGA Device Codes
66 h	3C h	LSW of Chip Select 0 Base Address	CS0BASE[15:0]	0801 h	
68 h	42 h	MSW of Chip Select 1 Base Address	CS1BASE[31:16]	0000 h	CS1 disabled
6A h	40 h	LSW of Chip Select 1 Base Address	CS1BASE[15:0]	0000 h	
6C h	46 h	MSW of Chip Select 2 Base Address	CS2BASE[31:16]	0000 h	CS2 disabled
6E h	44 h	LSW of Chip Select 2 Base Address	CS2BASE[15:0]	0000 h	
70 h	4A h	MSW of Chip Select 3 Base Address	CS3BASE[31:16]	0001 h	CS3 enabled ADD=1XXXXh Range 64KB BIS FLASH
72 h	48 h	LSW of Chip Select 3 Base Address	CS3BASE[15:0]	8001 h	
74 h	4E h	Serial EEOROM Write–Protected Address Boundary	PROT_AREA[7:0]	0030 h	Default
76 h	4C h	LSW of Interrupt Control/ Status	INTCSR[15:0]	0041 h	Local Int.1 low level

78 h	52 h	MSW of PCI Target Response, Serial EEPROM, Initialization Control	CNTRL [31:15]	1078 h	
7A h	50 h	LSW of PCI Target Response, Serial EEPROM, Initialization Control	CNTRL [15:0]	0000 h	
7C h	56 h	MSW of General Purpose I/O Control	GPIOC [31:15]	0049 h	
7E h	54 h	LSW of General Purpose I/O Control	GPIOC [15:0]	6E30 h	CS2 & CS3 enabled GPIO 4 used as output
80 h	72 h	MSW of Hidden 1 Power Management Data Select	PMDATA[7:0]	0000 h	
82 h	70 h	LSW of Hidden 1 Power Management Data Select	PMDATA[7:0	0000 h	
84 h	76 h	84 h 76 h MSW of Hidden 2 Power Management Data Scale Reserved	Reserved		
86 h	74 h	LSW of Hidden 2 Power Management Data Scale	PMCSR[14:13] hidden, PMCSR[7:0] used	0000 h	

Table 5.1 Contents of the PCI9030 Serial Configuration EEPROM

5.4.3 BIS Flash Prom at the Local Bus

This Flash Prom is used to store the BIS information of the unit and is configured via the IPSO Service WEB Tool. The flash prom, connected to PCI bus over the PLX controller, is accessible in the local CS3 address space.

Bus width: 2 byte, data bit 7...0 connected, data bit 15...8 unused;

Corresponding in a double used address range:

Bus cycle length circa 120 nsec for write and 240 nsec for read cycles.

Example BIS of a FRED

```
$Bis, 1, 20100803, 65536, LVDSMANIP, 1#
$Prd, H122608, 02, 00,, B-NMR-DE, 20100823#
$Nam, FRED Frequency Deputy#
$BasicBoard, 1.0, H12607, 02, 00, FRED Board#
$EndBis, CS1, CS2#
```

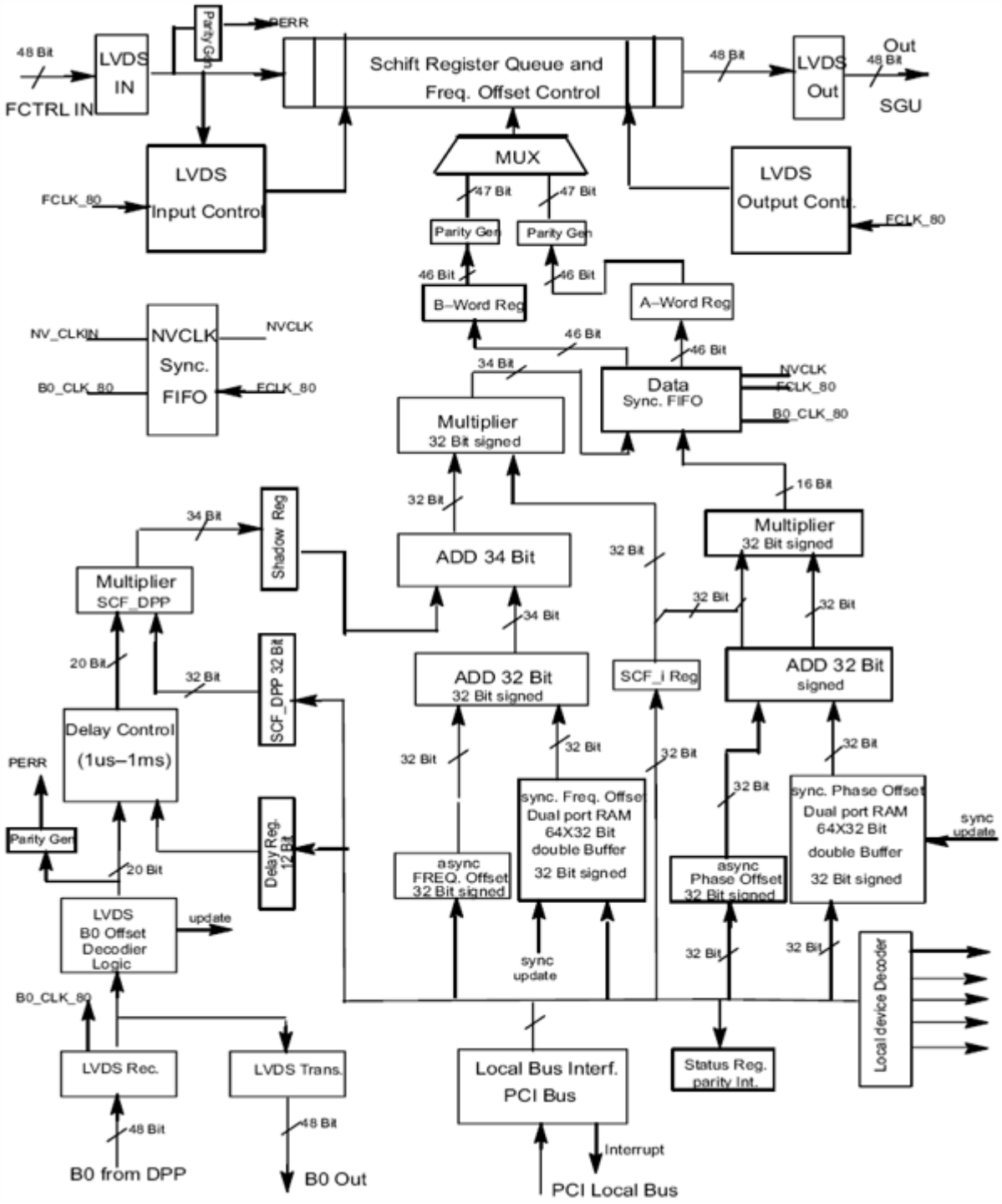


Figure 5.4 Logical Block Diagram of One Channel

Acronyms	Local Address	Function	Mode R/W	Bit
SFRAM	X0000000- X00000FF	Frequency offset RAM buffer for synchronous update.	R/W	31- 0
SPHRAM	X0000100- X00001FF	Phase offset RAM buffer for synchronous update.	R/W	31- 0
AFRREG	X0000200	Asynchronous frequency register.	R/W	31- 0
APHREG	X0000204	Asynchronous phase register.	R/W	31- 0
SCF_A	X0000208	Scale factor for channel A.	R/W	31- 0
SCF_B	X000020C	Scale factor for channel B.	R/W	31- 0
SCF_C	X0000210	Scale factor for channel C.	R/W	31- 0
SCF_DPP	X0000214	Scale factor for DPP B0 channel.	R/W	31- 0
B0_DEL	X00000218	Value of delayed B0 input data.	R	19 - 0
DEL_REG	X0000021C	Register to delay the B0 Input (delay = register value X NV clock cycles).	R/W	9 - 0
SELRAM	X00000220	Signal to select the synchron frequency/phase offset list (RAM buffer select) for write access. Bit0=0 buffer 1 selected Bit0=1 buffer 2 is selected Read value via DEL_REG	W	Bit 0
SELCREG	X00000224	Synchronous frequency/phase RAM address counter. Read value via DEL_REG	W	5-0
FRPH_UPD	X00000228	Update synchronous frequency/phase value via PCI access.	W	X
FREQOFF_A	X00000300	Read frequency offset of channel A.	R	31-0
FREQOFF_B	X00000304	Read frequency offset of channel B.	R	31-0
FREQOFF_C	X00000308	Read frequency offset of channel C.	R	31-0
PHOFF_A	X0000030C	Read phase offset of channel A.	R	31-0
PHOFF_B	X00000310	Read phase offset of channel B.	R	31-0
PHOFF_C	X00000314	Read phase offset of channel C.	R	31-0
INTRPT	X00000318	Interrupt and status register & FPGA version register.	R/W	3 - 0
CLR_ADDC	X0000031C	Clear RAM address counter.	W	0
RESET	X00000320	Reset device.	W	0

Table 5.2 Control Registers and Device Code Commands on FRED

5.5 Register and Device Code Description

Acronyms	Local Address	Function	Mode R/ W	Bit
SFRAM	X0000000-X00000FF	Frequency offset RAM buffer for synchronous update.	R/W	31-0

Table 5.3 Synchronous Frequency Offset RAM

The RT-client can access the Synchronous Frequency Offset RAM (size = 64 x 32 bit) via the PCI bus. The RAM is realized as a dual port memory with two RAM arrays each 64 x 32 bit. In this way the RT-client can preload a new list of offset values while the active list in the second RAM array is in use. The activation of the list is controlled by the RT-client with the SELRAM command. The usable (length) size of the RAM can be defined by the RT-client using the SELCREG (select counter register) command. After a synchronous update command from the DPP, the counter of the frequency RAM buffer is incremented automatically for the next value in the activated list. If the counter reaches the programmed end of the list it is reloaded and points to the first entry again.

The offset value is activated synchronously with the pulse program using a special LVDS UPDATE command from the DPP, and becomes valid with the next NV-clock signal from the DPP. The time between the UPDATE and the NV_CLOCK should be 100 ns (62.5 ns).

The synchronous frequency offset is a 32 bit signed integer value with a resolution of 0.0047 Hz

Acronyms	Local Address	Function	Mode R/ W	Bit
SPHRAM	X0000100-X00001FF	Phase offset RAM buffer for synchronous update.	R/W	31-0

Table 5.4 Synchronous Phase Offset RAM

The functionality of the Synchronous Phase Offset RAM buffer is the same as the frequency offset buffer. The RT-client can access this RAM (size = 64 x 32 bit) via the PCI Bus. The RAM is realized as a dual port memory with two RAM arrays each 64 x 32 bits. In this way the RT-client can preload a new list of offset values while the active list in the second RAM array is in use. The activation of the list is controlled by the RT-client with the SELRAM command.

The offset value is activated synchronously with the pulse program using a special UPDATE command from the DPP and becomes valid with the next NV-clock from the DPP. The time between the UPDATE and the NV_CLOCK should at least be 100 ns (62.5 ns).

The synchronous phase offset is a 32 bit signed integer fixed point (16.16) value, where 1.0 corresponds to a phase value of 2P.

Acronyms	Local Address	Function	Mode R/W	Bit
AFRREG	X0000200	Asynchronous frequency offset register.	R/W	31-0

Table 5.5 Asynchronous Frequency Offset Register

The Asynchronous Frequency Offset Register is a 32 bit (signed integer value) register which can be accessed over the PCI bus. This offset value always becomes active and is sent to the connected SGU's with the next NV_clock from the DPP. The time delay from the NV_clock to the data send over the LVDS is 125 ns.

Acronyms	Local Address	Function	Mode R/W	Bit
APHREG	X0000204	Asynchronous phase register.	R/W	31-0

Table 5.6 Asynchronous Phase Offset Register

The Asynchronous Phase Offset Register is a 32-bit (signed integer fixed point value 16.16, whereby 1.0 equals to 2PI) register which can be accessed over the PCI bus. The asynchronous phase offset value always becomes active and is sent to the connected SGU's on the next NV_clock from the DPP. The time from the NV_clock to the data send over the LVDS is 125 ns.

Acronyms	Local Address	Function	Mode R/W	Bit
SCF_A	X0000208	Scale factor for channel A.	R/W	31-0
SCF_B	X000020C	Scale factor for channel B.	R/W	31-0
SCF_C	X0000210	Scale factor for channel C.	R/W	31-0

Table 5.7 Scale Factor Register for Channel A, B, C

The Scale Factor Register is a 32-bit (signed integer value) representing a range from 0..1. The offset values (synchronous and asynchronous) of each channel are summed together and then multiplied with the scale factor. There are three scale factor registers (SCF_A, SCF_B, SCF_C) to adjust the frequency and phase offset of each channel. A scale factor with a value of 0 disables the corresponding channel, meaning that an incoming B0 offset or an synchronous/asynchronous offset value is not transferred to the connected SGU.

Acronyms	Local Address	Function	Mode R/W	Bit
SCF_DPP	X0000214	Scale factor for DPP B0 channel.	R/W	31-0

Table 5.8 Scale Factor Register for the BO Offset

The B0 offset values coming from the DPP has a resolution of 20 bits. The scale factor SCF_DPP is an unsigned fixed point value with 32 bits. The bits 0-19 are fractional and the bits 20-31 are integer values. In order to adapt the 34-bit frequency range of the SGU, the bits 20-31 of the scale factor are used to shift the 20-bit B0 value in an appropriate manner.

Acronyms	Local Address	Function	Mode R/W	Bit
DEL_REG	X0000021C	Register to delay the B0 input (delay = register value X NV clock cycles).	R/W	9 - 0

Bits	31..25	24	23, 22	21..16	15..10	9..0
Fields	Unused	SELRAM Bit	Unused	RAM Address size counter.	Unused	Delay value

Table 5.9 Duration Register to Delay the Incoming B0 Value

The B0 offset values coming from the DPP device needs to be delayed in order to synchronize the activation of the frequency offset with the gradient and shim channels. The Duration Register is used to delay the incoming B0 value from the DPP in steps (resolution) of the NV clock. In case of an 1µs NV_Clock period the delay is programmable from 1µs to 1024µs. The register provides additional bits written by other device codes to read back for test purposes, see table above.

Acronyms	Local Address	Function	Mode R/W	Bit
B0_DEL	X00000218	Value of delayed B0 input data.	R	19 - 0

Table 5.10 Device Code to Read the Delayed B0 Value

This is a read only register for debugging purposes. The register provides the delayed B0 data from the DPP input, for the output of the duration logic inside the FPGA.

Acronyms	Local Address	Function	Mode R/W	Bit
SELRAM	X00000220	Signal to select the synchronous frequency/ phase offset list (RAM buffer select) for write access. Bit0=0 Buffer 1 can be written, Buffer2 is active Bit0=1 Buffer 2 can be written, Buffer1 is active Read value via DEL_REG.	W	Bit 0

Table 5.11 Select Frequency/Phase RAM List for Synchronous Update

This device code is used to activate the preloaded RAM list to update the synchronous frequency and phase offset. A new frequency/phase value is transferred only if the synchronous UPDATE command (LVDS) from the DPP, or the FRPH_UP device code via PCI Bus, is detected. The RAM is organized as a dual port buffer including two lists. While one list is always active the other can be written by the RT-client over the PCI bus. The RT-client should load the list before the start of the experiment.

Acronyms	Local Address	Function	Mode R/W	Bit
SECREG	X00000224	Defines the size of the synchronous frequency/phase RAM buffer.	w	5 - 0

Table 5.12 Frequency/Phase RAM Buffer Size

This register is used to configure the size of the synchronous frequency/phase offset RAM buffer (e.g. a value of 0 equal a list of 1 frequency/phase offset value, a value of 3 equals a list of 4 entries).

The size is adjustable from 1 to 64 words (HEX value 0-4F). After power-up or reset the register is set to zero. For details see the SFRAM device code description. The value is readable via the DEL_REG register.

Acronyms	Local Address	Function	Mode R/W	Bit
FRPH_UPD	X00000228	Update synchronous frequency/ phase value via PCI access.	w	X

Table 5.13 Frequency/Phase Update Command via PCIe

This device code is used to activate a frequency/phase value stored in the synchronous offset RAM buffer via an access from the PCI bus. This mode of operation is only used for initialization or test purposes. The device code simulates the function of the synchronous update command normally sent by the DPP pulse program via the LVDS channel.

Acronyms	Local Address	Function	Mode R/W	Bit
FREQOFF_A	X00000300	Read frequency offset of channel A.	R	31-0
FREQOFF_B	X00000304	Read frequency offset of channel B.	R	31-0
FREQOFF_C	X00000308	Read frequency offset of channel C.	R	31-0

Table 5.14 Read Calculated Frequency Offset of Each Channel

These registers are read only and provide the calculated frequency offset for the channel A, B, and C for test purposes.

The B0 offset values coming from the DPP are multiplied with SCF_DPP and then added to the sum of the valid synchronous and asynchronous frequency offset values from the RT-client. This result is multiplied with the corresponding scaling factor SCF_i (value range 0..1) for each frequency channel.

Foffset,i = SCF_i*(B0_dpp*SCF_dpp +Foffset_sync+Foffset_async)

Equation 5.1: Formula to Compute the Frequency Offset.

Acronyms	Local Address	Function	Mode R/W	Bit
PHOFF_A	X0000030C	read Phase Offset of channel A.	R	31-0
PHOFF_B	X00000310	read Phase Offset of channel B.	R	31-0
PHOFF_C	X00000314	read Phase Offset of channel C.	R	31-0

Table 5.15 Read Calculated Phase Offset of Each Channel

These registers are read only and provide the calculated phase offset for the channel A, B, and C for test purposes.

The valid synchronous and asynchronous phase offset values from the RT-client are summed up and then multiplied with the corresponding scaling factor SCF_i (value range 0..1) for each channel. Only the lower bits 15..0 are valid, the bits 31..17 are set to zero. The 360 degree module of the result value is then transferred to the phase offset register of the connected SGU's.

PHoffset,i = SCF_i*(Phoffset_sync+Phoffset_async)

Equation 5.2: Formula to Compute the Phase Offset.

Acronyms	Local Address	Function	Mode R/W	Bit
INTRPT	X00000318	Interrupt and status register & FPGA version register.	R/W	3 - 0
Bits	**31..24**	**23..16**	**7..4**	**3..0**
Fields	Board Revision. (read only)	FPGA Version (read only).	PERR Status	Interrupt Enable Bits (R/W)

Table 5.16 Interrupt Status Register

Each bit (0..3) is used to enable (set to 1) or disable/clear (set to 0) the corresponding bit 4..7 as the interrupt source. An initiated interrupt will stay active on the PCI bus until the corresponding register is cleared (set to 0) by the PCI bus master in an appropriate interrupt service routine.

After a reset or power-up the bits are zero and the interrupts are cleared and disabled.

The interrupt/status bit 7..4 indicates that a parity error has occurred on the receiving channel.

Bit 4 = 1 represent a parity error on input channel A.

Bit 5 = 1 represent a parity error on input channel B.

Bit 6 = 1 represent a parity error on input channel C.

Bit 7 = 1 represent a parity error on input channel B0.

Bit 23:16 represent the actual FPGA program version number default = 00.

Bit 31:24 board revision number default = 00.

Acronyms	Local Address	Function	Mode R/W	Bit
CLR_ADDC	X0000031C	Clear RAM address counter.	W	0

Table 5.17 Device Code Clear RAM Address Counter

The device code clears (set to 0) the address counter which points to the active list of the synchron phase and frequency RAM.

Acronyms	Local Address	Function	Mode R/W	Bit
RESET	X00000320	Reset Device.	W	0

Table 5.18 Reset Device Code

The device code initialize all the internal register of the FPGA. The SCF_i, the asynchronous frequency offset register, the delay register and the interrupt status register are set to zero.

The delay register is set to 0. The address and size of the counter which controls the synchronous offset RAM is set to 0. This initialization is also executed during the power-on sequence.

5.6 LVDS Word Structure

Bits	47	46	45	44	43	42	41	..	32	31	..	16	15	..	0
Field	PAR	SYN	WID	PLS	PA	A	REG9..0			PHASE15..0			SHAPE15..0		
Number	1	1	1	3			10			16			16		

Table 5.19 Word A of LVDS Interface FCTRL to SGU

Bits	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	..	0
Field	PAR	SYN	WID	NCO_SEL(2..0)			REG_VAL (L1..0)		F_VAL(2..0)			PH_VAL(1..0)		SH_VAL	F_DATA (33..0)		
Number	1	1	1	3			2		3			2		1	34		

Table 5.20 Word B of LVDS Interface FCTRL to SGU

Field	Value	Description
F_DATA 33...0		34 bit frequency information.
SHAPE 15...0		16 bit amplitude information.
PHASE 15...0		16 bit phase information.
REG 9...0		10 bit register data.
PLS, PA, A		3 bit gate information.
SH_VAL		1 valid bit of amplitude information.
PH_VAL 1:0		2 valid bit of phase information.
F_VAL 2:0		3 valid bit of frequency.

Table 5.21 Bit Fields of the F-Controller Output Word

REG_VAL 1...0		2 valid bit of register data.
NCO_SEL 2...0		3 select bits.
WORD_ID(WID)		Bit 46 in each word.
	0	Word A.
	1	Word B.
SYNCHRO		Reflects the current state of the 20−MHz reference clock at transmitter.
PARITY		The even parity bit, created from bit 0 to 45.

Table 5.21 Bit Fields of the F-Controller Output Word

The FRED always transfers a frame A/B word from the connected IPSO FCTRL to the corresponding SGU. A new calculated frequency and phase offset value is embedded in the FCTRL LVDS data stream by the FRED if a time window of 25 ns exists. The F_VAL(2..0) field in word B is used by the FRED logic to address the new frequency and phase offset register at the SGU unit (Global Frequency and Phase Address = 0 x 5).

Bits	47	46..37	36..17..	16..5	4..3	2	1	0
Field	Parity	ADD 9..0	Data 19..0	GND	RES	LAST	BSTR	NGO
Number	1	10	20	12	2	1	1	1

Table 5.22 LVDS Word DPP to FRED

Field	Bit	Description
Parity	47	Even parity of the LVDS word created from bit 0 to 46.
ADD	46..37	10 Bit address of gradient data word.
DATA	20	20 bit gradient data.
GND	12	Unused connected to GND.
RESERV	2	2 reserve bIts.
LAST	1	Indicates the last frame of a gradient data block (active low).
BSTR	1	Indicates the validity of the gradient address and data lines (active low).
NGO	1	Indicates that the preloadet gradient data should be activated.

Table 5.23 Description of the LVDS Gradient Word from the DPP or GCTRL

The LVDS interface operates at 80 MHz. Each NGO signal is followed by a new gradient packet which must be loaded in the gradient amplifier and activated with the next NGO. For a detailed description refer to the IPSO 48 bit LVDS interface manual.

Name	Gradient Address	Gradient Data	Meaning
X Gradient	0x000	Amplitude Value	X gradient.
Y Gradient	0x001		Y gradient.
Z Gradient	0x002		Z gradient.
B0 Gradient	0x003		B0 gradient.
Control Word	0x03f	0x10	Count down X, Y, Z, B0 down.
		0x20	
		0x01	Blank of X gradient.
		0x02	Blank of Y gradient.
		0x04	Blank of Z gradient
		0x08	Blank of B0 gradient
		0x0F	Blank of all gradient.
		0x1000	Synchronous update command of the B0 offset at FRED.

Table 5.24 Gradient address and data Layout

The FRED decodes two addresses of the LVDS word send by the DPP. The address 0x003 transfers the B0 gradient value which is used by the FRED to calculate the frequency offset. The control word address 0x03F with the data pattern 0x1000 is the synchronous update command to activate and increment the predefined frequency/phase list on the FRED.

5.7 The FRED Board H12607

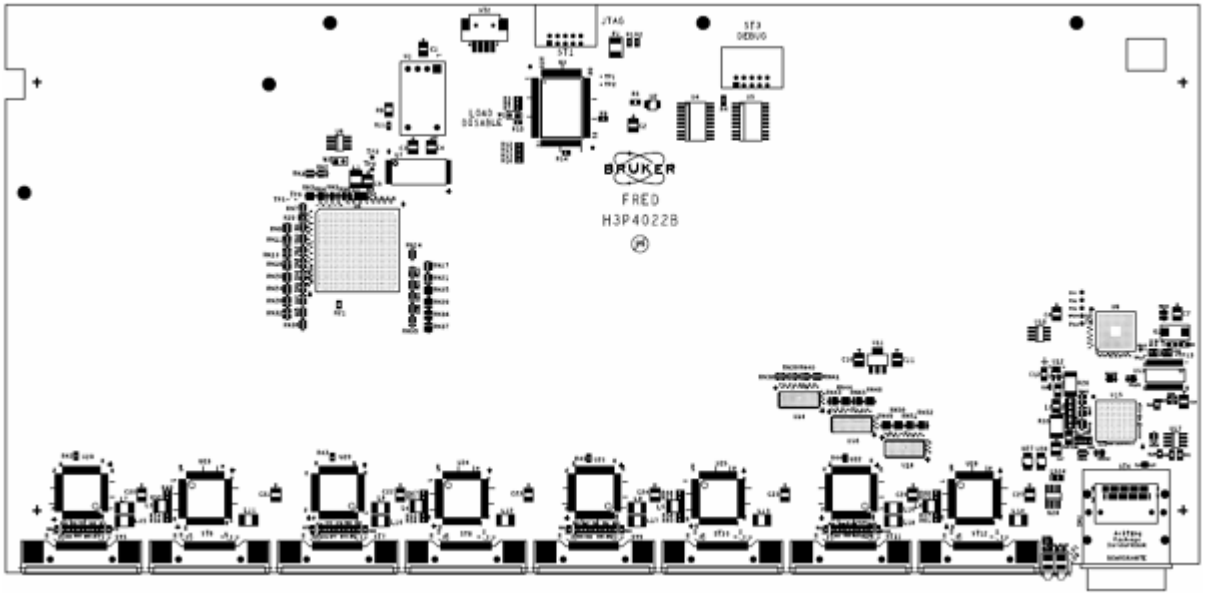


Figure 5.5 FRED Board

5.8 JTAG Structure

Pin Number	Signal		Pin Number	Signal
1	TRST*		6	JTAG Power +5V
2	Cable Detection		7	TMS
3	TDO		8	GND
4	GND		9	TCK
5	TDI		10	GND

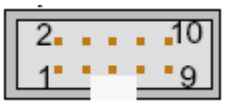


Figure 5.6 JTAG Connector Pin Assignment: Top View Male

Table 5.25 JTAG Connector Pin Assignment

Signal	Description
TRST*	JTAG TAP reset. When asserted low, the TAP controller is asynchronously forced to enter a reset state, which in turn asynchronously initializes other test logic. An unterminated TRST_I produces the same result as if it were driven high. The TAP controller must be reset before the chip can function in normal operating mode.
Cable Detection	Open collector input. Not used in the FRED.
TDO	JTAG serial data out. Signal TDO is the serial output through which test instructions and data from the test logic flow.
TDI	JTAG serial data in. Signal TDI is the serial input through which JTAG instructions and test data enter the JTAG interface. The new data on TDI is sampled on the rising edge of TCK. An unterminated TDI produces the same result as if TDI were driven high.
TMS	JTAG test mode select. Signal TMS causes state transitions in the test access port (TAP) controller. An un-driven TMS has the same result as if it were driven high.
TCK	JTAG boundary scan clock. Signal TCK is the clock controlling the JTAG logic.

Table 5.26 IPSO JTAG Signal Description

IC	JTAG Chain 1	
	IN	OUT
U3	TDI	TD1
U5	TD1	TD2 (buffer only)
U8	TD2	TD3
U9	TD3	TD4
U15	TD4	TD5
U5	TD5	TDO (buffer only)

Table 5.27 FRED JTAG Chain Structure

5.9 Power Requirements

Pin Number	Signal			
1	3.3 V			
2	3.3 V			
3	GND			
4	GND			

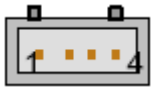


Figure 5.7 ST2 Power Connector Pin Assignment: Top View Male

Table 5.28 ST2 Power Connector Pin Assignment

Part Number	Assembly	+3.3 V
H12607	FRED BOARD	2 Amp

Table 5.29 Power Requirement FRED

5.10 Pin Allocation for the LVDS Connectors

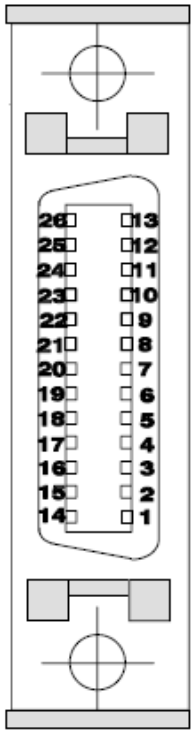


Figure 5.8 Pin Assignment for the 48-Bit LVDS Connector at the PCB

Function	Wire Type	Transmitter Signal	Receiver Signal	Pin Nr.
Signal: Differential pair of the received serial transmit clock connected to the corresponding inputs of the transmitter.	Twisted and shielded	TxCLK_P	RxCLK_P	6
		TxCLK_M	RxCLK_M	18
Shield: Common drain wire of all separate shields, connected to CHASSIS.		LVDS Gnd		26
Signal: Differential pair of the received serial data stream connected to the corresponding inputs of the transmitter.	Twisted and shielded	TxIN_P0	RxIN_P0	3
		TxIN_M0	RxIN_M0	15
Shield		LVDS Gnd		26
Signal	Twisted and shielded	TxIN_P1	RxIN_P1	4
		TxIN_M1	RxIN_M1	16
Shield		LVDS Gnd		26
Signal	Twisted and shielded	TxIN_P2	RxIN_P2	5
		TxIN_M2	RxIN_M2	17
Shield		LVDS Gnd		26
Signal	Twisted and shielded	TxIN_P3	RxIN_P3	9
		TxIN_M3	RxIN_M3	21
Shield		LVDS Gnd		26
Signal	Twisted and shielded	TxIN_P4	RxIN_P4	10
		TxIN_M4	RxIN_M4	22
Shield		LVDS Gnd		26
Signal	Twisted and shielded	TxIN_P5	RxIN_P5	11
		TxIN_M5	RxIN_M5	23
Shield		LVDS Gnd		26
Signal	Twisted and shielded	TxIN_P6	RxIN_P6	12
		TxIN_M6	RxIN_M6	24
Shield		LVDS Gnd		26
Signal	Twisted and shielded	TxIN_P7	RxIN_P7	13
		TxIN_M7	RxIN_M7	25
Shield		LVDS Gnd		26
USB signal pair, left open.	Twisted and shielded	USB+		1
		USB-		14
Shield of the USB signal pair, connected to CHASSIS		USB Gnd		2
Signal: Connected to Bit1 of register „chan-conf“ on F- and G-Controllers.	Individual	CHANNEL_DETECT0		7
Signal: Connected to Bit0 of register „chan-conf“ on F- and G-Controllers.	Individual	CHANNEL_DETECT1		20
VCC of USB power, left open.	Individual	USB pwr		19

Table 5.30 LVDS Connector: Cable and Pin Assignment

GND of USB power, connected to GND.	Individual	USB Gnd	8
Common shield of the entire bundle.	Shield	CHASSIS	body

Table 5.30 LVDS Connector: Cable and Pin Assignment

The CHASSIS pin is connected to a separate plane in the PCB layer stack. This plane is stacked close by the ground plane, giving a very tight capacitive (only capacitive) and low inductance coupling to GND. The chassis plane is screwed together with the external chassis along the front edge near the connectors and the line drivers.

This solution reduces the digital noise at that point and the noise which is picked up by the driver and carried to the outside. In addition this avoids parasitic current through the GND plane which could be caused by potential differences of the remote device.

6 Transport, Packaging and Storage

The FRED unit contains sensitive parts and assemblies that must be handled with care to prevent damage.

i Installation and initial commissioning must only be carried out by employees of the manufacturer or persons authorised by the manufacturer.

Nevertheless, it may happen in the course of installation and further use that the owner‘s operating or maintenance personnel may be entrusted with handling pack units. In this regard, it is vital to observe the instructions listed below.

6.1 Inspection at Delivery

When the FRED is delivered it has to be inspected for completeness and transport damage.

Proceed as follows in the event of externally apparent transport damage:

- Do not accept the delivery, or only accept it subject to reservation.
- Note the extent of the damage on the transport documentation or the shipper‘s delivery note.
- All the shipping cartons should be stored for further investigation.
- Initiate complaint procedures immediately.

6.2 Packaging

The individual packages are packaged in accordance with anticipated transport conditions. Only environmentally friendly materials have been used in the packaging.

The packaging is intended to protect the individual components from transport damage, corrosion and other damage prior to assembly. Therefore do not destroy the packaging and only remove it shortly before assembly.

6.2.1 Handling Packaging Materials

Keep the original container and packing assembly, at least as long the warranty is valid, in case the unit has to be returned to the factory. When the packaging material is no longer needed dispose of in accordance with the relevant applicable legal requirements and local regulations.

6.3 Storage

When the FRED is not installed immediately, it has to be stored in the original packing under the following conditions:

- Do not store outdoors.
- Store in dry and dust-free conditions.
- Do not expose to aggressive media.
- Protect against direct sunlight.
- Avoid mechanical shocks.
- Storage temperature: 5°C to 40°C.
- Relative humidity: Maximum of 80% for temperatures up to 31°C, linearly decreasing to 50% at a temperature of 40°C.
- If stored for longer than 3 months, regularly check the general condition of all parts and the packaging. If necessary, top-up or replace preservatives.

7 Installation and Initial Commissioning

Installation and initial commissioning must only be carried out by Bruker Service personnel or persons authorized by Bruker!

⚠ WARNING

Danger to life from incorrect installation!

Errors during installation may result in potentially hazardous situations and may cause significant damage to property.

- ► Installation must only be carried out according to the instructions provided in this manual.

7.1 Safety

Improper initial commissioning

⚠ WARNING

Danger of injury from improper initial commissioning!

Improper initial commissioning can result in serious injury and significant damage to property.

- ► Before the initial commissioning, ensure that all installation work has been carried out and completed in accordance with the information and instructions in this manual.

Electrical system

⚠ WARNING

Danger to life or material damage from electric power!

Contact with live parts may prove fatal. When switched on, electric components are under high voltage.

- ▶ Switch off the power supply before starting work and make sure that it cannot be switched on again.

7.2 Installation

All the requirements concerning the environment described in the "Operating Environment" on page 12 have to be met before the unit can be installed.

To reduce the risk of electric shock and malfunctioning, install these devices in a temperature and humidity controlled indoor area free of conductive contaminants. The power supply cable is intended to serve as the disconnect device. The socket outlet should be near the equipment and easily accessible.

7.2.1 Console Installation

The FRED unit is mounted in the AQS/3 system P/N Z106171. Check the system and install the unit in an empty slot securing it with the four mounting screws.

7.2.2 External Connections

The following cables have to be connected before the FRED can be put into operation:

1. Connect the PCI Express input at the PCIe, to the PCI adapter installed on the IPSO Unit using cable P/N 1805036.
2. Connect the LVDS Input to a IPSO FCTRL (TX CTRL 1-3) channel using cable P/N 86868.
3. Connect the LVDS outputs SGU1-3 to the appropriate SGU's.
4. Connect the LVDS input ‘Gradient Preampl.‘ to the LVDS output of the DPP.
5. Connect the Output ‘Gradient Ampl.‘ to the BGU (Gradient Amplifier)

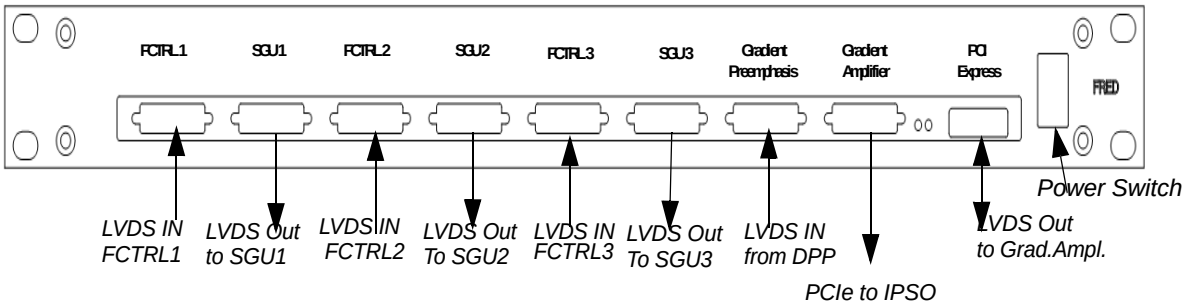


Figure 7.1 External Connections for the PEXMUX8 Unit

For a detailed description of the operation refer to the "Operating Instructions" on page 43.

To operate the FRED unit, turn on the unit before (or simultaneously) switching on the IPSO unit to allow the IPSO to detect the FRED via the PCIe bus. During the start-up the FRED will send a defined LVDS B-word to the connected SGU to prevent data error at the SGU.

The IPSO test program has special commands used to test the correct function of the FRED unit. In this case the LVDS input gradient preamplifier must be connected to the DPP output and the appropriate LVDS input should be connected to the IPSO FCTRL channel. The output channel which should be tested, is normally connected to the SGU, but must be connected to the IPSO RCTRL channel for testing. The FRED outputs are sequentially tested from output SGU1to SGU3.3.

8 Operating Instructions

Before operating the FRED unit, it must be installed as described in section "Installation" on page 40.

To operate the FRED unit, turn on the unit **before** (or simultaneously) switching on the IPSO unit to allow the IPSO to detect the FRED via the PCIe bus. During the start-up the FRED will send a defined LVDS B-word to the connected SGU to prevent data error on the SGU.

8.1 Switching ON the FRED Unit

Switch on the unit by using the power switch on the front panel.

Figure 8.1 Location of the ON/OFF Switch

8.2 Switching OFF the FRED Unit

Switch off the unit by using the power switch on the front panel.

8.3 Operation

Once the unit is switched on there are no further operating procedures for the FRED unit.

The FRED unit is a part of the IPSO system and does not have its own software, rather it is controlled by one of the following software running on the IPSO system:

- TopSpin version 3.1 or higher.
- Paravision version 6.0 or higher.

During operation the user must take great care in following the safety related information provided in this manual.

⚠ WARNING

Danger of injury if personnel are insufficiently qualified.

If unqualified personnel perform work on the unit or are in the units danger zone, hazards may arise which can cause serious injury and substantial damage to property:

- ► Except for CRU‘s, all operations inside the FRED must be carried out by a Bruker service engineer or an authorized agent.

8.4 Operator Protection

The electronic circuitry of the FRED operates with low and safe voltages, except for the power supply and its mains connection. Nevertheless, any electrical equipment may become a source of danger under extreme conditions:

⚠ WARNING

Risk to life due to extreme weather conditions.

During a lighting storm contact with cables may be life-threatening:

- ► Ensure that the electrical power source is properly grounded.
- ► Do not loosen, connect or touch any cables during a lightning storm.

⚠ WARNING

Material or personnel damage from worn or damaged parts.

Damaged or worn parts may result if one or the following circumstances occurs:

- ► The power cord, power plug or power supply are cracked, brittle or damaged.

⚠ WARNING

Electrical hazard from electrical shock.

A life threatening shock may result when the housing is open during operation.

- ► Disconnect the device from the electrical power supply before opening the device. Use a voltmeter to verify that the device is not under power!
- ► Be sure that the power supply cannot be reconnected without notice.
- ► The housing must be closed during operation.

8.5 Unit Protection

NOTICE

Material damage hazard from electrostatic discharge (ESD).

Friction between material being conveyed may result in the buildup of electrostatic potential. Contact with the uncovered metal of the printed circuit board (PCB) may result in material damage.

- ► Potential equalisation must be ensured before making contact with parts.
- ► Where appropriate use ESD flooring and wear ESD shoes.

8.5.1 Incorrect Cable Connections

Incorrect cable connections or disconnecting cables while the unit is under operation may result in improper operation.

- Do not connect a transmitter to the LVDS OUT connectors (SGU1 - SGU3, GRAD. Ampl.) of the FRED unit!
- A LVDS cable should never be removed from or connected to an operating controller. Corrupted data may be sampled as valid.
- The PCIe cable should never be removed while the IPSO Unit is powered up.This will hang up the IPSO unit and the system must be rebooted.

9 Maintenance and Cleaning

9.1 Safety

⚠ WARNING

Danger to life or material damage from electric power!

Contact with live parts may prove fatal. When switched on, electric components are under high voltage.

- ▶ Switch off the power supply before starting work and make sure that it cannot be switched on again.

⚠ WARNING

Danger of injury from improperly executed maintenance work!

Improper maintenance may result in serious injury and significant damage to property.

- ▶ Ensure sufficient assembly space before starting work.
- ▶ Pay attention to orderliness and cleanliness in the assembly location! Loosely stacked or scattered components and tools could cause accidents.
- ▶ If components have been removed, pay attention to correct assembly, refit all fixing elements and comply with bolt tightening torques.

Before the restart, ensure that:

- ▶ All maintenance work has been carried out and completed in accordance with the specifications and instructions in the manual.
- ▶ No persons are in the danger zone.
- ▶ All covers and safety devices are installed and functioning properly.

9.1.1 Environmental Protection

Observe the following environmental protection instructions during maintenance work:

- In respect to all lubrication points supplied manually with lubricant, remove any escaping, used or surplus grease and dispose of it in accordance with applicable local regulations.
- Catch replaced oils in suitable containers and dispose of in accordance with applicable local regulations.

9.2 Maintenance

The FRED unit can be expected to have a long and trouble-free life with a minimum of preventive maintenance. Environmental issues are essential in determining the reliability. The temperature and humidity have to be within specifications. All servicing must be performed by qualified service personnel.

Before maintenance, repair or shipment, the unit must be completely switched off and unplugged or disconnected and dismounted from its rack.

9.3 Cleaning

Cleaning the surface of the enclosure and/or front panel can be carried out by the customer, if the following instructions are adhered to.

1. Switch off the equipment and unplug the power cable and all data cables.
2. Clean up the surface with a dry or damp cloth.
3. Let the enclosure completely dry before installing
4. Connect all cables and power up.

9.4 Service Requests

In case of questions or problems, please contact your nearest Bruker office or representative. See "Contact" on page 51 for details

10 Dismantling and Disposal

After the lifespan of the instrument, Bruker takes responsibility for disassembly and disposal in accordance with the European directive 2012/19/EC WEEE. Bruker BioSpin GmbH offers to take back the components free of charge after usage at the customer site upon request by the customer. If the customer wants to arrange disposal on their own, then this has also to be stated when the product is ordered.

Dismantling and Disposal

11 Contact

Manufacturer:
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Germany
Phone: +49 721-5161-0
http://www.bruker-biospin.com
WEEE DE43181702

NMR Hotlines

Contact our NMR service centers.

Bruker BioSpin NMR provide dedicated hotlines and service centers, so that our specialists can respond as quickly as possible to all your service requests, applications questions, software or technical needs.

Please select the NMR service center or hotline you wish to contact from our list available at:

http://www.bruker-biospin.com/hotlines_nmr.html

Contact

Appendix A

A.1 Warning Signs

Warning Signs

A.2 Figures

Figures

A.3 Tables

Tables

A.4 Glossary

BIOS
Basic Input Output System

CASCON
A conflict analysis system

DPP
Digital Preemphasis Processor

EEPROM
Electrically Erasable Programmable Read-Only Memory

FCTRL
Frequency Controller

FPGA
Field Programmable Gate Arrays

FRED
Frequency Deputy Unit

GND
Ground

JTAG
Joint Test Action Group

PCB
Printed Circuit Board

PCI
Peripheral Component Interconnect

PCIe
Peripheral Component Interconnect Express

PLX
PLX Technology, Inc.

PROM
Programmable Read-Only Memory

ROM
Read Only Memory

RT-client
Real Time Client

SGU

Signal Generation Unit

A.5 Index

T

Revision History List

Index	Date	Alteration Type

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Order No: Z31976