Bruker BioSpin

AVANCE III

IPSO 19" External Unit
Technical Manual

Version 001

think forward

NMR Spectroscopy

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This manual was written by

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Terms and Abbreviations

The following table lists terms and abbreviations used in this dokument.

TOPSPIN−PC	Processing Computer running TOPSPIN; server of the IP-SOs diskless Linux
IPSO	Intelligent Pulse Program Organizer; System consisting of the IMB, the PCI−Host and a different bundle of Controllers
IPSO AQS	IPSO version to be mountet in the AQS−Rack (”Nanobay” or “Microbay”)
IPSO 19” Unit, IPSO 19inch Unit	IPSO version as standalone Case of the 19−Inch Standard
IPSO Host, CCU, PCI−Host, spect	Assemly group containing the IPSO Host Controller (PC module, ETX), Computer Interfaces and the Host Bus (PCI)
IPSO Host Controller	IBM−PC compatible Modulcomputer (ETX)
IPSO AQS Host	IPSO Host of IPSO AQS including computer, interfaces and R−Controller
IPSO Motherboard, IMB	IPSO Host of IPSO 19”−Unit including computer, interfaces and bus structure
IPSO−Tx, TxController, TxCtrl	TxController, capable of sending sequences of application parameters; Single channel for IPSO 19” Unit, five channel for IPSO AQS
IPSO AQS ACQ	Five channel TxController board of IPSO AQS
IPSO−Rx, RxController, RC, rc R−Controller, RxCtrl	RxController, capable of receiving sequences of application results or parameter streams sent by TxCtrl in cases of using the “ipsotest”
T−Controller, TC, tc; F−Controller, FC, FC1, fc, fc1; G−Controller, GC, gc;	TxController with dedicated and application specific functio-nallity for: T=Timing control, F=Frequency control, G=Gradient control; In print messages: “...F−Controller1, (fc1)...” means the first channel frequency controller.

X–Controller, XC, xc Controller Board, Controller	Collektive term of controllers without functional differentiation; means in each case a TC or RC controller based on C6400
U–Controller, UC, uc;	Stands for “unknown controller” and describes a C6400–based controller with unknown content in its version register, e.g. a C6400–based device of an unknown manufacturer
C6400	CPU of the Controller; DSP from Texas Instruments
IMB	IPSO Motherboard, IPSO Host of 19”–Unit
Host–Bus, PCI–Bus	Control–, data– and addressbus for communication between Host Controller and X–Controllers
RCP	Real–Time–Clock–Puls
LVDS Cable	Transmission cable at the LVDS connector of X–Controllers
PCI–Master	PCI device which is able to initiate a transaction over the PCI bus (Host Bus)
Local Address	Onboard address out of the local processor’s address layout, different from the PCI Address in the upper 10 bit
PCI Address	Onboard address out of the PCI bus address layout, different from the Local Address in the upper 10 bit; The Bruker user interfaces use the Local Address only.
channel, Kanal	Controller dedicated to a subtask of the application
AQ–Bus	Bundle of signals which control on a clock base (80 MHz) the channel operation and the communication between the channels
Master Controller	Controller of the zero–delay channel (first one) which decides on the AQ–Bus operation and communicates with the Slave Controllers One exclusive master has to be in the system. Only the ma ster drives many of the AQ–Bus signals.
Slave Controller	A controller which is funcional dependent on the decisions of the Master Controller. “Slaves” have a clock cycle delay with respect to the Master of ≥ 0 It is not allowed to have only Slave Controllers in the system.

Last Slave Controller	Is the Slave with the greatest delay in the system respective to the Master. Only this Slave drives some AQ−Bus signals and communicates with the Master.
Independent Controller	Whenever started runs its own program independent of the AQ−Bus. The Independend Controller drives no AQ−Bus signals. It is not allowed to have only Independend Controllers in the system.
trigger, trigger event, external event	External signal which can assign the time of any decision to the Master Controller
Firmware	Software which is loaded to the controller memory and runs the C6400
AQ device driver	A program that must be loaded into the Linux Kernel which enables access to the X−Controllers
AQSTART	Start of application; carried out via the T−Controller and AQ−Bus
semif	Register to select FIFO or C6400 to load the LVDS output
EDMA, QDMA	Transactions of data between memory ranges and/or interfaces initiated by the DMA controller of C6400; EDMA=Extended DMA, QDMA=Quick DMA (not faster than EDMA)
OPT, SRC, CNT, DST, IDX, RLD	Fields of the DMA controllers: Option, Source, Count, Destination, Index, Reload
EMIFA, EMIFB	Interfaces of the C6400 to the memory and registers; EMIFA=64−Bit, EMIFB=16−Bit

Important Safety Instructions

This Manual covers the spectrometer control unit called IPSO in versions:

- IPSO 19inch

which are used in the *AVANCE III* spectrometers

It is mandatory to read this whole chapter before installation and use !

General Safety Instructions

These instructions refer to any IPSO model.

The IPSO can be damaged by inappropriate usage. The damage could be such, that the equipment must not be used before having been checked by the service.

The user should re−check the equipment at regular intervals for any damage or wear and is expected to inform the service immediately of any abnormality.

Danger	Do not use the equipment and inform the service staff, if you are in doubt about the correct state of any component.

In the unlikely case of one of the following, stop using the equipment, interrupt the current supply, disclose this circumstance to the service staff and ask for instructions:

- The power cord, power plug or power supply are cracked, brittle or damaged
- Signs of excessive heat appear
- There is evidence or suspicion that a liquid has intruded into any enclosure
- The power cord or the power supply have been in contact with any liquid
- The IPSO has been dropped or damaged in any way
- The equipment does not work correctly

Danger	Do not try to service the equipment by yourself, unless you are specifically asked to do so and are given instructions by the service staff. In case of questions or problems, please contact your nearest Bruker office or representative.

Some components of IPSO can be installed or replaced by the customer. These components are referred to as “Customer Replaceable Units” (CRUs), see below.

With the exception of the Customer Replaceable Units (CRUs), all servicing must be performed by qualified service personnel.

Before maintenance, repair or shipment, the IPSO must be completely switched off and unplugged or disconnected and dismounted from its rack.

Special Safety Symbols

These symbols are used on the equipment and/or throughout this manual. They alert to danger and important information:

Warning	This symbol denotes hints or instructions throughout this manual whose noncompliance could lead to erroneous or incalculable behaviour of the system
Danger	Throughout this manual, the symbol indicates hints or instructions whose noncompliance can lead to an injury of the user or whose necessary compliance implies also a risk. On the equipment, the symbol implies also a danger and alerts the user.

 **Danger**	Throughout this manual, this symbol indicates necessary actions which imply a risk of being injured by high voltages. On the equipment, the symbol indicates electrical hazards and alerts the user.
 **Danger**	On the equipment, the symbol indicates hot surfaces and alerts the user.

Product and Manufacturer

The following description refers to:

Product	IPSO 19inch Unit P/N H9987
Manufacturer	Bruker BioSpin GmbH Silberstreifen 4 76287 Rheinstetten (Germany)
Conformity	EN 61010−1

Technical Specifications

Non−Intended Usage

All IPSO models contain generally available computer assemblies and provide their standard interfaces. All IPSO models are not qualified to be used beyond their “Intended Usage” neither as a single computer nor as networked one.

 **Warning**	Do not use IPSO for a purpose other than the described “Intended Usage”

Intended Usage

All IPSO models are dedicated only for the limited purpose of being used to steer the *AVANCE* ^{III} spectrometers of the manufacturer.

Environmental Requirements

Permissible ambient temperature	5 to 40 degree Celsius
Permissible altitude	up to 2000 m (above sea level)
Relative humidity.	max 80% up to 31 degree Celsius and linear decreasing to 50% at 40 degree Celsius
Permissible storage temperature	5 to 40 degree Celsius
Pollution degree	2,according to EN 61010−1 or IEC 60664−1 any pollution is non−conductive, except condensed moisture.
Audible noise	‹ 50 dB

Utility Requirements of “IPSO−19inch Unit”

Ingress protection class	IP 20, secured against touching dangerous points

	inside, not secured against ingress of water.
Overvoltage protection category	CAT II, according to EN61010−1or IEC60664−1 safe against overvoltage by switching, not safe against lightning Surge immunity of PSU is level 3, according to IEC61000−4−5
IEC protection class	Class I, according the IEC 61140, connected to mains by phase, neutral and protective−earth
Input Voltage range	110V to 240 V~
Frequency	50/60 Hz
Input Power	100 VA
Fuse on mains input	250VAC 6.3A
Connection	Socket outlet with phase, neutral and protective−earth according to VDE 0620−1

Weight and Dimensions of “IPSO−19inch Unit”

Weight	11 kg
Dimension	(420x532x85) mm, according to DIN41494 or IEC 297, (84TE, 2HE)

Preparation and Transportation

Because of the IPSO contains a large amount of sensitive and damageable parts and assemblies, it must be handled with care and must not be dropped.

Storage

If the IPSO is not installed immediately, it has to be inspected for any damage during shipment and must be stored in the original packing.

Attention has to be paid to the recommended storage conditions, the temperature and the protection from moisture.

Unpacking

All packing materials have to be removed. The equipment must be inspected for any damage during shipment.

If damage has occurred during transit, all the shipping cartons should be stored for further investigation. A claim for shipping damage has to be advised immediately.

Installation

All the requirements concerning environment described in the Technical Specifications have to be met.

To reduce the risk of electric shock and malfunctioning, install these devices in a temperature−controlled and humidity−controlled indoor area free of conductive contaminants.

The power supply cord is intended to serve as the disconnect device. The socket−outlet should be near the equipment and should be easily accessible.

The installation of IPSO has to meet all instructions of the “User’s Guide” and of Chapter “1.” of this manual.

Each IPSO model has to be installed in its dedicated rack:

IPSO 19inch Unit: AVANCE CONSOLE WIRED MICROBAY
P/N H03128

Make sure that ventilation and space requirements are according to specification. There must be clearance at the rear for ventilation and at the front for operation.

Make sure that cabling can not be a source of danger.

All cables have to be connected before the IPSO is put into operation.

Operating Instructions

The only user operations permitted are:

- Starting up and shutting down the IPSO
- Operating the users software interface
- Connecting data interface cables
- Replacing the Customer Replaceable Units (CRUs)

These operations must be performed according to the instructions in Chapter “1.” et seq. of this manual. During any of these operations the user must take the greatest care and perform only the prescribed operations.

Do not operate the equipment in the presence of flammable gases or fumes.

Warning	Except for CRUs, all operations inside the IPSO must be carried out only by a service engineer from the manufacturer or from an agent authorized by the manufacturer.

Operator Protection

The electronic circuitry of IPSO is operating with low and safe voltages, except for the power supply and its connection to mains. Nevertheless, any electrical equipment can become a source of danger under extreme conditions.

Danger	Do not loosen, connect or touch any cable during lightning.

Danger	Do not use a cable that shows any signs of damage or that have been stressed and could be damaged.

Do not open the IPSO enclosure, except for replacing CRUs.

Where opening of the IPSO enclosure is necessary, switch off and let five minutes elapse to let hot spots cool down.

Pay attention to the special Safety Symbols inside.

Danger	Do not open the power supply. There may be dangerous voltage. In case of service, the fan of the power supply can be exchanged without opening the power supply and without opening the IPSO enclosure.

Function Protection

Handling under ESD safety conditions is absolutely necessary.

Warning	Don’t touch uncovered metal of the PCB, electronic devices and connectors before discharging yourself!
Warning	Do not connect a receiver to the LVDS connector of the controller in Slot2 of the IPSO 19” Unit. There will never be valid data.
Warning	A LVDS cable should never be removed from or connected to a powered controller. Corrupted data could be sampled as valid.
Warning	Do not connect more than one Gradient Amplifier to the same system.

Customer Replaceable Units (CRUs)

To insert and remove the Customer Replaceable Units, follow the instructions in Chapter “1.” of this manual.

Replacing CRUs requires opening of the enclosure. Before doing this, the unit must be completely switched off and unplugged or disconnected and dismounted from its rack.

Warning	In case of IPSO−AQS, the replacement of units should be left to qualified service personnel.

Depending on the IPSO model, there are the following replaceable units:

IPSO 19inch Unit:	IPSO−TxController Board	P/N H12538F2
	IPSO−RxController	P/N H12532
	PC 2CH RS232 PCI Adapter	P/N O10394
	PCI RxController	P/N H12565
	DPP1 Digital Preemphasis Board	P/N H12513F1
	RTC Battery 3V Lithium	P/N 72385, type “Varta CR2032”

Maintenance and Cleaning

Cleaning

Cleaning the surface of the enclosure and/or front panel can be carried out by the customer, if the following instructions are adhered to.

1. Switch off the equipment and unplug the power cable and all data cables.
2. Clean up the surface with a dry or damp cloth.

Warning	Use only water or a mild detergent. The surface might be damaged or etched, if solvents were to be used.

3. Let the enclosure completely dry before installing

4. Connect all cables and power up.

Maintenance

Any IPSO model can be expected to have a long and trouble−free life with a minimum of preventive maintenance. Environmental issues are essential in determining the reliability. The temperature and humidity have to be within specifications. The area around should be kept relatively clean and dust free.

With the exception of the Customer Replaceable Units (CRUs), all servicing must be performed by qualified service personnel.

Before maintenance, repair or shipment, the unit must be completely switched off and unplugged or disconnected and dismounted from its rack.

Service Requests

In case of questions or problems, please contact your nearest Bruker office or representative.

A list of all our offices is published on the web:
`http://www.bruker-biospin.com/contact_us.html`

Intelligent Pulse Sequenz Organizer (IPSO)

This Manual covers the spectrometer control unit called IPSO in versions:

- IPSO 19inch

which are used in the *AVANCE III* spectrometers

Chapter “1.” summarizes the most essential informations for users to get started quickly and to avoid beginner’s mistakes without reading plenty of pages.

Chapter “2.” lists the part/order numbers of the main assemblies, subassemblies and devices.

Chapter “3.” et seq. provide the more detailed descriptions of assemblies and devices.

1. Condensed Introduction to the Essentials

Do’s and Don’ts

- Do not connect a receiver to the LVDS connector of the controller in Slot2 of the IPSO 19” Unit. There will never be valid data.
- A LVDS cable should never be removed from or connected to a powered controller. Corrupted data could be sampled as valid.
- Do not connect more than one Gradient Amplifiers to the same system.

1. 1. Structure and Features

Features

- IPSO is a digital spectrometer control unit with a variable number of output channels (TxControllers)
- Each TxController outputs a stream of 48−bit words at a clock rate of 80 MHz per word
- Transferral of a complete set of frequency parameters requires two words.
- The time resolution of parameter switching in any combination of Frequency, Phase, Amplitude is 12.5 nsec.
- The minimal duration of any combination of parameters is 25 nsec.
- Gradient channels require one word per gradient.
- The maximal number of addresses for different gradients (the max. number of gradient channels) is 1k.
- A constant time delay between the outputs of the different TxControllers may be adjusted to any number of 80MHz clock cycles up to 2^{29}x12.5nsec

Structure

The distinctive Parts of the system are the Host Controller charged with administrative tasks, the number of TxControllers generating and transferring the parameter sequences and the Sequencer providing for a means of communication between the TxControllers.

The Controllers

The system contains the 3 types of controllers, Host Controller, RxController and the TxController.

Host Controller: There is only one Host Controller in the system. The Host Controller is an IBM compatible PC with all standard interfaces thus making access possible to the whole pool of standard hardware and software.

The Host Controller boots its operating system software (diskless LINUX) from and communicates with the TOPSPIN−PC over Ethernet. It also communicates over its standard interfaces with the Rx− and the TxControllers and with peripheral devices.

RxController: The RxController is able to receive 48−bit words at its LVDS interface at a rate of up to 100−Mega words. Therefore it can be used as a fast data link from the receiver channel to the transmit channel, bypassing the ethernet and the TOPSPIN−PC. Furthermore all TxControllers and their LVDS interfaces can be tested with the IPSOTEST if their interfaces are connected to a RxController.

Realtime processing of that data can be done by an onboard DSP. The processed data can be transferred by the DMA channels of the DSP over the system bus to any other controller or may be fetched by any other controller.

Usually there is one RxController in the system. Without additional software (that means transparent to the software) it is possible to include additional RxControllers using extension boxes.

The RxController has no connections to the Sequencer and communicates and exchanges data with other controllers via the system bus. It will function in any slot of the IPSO but should be inserted in slot 1.

TxController: Depending on its configuration, the TxController can be used for any of the 3 output functions in the system. These functions are the T−Controller servicing the RCP outputs at T0 with timing signals, the F−Controller generating the frequency parameters for the SGUs and the G−Controller generating the gradient packets for the amplifiers.

The TxControllers and their common Sequencer are the most decisive parts of the IPSO system. The Sequencer is a single device, just one piece of silicon. It contains the communication and decision making logic of all TxControllers and the communication bus between them known from former systems as the AQ−Bus. The AQ−Bus allows for real time communication on a 1−clock base of 12.5 nsec.

The controller itself consists of a DSP with memory, FIFO, output logic and interfaces to the system bus and the Sequencer. The DSP gets its code from the Host Controller, generates the parameter sequences and writes them into the FIFO. Its most important task is to keep the FIFO full. The Sequencer (once started) reads the words out of the FIFOs of all controllers, realizes the defined timing in each channel and controls the outputs.

The global functions of the Sequencer (e.g. START, STOP, SUSPEND, RESUME and so on) are part of the Sequencer logic of the T−Controller. Therefore a T−Controller has to be in the system to carry out any type of acquisition.

LVDS

The LVDS cable is the transport media for digital data words between the Tx− and the RxControllers respectively and the peripheral devices like SGU, Gradient Amplifier, DRU and DPP

(Digital Preemphasis Processor). The abbreviation LVDS means “low voltage digital signal”. The voltage switching range of the data lines is between 1.0V and 1.4V.

The used devices take 48−bit data words at a clock rate of 80MHz (and 100MHz between DRU and RxController respectively) and serialize and transport them over 8 balanced data line pairs accompanied by one clock pair. At the receiver side the data stream is deserialized and the 48−bit data word and its 80MHz clock are reconstructed.

Because there are 8 data lines, the cable has to transport 6 data bit plus one balance bit per 12,5nsec. That means a bit frequency of 560MHz on each data line. Since a good signal quality needs a good transmission behavior up to the fifth harmonic wave this cable has to transport the signals up to about 3−GHz without frequency dependent distortions.

The LVDS cable driver is always active even if the TxController is transmitting no valid data.

There are 2 options called “Deskew” and “Preemphasis” which are intended to compensate the negative influence of cables longer than about 3 meters to the signal quality. The usual cable length below 2 meters requires neither Deskew nor Preemphasis.

Deskew: This feature minimizes the effective skew of the different data line pairs in the cable. To be effective it has to be enabled at the receiver and carried out at the transmitter. The default state at introduction is “NOT ENABLED” at the receiver and is activated at the transmitter by a software command only.

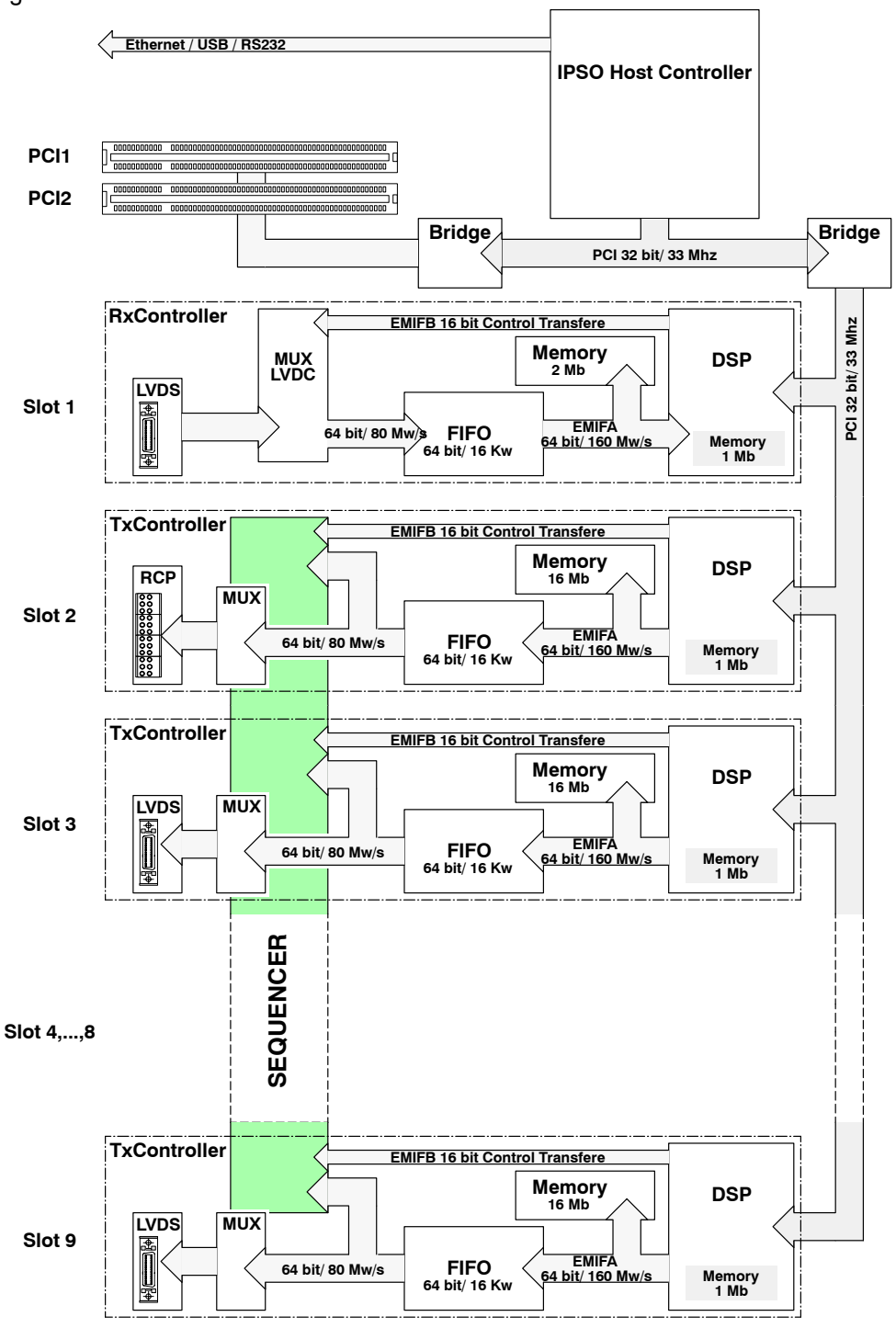
If enabled at the receiver Deskew has to be carried out after power−up and again each time after the cable has been plugged out and in under power. This can be done by software using the command “`Deskew`” of the “`ipsotest`” program.
Software activated Deskew needs TOPSPIN 2.0b6 and a TxController with Part# “H12538F2”. Otherwise with “Deskew enabled at the receiver” the system has to be powered up again after reconnecting.

Preemphasis: This feature compensates for the greater need of charge on cables longer than 2 meters. To be effective it needs one cable−length−dependent resistor at the transmitter. If ever necessary such Tx_Controllers will be given a special part number.

The state of the TxControllers with part number “H15538” and ”H15538F1” and H12538F2 is “NO PREEMPHASIS”

Besides the data and clock lines the LVDS cable includes 4 lines of an USB channel (unused so far) and 2 state lines. The state lines tell the TxController the kind of the connected device like “unconnected, SGU connected, Gradient Amplifier connected, DPP connected”.

Figure1: Block diagram of the IPSO 19” Unit



1. 2. Handling

ESD

Handling under ESD safety conditions is necessary.
Don’t touch uncovered metal of PCB and connectors before discharging yourself!

Boot procedure

The IPSO needs to boot its diskless LINUX from the TOPSPIN−PC via the Ethernet. This connection with or without an hub included requires the following cable:

Connection	Type	Color	Part#	Length
point–to–point	UTP/CAT5, crossed	red	84338	5m
			83980	10m
point–to–hub	UTP/CAT5, straight	white	83025	5m
			83026	10m

If connected, the IPSO needs only to be switched on or to be resetted to begin booting.

Power ON/OFF Button
To be effective this button needs to be pressed for about 2 seconds to switch the system on and 6 seconds to switch it off.

Reset Button
This button resets the Host Controller, the PCI logic and restarts the boot process. So it leads to the same result as ON/OFF without Power OFF.

Board Installation

Opening the IPSO 19” Unit
The case of the IPSO has to be opened to facilitate controller/PCI card installation. To do that it is only necessary to remove the two screws (right and left) of the top cover next to the front side.

Rules of Modularity on the IPSO 19” Unit
There are two kind of controllers (RxController and TxController) which can be plugged into the 9 slots. Some of the slots are dedicated to a unique controller and some stamp a special function on the generic TxController:

RxController: Slot1 is intended to be used by the RxController only. But it would work as receiving controller in any other slot.

TxController: Slot2 to Slot9 are designed to be TxController’s places. Plugged into Slot1 the TxController would be recognized as “unknown” (U–Controller) but it will not be able to communicate with the sequencer and to transmit data.

Slot2: Only this slot provides access to the acquisition global functions like START, STOP and so on and to the RCP outputs. Therefore the TxController in this slot gets the task of the T–Controller. It controls the RCP outputs instead of its LVDS output. Do not connect a cable to this LVDS connector. The LED below this connector is always off.

Slot3 to Slot9: TxControllers in these slots can work as F–Controller (default) or G–Controller.

The LED below the LVDS connector lights green at the F–Controller and yellow at the G–Controller.

The channel numbering of the F–Controller begins at the leftmost one and counts up to the right. There must not be any gap between the F–Controllers.

Which F–Controller will become the G–Controller?
Only the F–Controller which is connected to a Gradient Amplifier will be configured as G–Controller and its LED below the LVDS connector will change from green to yellow.

Connecting more than one Controller to a Gradient Amplifier is not supported by TOPSPIN.

Previous to Rel.2.0, TOPSPIN will only allow the last F−Controller of a system to become the G−Controller. This would be the last one at the right side on “IPSO 19” Unit” and F/G−Controller−4 on “IPSO AQS”.

A later release might advantageously allow the G−Controller to be freely selected by connecting the Gradient Amplifier.

Until then an arbitrary F−Controller can be selected as G−Controller if all higher numbered F−Controllers will be logically disabled.

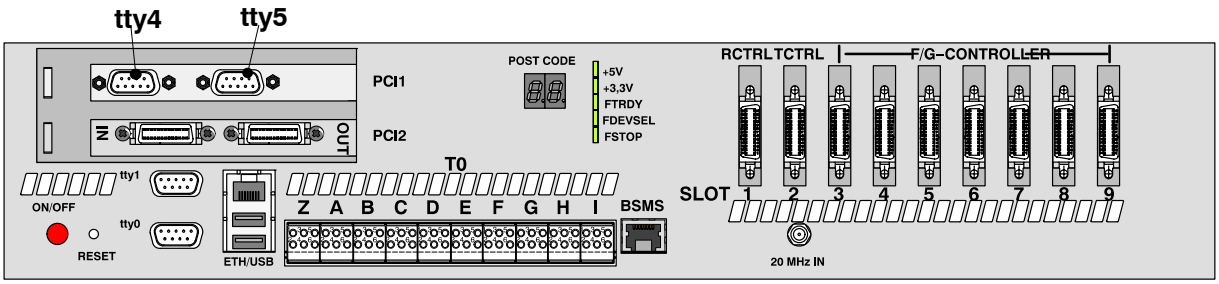
For Example:
You use 3 F−Controllers and 1 G−Controller which is in the slot of FxController−4.
If you want to disable the present G−Controller and use FxController−3 instead, you have to

1. unplug the LVDS−Cable from previous G−Controller
2. plug the LVDS−Cable to FxController−3
3. login to IPSO as root
4. and run
   `root@IPSO:/opt/test>sh aqmod.sh -disable fctrl4 ↵`

1. 3. Ports

The IPSO services the following Input− and Output Ports

Figure2: Front View of IPSO 19” Unit



PCI Slots

The two standard PCI slots meet the “PCI Local Bus Specification, Rev.2.1”. Both slots are intended for 5−Volt signaling cards (IPSO AQS can accept short cards only).

The total power consumption, summarized for both slots, must not exceed the following values:

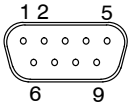
IPSO 19” Unit: 10A from +5V and 3.5A from 3.3V

Connectors

tty0, tty1: RS232C on ETX module, max. baud rate 115.2Kbaud
The configuration of the tty−interfaces (parity, number of stop bits, kind of handshake, baud rate) is defined and set by the application program.

Type of connector is D−Sub, 9 pin, female

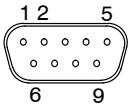
Pin #	Signal	Pin #	Signal	Pin #	Signal
1	RI	4	DTR	7	RTS
2	RxD	5	GND	8	CTS
3	TxD	6	DSR	9	not con.



tty4, tty5: RS232C on auxiliary PCI adapter EX−41052,
max. baud rate 115.2Kbaud
The configuration of the tty−interfaces (parity, number of stop bits, kind of handshake, baud rate) is defined and set by the application program.

Type of connector is D−Sub, 9 pin, female

Pin #	Signal	Pin #	Signal	Pin #	Signal
1	CDC	4	DTR	7	RTS
2	RxD	5	GND	8	CTS
3	TxD	6	DSR	9	RI



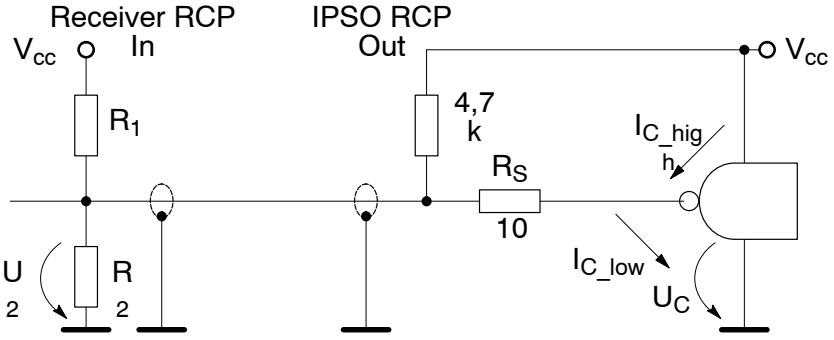
ETH 10/100 BaseT, Intel 82551ER

USB USB 1.1 OHCI

The Real Time Pulses (RCP) on Connector T0

Electrical Properties and Constraints of the RCP outputs and receiver inputs
The high and low switching levels (U_2) and the associated current (I_c) of the RCP signals depend on the circuitry and driving capacity of the driver and the circuitry of the connected receiver.

Figure3: RCP Circuit



$V_{CC} = 5V$

$U_{C\_low} = 0,3V$

$U_{C\_high} = (3,0..3,3)V$ $U_{2\_low/high} = \frac{\left\{V_{CC} + U_{C\_low/high} \times \frac{R_1}{R_S}\right\}}{\left\{1 + \frac{R_1}{R_2} + \frac{R_1}{R_S}\right\}}$ $I_{C\_low/high} = \frac{\left\{U_{2\_low/high} - U_{C\_low/high}\right\}}{R_S}$

The table shows the resulting voltage levels and currents for some combinations of R_1/R_2. Other combinations are possible and can be checked by the formulas above.

Table1: RCP voltage levels and currents

Parameter	Combinations of Input Circuit				Units
R_1	100	100	100	200	Ohm
R_2	68	∞	100	200	Ohm
U_2 if I_C=0	2,0	5,0	2,5	2,5	V

Parameter	Combinations of Input Circuit				Units
U_{2_low}	0,64	0,73	0,66	0,5	V
U_{2_high}	2,8	3,18	2,91	2,95	V
I_{c_low}	34	43	36	20	mA
I_{c_high}	–20	–12	–30	–25	mA

Signals and Location

IPSO 19” Unit

The signals which are available at the front side connector T0 are:

Type of Signal	Direct.	Name	Count
RCP Output	out	TCU_xy	51
Trigger Input	in	Trig 1,...,4	4
Extern Suspend	in	EXT_MAN_SUSP	1
Extern Stop	in	EXT_MAN_STOP	1
Emergency Stop	in/out	EX_SGU_RES	1
Peripheral Status	in	SGU_ST	1
Next Value Clock for Preemphasis	out	EXT_GCLK	1

Another 19 RCP signals (red shadowed in column “T0”) are available at connector ST47 inside of the IPSO case.

Figure4: RCP pin location of IPSO 19” Unit

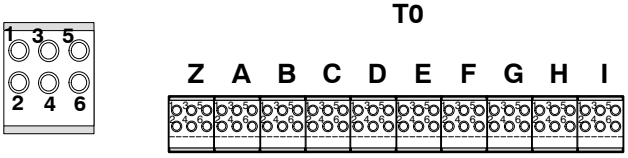


Table2: Pin assignment of the RCP signals on IPSO 19” Unit

Source/ Destination	RCP and Control Signals of the T–Controller on IPSO 19” Unit								NMR		
	FIFO Word+ Bit Position (64,...,1)		tctrl output reg. tout0, ..., tout4	set nmr 0(#)	set nmr 3(#)	set nmr 4(#)	Layout Name	Direction			
	A	B							Meaning	T0	BSMS
BSMS/ LCB		2	T0(0)		0		TCU62	out	!LOCK_HOLD	B1	2
BSMS/ SCBR		3	T0(1)		1		TCU0	out	!HOMOSPOIL	B2	6
1H Transm.		4	T0(2)		2		TCU1	out	SELH_!H/F	B4	
1H Transm.		5	T0(3)		3		TCU2	out	SELX_!X/F	B5	
BSMS/ LCB		6	T0(4)		4		TCU3	out	!INT_A_(Z0)	B3	4

	RCP and Control Signals of the T–Controller on IPSO 19” Unit										
Source/ Destination	FIFO Word+ Bit Position (64,...,1)		tctrl output reg. tout0, ..., tout4	set nmr 0(#)	set nmr 3(#)	set nmr 4(#)	Layout Name	Direction	NMR		
	A	B							Meaning	T0	BSMS
BP		7	T0(5)		5		TCU4	out	MIXCC	B6	
		8	T0(6)		6		TCU5	out	res	C1	
HPPR		9	T0(7)		7		TCU6	out	RCP_PA_SWITCH	C2	
QNP		10	T0(8)		8		TCU7	out	FXA	C3	
QNP		11	T0(9)		9		TCU8	out	FXB	C4	
		12	T0(10)		10		TCU9	out	res	D1	
		13	T0(11)		11		TCU10	out	res	D2	
		14	T0(12)		12		TCU11	out	res	D3	
		15	T0(13)		13		TCU12	out	res	D4	
		16	T0(14)		14		TCU13	out	res	D5	
		17	T0(15)		15		TCU14	out	res	D6	
		18	T1(0)		16		TCU15	out	res	G1	
		19	T1(1)		17		TCU16	out	res	G2	
		20	T1(2)		18		TCU17	out	res	G3	
		21	T1(3)		19		TCU18	out	res	G4	
		22	T1(4)		20		TCU19	out	res	G5	
		23	T1(5)		21		TCU20	out	res	G6	
		24	T1(6)		22		TCU21	out	res	H1	
		25	T1(7)		23		TCU22	out	res	H2	
MED		26	T1(8)		24		TCU23	out	ECG_START_TRIG	H3	
MED		27	T1(9)		25		TCU24	out	AUT_TUNG_IN	H4	
MED		28	T1(10)		26		TCU25	out	AKTIV_DEC_RES	H5	
MED		29	T1(11)		27		TCU26	out	AK-TIV_DEC_RES	H6	
MED		30	T1(12)		28		TCU27	out	Customer specified	I1	
MED		31	T1(13)		29		TCU28	out	Customer specified	I2	
MED		32	T1(14)		30		TCU29	out	Customer specified	I3	
MED		33	T1(15)		31		TCU30	out	Customer specified	I4	
		34	T2(0)			0	TCU31	out	GAIN_0_TR1	ST47 pin 1	

	RCP and Control Signals of the T–Controller on IPSO 19” Unit										
Source/ Destination	FIFO Word+ Bit Position (64,...,1)		tctrl output reg. tout0, ..., tout4	set nmr 0(#)	set nmr 3(#)	set nmr 4(#)	Layout Name	Direction	NMR		
	A	B							Meaning	T0	BSMS
		35	T2(1)			1	TCU32	out	GAIN_1_TR1	ST47 pin 3	
		36	T2(2)			2	TCU33	out	C/AB_TR1	ST47 pin 5	
		37	T2(3)			3	TCU34	out	GAIN_0_TR2	ST47 pin 7	
		38	T2(4)			4	TCU35	out	GAIN_1_TR2	ST47 pin 9	
		39	T2(5)			5	TCU36	out	GAIN_2_TR2	ST47 pin 11	
		40	T2(6)			6	TCU37	out	GAIN_2_TR1	ST47 pin 13	
1H1 KW AMPL		41	T2(7)			7	TCU38	out	RELAY_H	E3	
X1 KW AMPL		42	T2(8)			8	TCU39	out	RELAY_X	E4	
X1 KW AMPL		43	T2(9)			9	TCU40	out	RELAY_Y	E5	
		44	T2(10)			10	TCU41	out	res RACK_ON/ OFF	E6	
		45	T2(11)			11	TCU42	out	RCP	F1	
X1 KW AMPL		46	T2(12)			12	TCU43	out	RELAY Z	F2	
		47	T2(13)			13	TCU44	out	RCP_Scope	F3	
		48	T2(14)			14	TCU45	out	RCP_EXT_ DEV	F4	
		49	T2(15)			15	TCU46	out	RCP	F5	
HIGH POWER		50	T3(0)			16	TCU47	out	STP1_DIR	ST47 pin 15	
HIGH POWER		51	T3(1)			17	TCU48	out	LB_SEL	ST47 pin 17	
HIGH POWER		52	T3(2)			18	TCU49	out	DCM_STRT	ST47 pin 19	
HIGH POWER		53	T3(3)			19	TCU50	out	STP1_CLK	ST47 pin 21	
HIGH POWER		54	T3(4)			20	TCU51	out	STP2_CLK	ST47 pin 23	
HIGH POWER		55	T3(5)			21	TCU52	out	RES_STP1	ST47 pin 25	
HIGH POWER		56	T3(6)			22	TCU53	out	DCM_RES	ST47 pin 27	

Source/ Destination	RCP and Control Signals of the T−Controller on IPSO 19” Unit										
	FIFO Word+ Bit Position (64,...,1)		tctrl output reg. tout0, ..., tout4	set nmr 0(#)	set nmr 3(#)	set nmr 4(#)	Layout Name	Di-rec-tion	NMR		
	A	B							Meaning	T0	BS MS
HIGH POWER		57	T3(7)			23	TCU54	out	GO_POS	ST47 pin 29	
2H Lock Switch		58	T3(8)			24	TCU55	out	SEL_2H AMP and TUNE_MODE in MRIs only	A1	
		59	T3(9)			25	TCU66	out	res	ST47 pin 31	
		60	T3(10)			26	TCU57	out	res	Z2	
		61	T3(11)			27	TCU58	out	Q_SWITCH and SCO/CCO in MRIs only	A3	
2H Lock Switch		62	T3(12)			28	TCU59	out	SEL_!X/2H and REF_MODE in MRIs only	A2	
		63	T3(13)			29	TCU60	out	res	F6	
		64	T3(14)			30	TCU61	out	res	I5	
	58		T3(15)			31	TCU56	out	res	I6	
GRASP	59		T4(0)	32			TCU63	out	BLK_GRAD_X	A4	
GRASP	60		T4(1)	33			TCU65	out	BLK_GRAD_Y	A5	
GRASP	61		T4(2)	34			TCU64	out	BLK_GRAD_Z	A6	
	62		T4(3)				TCU67	out			
	63		T4(4)				TCU68	out			
	64		T4(5)				TCU69	out			
BP HR MAS							TRIG1	in	Trigger 0	C5	
BSMS SLCB							TRIG2	in	Trigger 1	C6	
TRIG STRAFI							TRIG3	in	Trigger 2	E1	
TRIG Solid MAS							TRIG4	in	Trigger 3	E2	
Ext. Button							EXT_MAN_SUSP	in	Manual Suspend	Z5	
Ext. Button							EXT_MAN_STOP	in	Manual Stop	Z6	
							EX_SGU_RES	in/out	Emergency Stop	Z3	

	RCP and Control Signals of the T−Controller on IPSO 19” Unit										
Source/ Destination	FIFO Word+ Bit Position (64,...,1)		tctrl output reg. tout0, ..., tout4	set nmr 0(#)	set nmr 3(#)	set nmr 4(#)	Layout Name	Direction	NMR		
	A	B							Meaning	T0	BSMS
SGU							SGU_ST	in	STATUS	Z4	
DPP							EXT_GCLK	out	NEXT VALUE	Z1	
							GND				1,3,5

1. 4. Boot Operation

A successful boot operation requires the ethernet connection to the powered TOPSPIN−PC which services a valid “diskless”, the correct BIOS adjustments on the “IPSO Host Controller” and pushing the Power−On button for about 2 seconds.

The successful completion of the boot process can be checked in TOPSPIN by typing

```
ha↵
```

or in a LINUX shell by typing

```
/opt/topspin/prog/bin/scripts/GetSpectDev −i↵
```

Both methods return the IP−Address of the connected IPSO.

The boot process is automatically controlled by the DHCP process. Normally there is nothing to configure and thus nothing to set incorrectly. The causes of an unsuccessful boot process can only be:

- LAN Boot in BIOS not enabled. To enable the LAN Boot feature would require the connection of a monitor and a keyboard to the IPSO
- A corrupted “diskless” on the TOPSPIN−PC, which should be installed again
- A hardware error, which would necessitate further investigation of the boot process to get some more information.

Investigating the Boot Process

Additional information about the boot process can be obtained from 3 sources and from different phases of the boot sequence

1. By monitoring the POST code display and beep codes
   (requires no additional resources)
2. By configuring the Hyper Terminal application (Windows) or the “cu” application (LINUX) on the TOPSPIN−PC.
   (Shows messages of bootloader and LINUX)
3. By connecting a monitor and a keyboard to the IPSO
   (Shows all messages during the boot process and provides access to the BIOS adjustments)

POST Code Display

The Power−on−self−test and configuration routines (POST) start just after Power−on. The POST code points to the individual parts which are currently just running or have stopped in

case of an error. This sequence normally ends after about 20 seconds with “C0 = Trying to boot OS”

The list of references between POST codes and routines may be found in the addendum or can be loaded from the webside of “PHOENIX Technologies Ltd” (PhoenixBIOS 4.0, Rev.6).

The POST code display is undefined after start of Linux.

Occasionally occurred BIOS errors:

POST Code	POST Routine	Possible Causes	Recommended Actions
28	Auto size DRAM	DRAM error	1.Check insertion of the DRAM in the socket 2.Exchange DRAM or PC–Module
49	Unsuccessful PCI configuration	Faultily inserted PC–Module (Host Controller)	1.Check insertion of the PC–Module 2.Remove the controllers one after the other and try again 3.Check voltages of the Power Supply 4.Exchange the PC–Module
		Any defective Tx– or RxController in the system	
		Defective RESET sequence	
60	Check extended memory	Normal BIOS routine which takes about 10 seconds; the duration is dependend on the volume of memory	If the test doesn’t finish, check the correct fit of the memory.
98	Search for any extention ROM	Normal BIOS routine which takes only a few seconds	If the test doesn’t finish, check the correct fit of the PC–Module and any PCI–Connection.
B0	Check for errors, stops at B0 with 2 beeps in case of error	The timer containes corrupted time and date information.	To recover the content of the timer: 1. Press the RESET button or 2. Connect an USB–keyboard and press F1 to resume and correct time and date with LINUX or 3. Connect a monitor too, press F2 to enter the BIOS setup and correct the time and date or set “Hold on errors” to “NO”
C0	Try to boot	Successful BIOS process but “No Operating System found”	1.Check Ethernet connection. Yellow LINK LED on? Green Rx/Tx LED active? 2.Check in BIOS if Netboot=yes? (see below) or Netboot is at the top of the list in the submenu “Boot Device Priority” and set the item “Onboard LAN PXL ROM” to “Enabled”

Note: The PC–Module can be pulled off after removing the 4 screws on top of the Module.

To check or exchange the DRAM, the module has to be opened after removing the 2 screws at its bottom side.

Acoustic Beep Codes

Additional to the POST code display some POST routines sound a beep code on error. This beep code is derived from the hexadecimal POST code of the failing test as follows:

1. The 8–bit error code is broken down to four 2–bit groups.

2. Each group is made one–based (1 through 4) by adding 1.

3. Short beeps are generated for the number in each group.

Example: POST code 16h = 00 01 01 10 = 1–2–2–3 beeps

The “Hyper Terminal” or “cu” window

The boot messages of the IPSO−OS (LINUX) can be printed in a window of the TOPSPIN−PC. This needs a RS232 connection from tty0 of IPSO to a COM port of the TOPSPIN−PC. For details see the TOPSPIN Installation Guide.

Monitor and Keyboard at IPSO

The most detailed information about the boot process can only be obtained by connecting an additional monitor and a keyboard to the connectors inside of the case. It is then possible to watch the BIOS and Linux Messages during the boot sequence and to enter the BIOS setup utility.

Boot Sequence

	Phase of Boot Sequence	Post Code	POST Beeps	Operation
1.	Power On			
2.	Running POST Code	16h	1−2−2−3	Check BIOS ROM checksum
		20h	1−3−1−1	Test DRAM refresh
		22h	1−3−1−3	Test 8742 Keyboard Controller
		2Ch	1−3−4−1	RAM failure on address line xxxx*
		2Eh	1−3−4−3	RAM failure on data bits xxxx* of low byte of memory
		30h	1−4−1−1	RAM failure on data bits xxxx* of high byte of memory
		46h	2−1−2−3	Check ROM copyright notice
		4Ah		
		58h	2−2−3−1	Test for unexpected interrupts
		59h		
		6Eh		
		87h		
		98h	1−2	Search for option ROMs
		B0h	1−1	Halt on error
		C0h		Try to boot
3.	DHCP Process			IPSO applies for an IP address at the DHCP server
4.	Running Boot Loader			Load and Start of Bootloader First message sent to the Hyper Terminal window from Boot Loader
5.	Loading the OS			Boot messages of Linux in Hyper Terminal

Checking the BIOS Setup

This requires a monitor and a keyboard at IPSO.

The majority of BIOS items should retain their default values. The complete list of items and its values can be found in the “Addendum”.

To show the BIOS version press the Pause key after start of booting.

To investigate and modify the BIOS adjustments start the BIOS setup utility by pressing F2 when the following string appears during bootup.

```
Press <F2> to enter Setup
```

Note: Selecting incorrect values may cause boot failures. Load setup−default values to recover by pressing <F9>

Table3: BIOS adjustments

Entry	Meaning	Phönix BIOS 4.0, Rel. 6.0
Kontron−Version		MOD9R111
Network boot support?		yes
Display Control → Flat Panel Type		Auto Detect
PNP OS Installed	PCI Bridge Support	no
Onboard LPT	Used for JTAG	enable
Legacy USB Support	Global, Interface 0+1, extern	enable
On Chip USB 2 Device	Interface 2+3, intern to Slot A+B	disable
PCI Configuration → PCI IRQ Line1	IRQ select for Line “w”	Auto Select
PCI Configuration → PCI IRQ Line2	IRQ select for Line “x”	Auto Select
PCI Configuration → PCI IRQ Line3	IRQ select for Line “y”	Auto Select
PCI Configuration → PCI IRQ Line4	IRQ select for Line “z”	Auto Select

1. 5. System Configuration

System configurations of this context means:

1. During boot the BIOS checks for available hardware on the PCI bus, e.g. inserted controller or PCI cards. It recognizes the bus layout, scans all possible slots (sites) for devices, reads the type of the devices and their required amount of address space, defines and sets the base address of each device, lists all devices found and determines which interrupt line they are connected to.
2. After boot, the AQ−Driver uses the list of the BIOS, reads some additional registers of some devices and gains the necessary information to decide on which IPSO host model (IPSO 19” Unit or IPSO AQS) the software is coming up.

There is no active role for the user to influence this process other than changing the arrangement of inserted controllers and PCI cards. And normally this should not be necessary.

Modifying the arrangement changes the device number of each device and could alter the following situations:

- Which controllers can communicate with each other without having to go over a bridge. This is normally irrelevant.
- Which of the controllers share the same interrupt line with each other and with other devices, e.g. the Ethernet or the tty ports.
- To which priority level of the interrupt controller (there are 15) the interrupt of a device has been routed

The PCI bus contains 4 interrupt lines (INTw, INTx, INTy, INTz named in BIOS as Line1, Line2, Line3, Line4). The distribution of each controller slot interrupt to one of these lines is hard wired.

Table4: Interrupt distribution of the IPSO 19” Unit

	Controller Slot										
	1	2	3	4	5	6	7	8	9	PCI 1	PCI 2
	rctrl	tctrl	fctrl 1	fctrl 2	fctrl 3	fctrl 4	fctrl 5	fctrl 6	fctrl 7		
Line 1	x					x					
Line 2				x	x				x		
Line 3			x					x		x	
Line 4		x					x				x

The decision about routing of Line1/2/3/4 to any of the interrupt priority levels (IRQ) and sharing them with further interrupt sources is made by the BIOS, provided the BIOS parameter “PCI IRQ Line” is set to “Auto Select”. These routings can be checked in a LINUX shell with:

```
cat /proc/interrupts↵
```

We do not recommend replacing “Auto Select” by a special IRQ level.

	highest					Interrupt Priority Order									lowest
IRQ	0	1	8	9	10	11	12	13	14	15	3	4	5	6	7

Recognition of the host model

Recognition of the host model and the version of the installed controller will be performed by the AQ−Driver of LINUX in following steps:

1. Search for a PLX device with Subdevice−ID = 0x0200 and the IMBF version register implemented.

2. Read the content of the IMBF version register

3. If IMBF=0xFFFF or 0x0000, > IPSO 19” Unit

  1. Read the version register SLOT_BRDV on each Controller

  2. SLOT_BRDV=0xXFXX or 0xX0XX > 2MB external RAM on this Controller and DSP TMS320C6415
  SLOT_BRDV=0xX1XX > 16MB external RAM on this Controller and DSP TMS320C6415
  SLOT_BRDV=0xX2XX > 128MB external RAM on this Controller and DSP TMS320C6455

4. If IMBF= 0x0001, > IPSO AQS > IPSO AQS HOST including RxController with 2MB external RAM and DSP TMS320C6415

  1. Read the board version of IPSO AQS ACQ out of the T_BRDV register

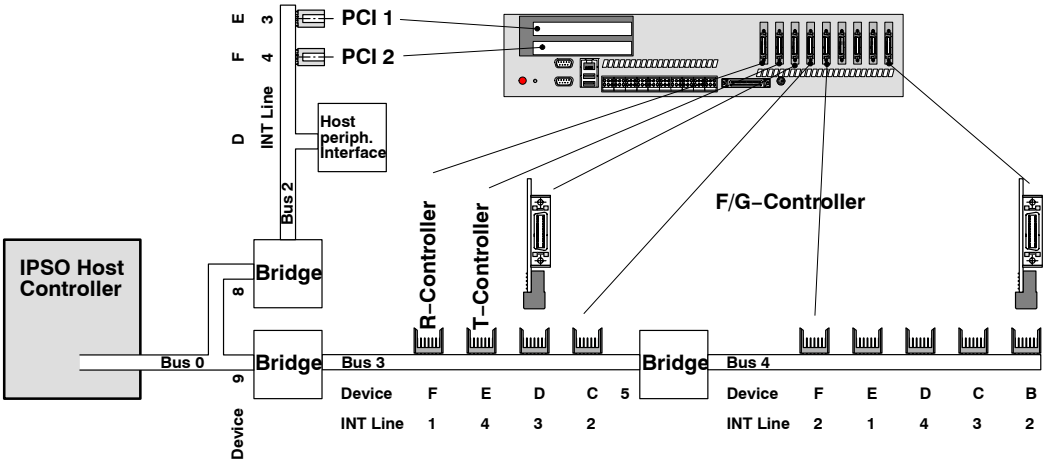
  2. T_BRDV=0x0000 > TxController with 16MB external RAM and DSP TMS320C6415 on IPSO AQS ACQ

  3. T_BRDV=0x0200 > TxController with 128MB external RAM and DSP TMS320C6455 on IPSO AQS ACQ

Table5: IPSO Versions

IMBF				T_BRDV				SLOT_BRDV				
variations			mo del	rev.		subrev.		slot	ver sn.	subv.		
F	F	F	F	not used								IPSO 19” Unit
0	0	0	0									
								X	F	X	X	TxController of IPSO 19” Unit ext RAM 2MB, DSP TMS320C6415
								X	0	X	X	
								X	1	X	X	TxController of IPSO 19” Unit ext RAM 16MB, DSP TMS320C6415
								X	2	X	X	TxController of IPSO 19” Unit ext RAM 128MB, DSP TMS320C6455
0	0	0	1					not used				IPSO AQS HOST, RxController with ext. RAM of 2MB, DSP TMS320C6415
				0	0	0	0					IPSO AQS ACQ, 5 TxController, ext. RAM 16MB, DSP TMS320C6415
				0	2	0	0					IPSO AQS ACQ, 5 TxController, ext. RAM 128MB, DSP TMS320C6455

Figure5: Host bus of the IPSO 19” Unit



Note: Inserting PCI cards with on−board bridges implies adding further bus segments which can in turn change the bus numbers!

Note: Inserting PCI cards with on−board bridges implies adding further bus segments which can in turn change the bus numbers!

Checking the Configuration

Modification of the system (by inserting or removing controllers or PCI cards) should always be followed by checking the system−recognized structure against the expected one. For instance, “has the system accurately recognized the number and the type of all inserted controllers?”.

Starting the ipsotest when logged in at the IPSO

root@IPSO:/opt/test>**ipsotest** ↵

returns a list of all recognized controllers, their bus and device numbers and their application specific utilization. Bus bridges, general PCI devices and interrupt routings are not shown.

A complete list of all PCI devices and interrupt routings is shown by typing

root@IPSO:/opt/test>**cat /proc/pci** ↵

Note: Devices on bus0 and bus1 are not application relevant!

1. 6. Power Supply

Checking Temperature and Voltages

Typing “mbmon –A” when logged in at the IPSO

root@IPSO:/opt/test>**mbmon –A**↵

returns something like the following values provided by voltage and temperature sensors:

On IPSO 19” Unit

Temp.=	82.0	80.5	80.5			(so far, June 2006, these values are not correct)
	below the Host Controller (PC–Module)	next to the Sequencer	next to the Voltage Regulators			Sensor location on the IPSO Base Board
Rot.=	0	0	0			Fan speed; not implemented
Vcore=	1.30	3.41				Core voltage of the Host Controller
Volt.=	3.41	5.03	12.46	–11.87	–5.25	Voltages of the Power Supply

Note: The –5Volt from Power Supply is not used!

Temp.=	82.0	80.5	80.5			(so far, these values are not correct)
	below the Host Controller (PC–Module)	next to the PCI connector	next to the RxController			Sensor location on IPSO AQS HOST Sensor location on IPSO AQS ACQ Sensor location on IPSO AQS HOST
Rot.=	0	0	0			Fan speed; not implemented
Vcore=	1.30	3.41				Core voltage of the Host Controller
Volt.=	3.41	5.03	12.46	–11.87	–5.25	Voltages of the Power Supply

Power Conditions on the IPSO 19” Unit

Currents and Voltages

Part–No.	Assembly		+5V	Σ +5 V	+3,3V	+12V	+5VSB	–12V
H12519	IMB	ETX 400Mhz + IMB		2,5 A	2,5 A	0,1	(1,8A)	0,1
		2 PCI Slot (25W)		10 A				
		70 RCP/30 mA		2,1A				

Part–No.	Assembly		+5V	Σ +5 V	+3,3V	+12V	+5VSB	–12V
H12538xx	TxController	1x(0,3+0,3)	0,6 A		0	0		0
		8x		4,8 A	0	0		0
H12532xx	RxController	1x	0,6 A	0,6 A	0	0		0
Current required from ATX Power Supply				20,0 A	2,5 A	0,1 A	(1,8A)	0,1 A
Power				108,25 W				
				109,45 W				
				118,15W				

Used Power Supply

Any ATX Power Supply with the same Formfactor would meet the functional requirements. But to keep the excellent quality and the mark of conformity valid, only the type

eNSP–300P–S20–00S

of the manufacturer Nipron has to be used for a replacement.

This installed type is ATX Version 2.03 compliant with 20–Pin Power Connector. Since –5Volt are not required, Power Supplies with 24–Pin Connectors (ATX12V Version 2.2) also meet the requirements but need an adapter.

The Nipron Power Supplies are said to run 24 hours a day during 10 years.

The Reliability Grade is “Factory Automation” instead of “Office Automation”.

The Fan can be replaced without disassembling either the Power Supply or the IPSO.

General Specifications			Continuous Output Specifications				
			+5V	+3.3V	+12V	+5VSB	–12V
Part–No.	87451		21 A	14 A	10A	1,5 A	0,8 A
Manufacturer	Nipron		125 W				
Type	eNSP–300P–S20–00S		185 W				
Continuous Power	200W		203 W				
Peak Power	300W						
Input	AC85~264V						
MTBF	100,000 hours						
Safety Standard	UL, CSA(c–UL), EN, CE						

2. IPSO Org

2. 1. Parts and Assemblies of the IPSO 19” Unit

IPSO CHASSIS UNIT KPL			**H9987**	
	IPSO 19” RD Case CPL		HZ14023	H1M14023A
		IPSO 19” RD Cover Pane	HZ14022	H4M14022A
		IPSO 19” RD Case Blind	HZ14028	H4M14028C
		Slot sheet for PC−Boards	HZ13609	H2M13609C
		IPSO Ventilator Unit	HZ13594	H3M13594A
		IPSO Mounting Kit	H9986	
	PC Power Supply PC 300W		87451	ENSP−300P−S20−00S
	IPSO Base Board		H12519	
		IPSO Base PCB	H12520	H3P2690E
		IPSO Base PCB	H12520F1	H3P2690F
		IPSO Base PCB	H12520F2	H3P2690G
		IPSO Base PCB	H12520F3	H3P2690H
		IPSO ETX Module	H12535	
		PC ETX Module VE−400	86739	
		Heatsink ETX modified	HZ13905	
		SDRAM 512MB SODIMM	87047	
	IPSO TX Board		H12538F2	
		IPSO TX PCB	H12537F4	H4P2760E
		IPSO 19” RD Cover Plate	HZ14029	H4M14029C
		IPSO 19” RD Circuit Lever, large	HZ14030	H2M14030A
		IPSO 19” RD Circuit Lever, short	HZ14031	H2M14031A
	IPSO RX Board		H12532	
		IPSO RX PCB	H12531F1	H3P2770C
	IPSO Display Board		H9975	
		IPSO Display PCB	H9974F1	H4P2790A
		IPSO Display Cable	HZ13591	H4D1391A
	IPSO PCI Board		H12524	
		IPSO PCI PCB	H12523F1	H4P2720B
	DPP1 Board		H12513F1	
		DPP1 PCB	H12551F3	H4P2820C
	PC 2CH RS232 PCI		O10394	EX−41052
	PC 4CH RS232 PCI		O10395	EX−41094

2. 2. LVDS Parts

IPSO LVDS Cable			
	48−Bit LVDS−Cable, 0,5m, Manufacturer 3M only	88201	14526−EZHB−050−0Q
	48−Bit LVDS−Cable, 1m, Manufacturer 3M only	86868	14526−EZHB−100−0Q
	48−Bit LVDS−Cable, 2m, Manufacturer 3M only	87925	14526−EZHB−200−0QC
	48−Bit LVDS−Cable, 3m, Manufacturer 3M only	87939	14526−EZHB−300−0QC
	48−Bit LVDS−Cable, 5m, Manufacturer 3M only	87940	14526−EZHB−500−0QC

2. 3. Test Accessories

IPSO Test Accessory			
	IPSO 19” trigger test cable	HZ14408	H3D14408A
	IPSO CPCI Board	H12521	
	IPSO CPCI PCB	H12522	H4P2710

2. 4. Introduction Status

IPSO 19” Unit

Part#	Name	Layout#	Modifi-cation	Prog file	Firm-ware
H12519	IPSO Base Board	H3P2690E	no	IPSO−IMB−2690E00	no
H9975	IPSO Display Board	H4P2790	no	n.a.	no
H12524	IPSO PCI Board				

Prog File

Modifications of the introduced assemblies

Jumper Setting

Firmware

Part#	Name	Layout#	Modifi-cation	Prog file	Firm-ware

Prog File

Modifications of the introduced assemblies

Jumper Setting

Firmware

2. 5. History of the IPSO 19” Unit

IPSO Base Board, H12519

EC No.	Date	Layout Number	Description of Bugs, Changes and Modifications	Ser.No.	EC–Level
ECH 3371	22.12.05	H3P2690E	Introduction of IPSO Base Board Prog file H12566 version IPSO–IMB–2690E00, no modifications, serial# below 0033 must not be officially used	0033	00
ECH 3375	17.01.06	H3P2690E	Modification of the IPSO Base Board due to the PCI PLX Bridge generating interrupt on the wrong PCI interrupt line: Needed: layout modification, Prog file H12566 version IPSO–IMB–2690E01	0065	01
ECH 3381	17.01.06	H3P2690F	Introduction of new IPSO Base Board Layout, removing some inconvenience for production, no functional modifications	0065	02
ECH 3430	04.04.06	H3P2690E/F	Modification of the IPSO Base Board (Layout version H3P2690E/F) due to incorrect Flash PROM wiring and power control logic tuning	0113	03
ECH 3431	27.06.06	H3P2690G	Introduction of new IPSO Base Board Layout version H3P2690G	0160	04
ECH 3439	18.08.06	H3P2690G	Modification of the IPSO Base Board Layout Version H3P2690G due to a JTAG programming failure of the configuration flash FPGA U34	0205	05
ECH 3471	20.10.06	H3P2690E/F/G	Modification of the IPSO Base Board when using JTAG SCAN Booster cable from Göpel	0295	06
ECH 3533	4.6.07	H3P2690H	Introduction of Layout version H3P2690H This layout supports modules with 5V– and 3.3V–PCI signaling. All former versions support only 5V–modules or 5V–tolerant modules, but not the “ETX VE4, P/N86739”	0600	07

IPSO–Tx, H12538F1, 2–MByte Memory, TMS320C6415

EC No.	Date	Layout Number	Description of Bugs, Changes and Modifications	Ser.No.	EC–Level
ECH 3405	22.02.06	H4P2760B	Introduction of controller IPSO–Tx; Prog file H12568:IPSO–TX–2760E00	0010	00
ECH 3406	23.02.06	H4P2760B	Addendum of 2 wires at LVDS interface to detect the type of the external connected devices. No change of Prog file.	0018	01
ECH 3407	23.02.06	H4P2760C	Introduction of a new layout containing former modifications. No change of Prog file.	0039	02
ECH 3408	24.02.06	H4P2760D	Adding termination resistors in FIFO data lines due to undershoot errors when inserted in slots 7, 8 or 9	0068	03

IPSO–Tx, H12538F2, 16–MByte Memory, TMS320C6415

EC No.	Date	Layout Number	Description of Bugs, Changes and Modifications	Ser.No.	EC–Level
3429	14.03.06	H4P2760E	Added Deskew function, initiated by a software command	0010	00

IPSO–Tx, H12538F3, 128–MByte Memory, TMS320C6455

EC No.	Date	Layout Number	Description of Bugs, Changes and Modifications	Ser.No.	EC–Level
					00
					01
					02
					03

IPSO–Rx, H12532F1, 2–MByte Memory, TMS320C6415

EC No.	Date	Layout Number	Description of Bugs, Changes and Modifications	Ser.No.	EC–Level
					00
					01
					02
					03

IPSO Display Board, H9975

EC No.	Date	Layout Number	Description of Bugs, Changes and Modifications	Ser.No.	EC–Level
3370	12.12.05	H4P2790	Introduction without modifications	0010	00
3372	13.1.06	H4P2790A	No power at pin 1 and 3 of LD1. The new layout connects them to LD1 pin 6	0157	01

IPSO PCI Board, H12524

EC No.	Date	Layout Number	Description of Bugs, Changes and Modifications	Ser.No.	EC–Level
3409	30.03.06	h4p2720a	Introduction of the PCI riser card for the IPSO 19” Unit	0010	00
3410	30.03.06	h4p2720a	Modifying the layout due to an INT wiring error for the INTA pin	0021	01
3411	30.03.06	h4p2720b	Introduction of a new layout with all former modifications	0165	02

IPSO Display Kabel, HZ13591

EC No.	Date	Layout Number	Description of Bugs, Changes and Modifications	Ser.No.	EC–Level

3. IPSO Host

In each IPSO system there is only one IPSO Host comprising of the IPSO Host Controller and its data and control buses and communication interfaces .

The IPSO Host Controller is an IBM compatible PC (ETX−Module) with all standard interfaces. Thus making access possible to the whole pool of standard hardware and software.

Operation

The Host Controller communicates with the TOPSPIN−PC and boots its operating system software (diskless LINUX) from the TOPSPIN−PC via Ethernet. It also communicates over its standard interfaces with the Rx− and the TxControllers and with peripheral devices.

Versions

Location	Name	Part#	EC#	FW#	Functional Increments	Software Req.
IPSO 19”	IPSO Base Board	H12519	00			
IPSO 19”	IPSO Base Board	H12519	01		PCI PLX−Int correction	
IPSO 19”	IPSO Base Board	H12519	02		No, new layout only	
IPSO 19”	IPSO Base Board	H12519	03		Correction of Flash−Prom wiring	
IPSO 19”	IPSO Base Board	H12519	04		No, new layout only	
IPSO 19”	IPSO Base Board	H12519	05		Due to JTAG programming	
IPSO 19”	IPSO Base Board	H12519	06		Due to JTAG programming	
IPSO 19”	IPSO Base Board	H12519	07		3.3V PCI signal level	

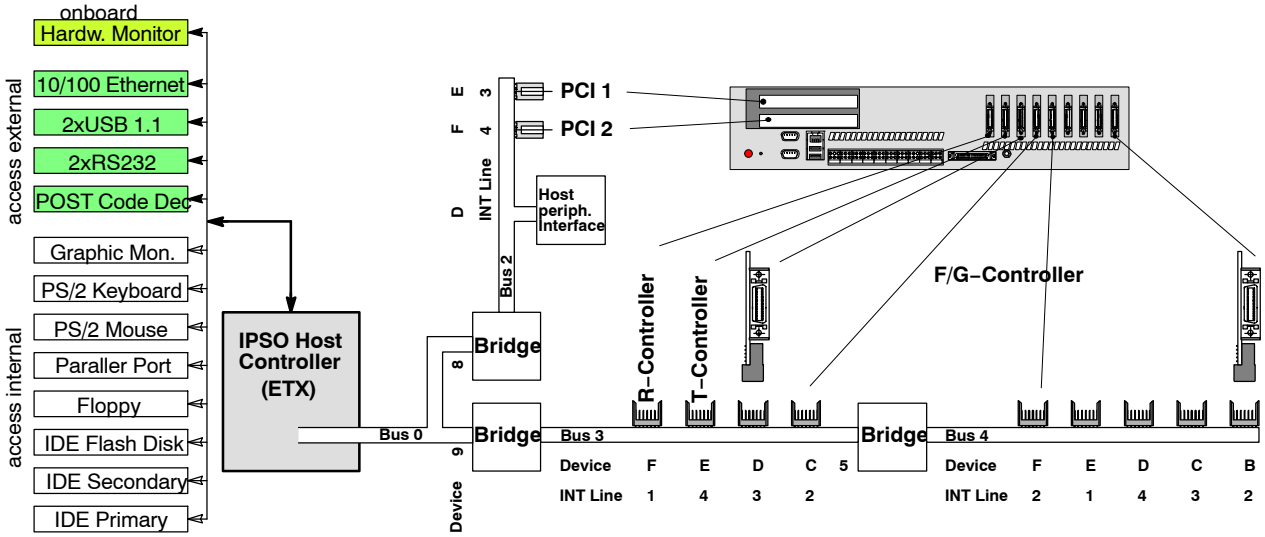
Features

- ETX Computer Module, up to 512 MByte SDRAM
- 20 Pin standard PC ATX Power connector
- 2 PS/2 6 pin header connectors for keyboard and mouse
- 2 PC standard IDE interface and 1 Floppy interface (shared with parallel port)
- Parallel port (shared with floppy)
- Flash Disk Interface (on secondary IDE side)
- 2 PC standard COM/RS232
- 2 USB ports
- VGA output
- 10/100−Mbit Ethernet
- PCI bus with 2 PCI−to−PCI bridge chips able to drive up to 9 devices (IPSO 19” System only)
- PCI bus with 2 PCI−to−PCI bridge chips, driving 6 devices (IPSO AQS System only)
- 2 standard PCI slots, 33MHz, 32 bit, 5V, each system

- Beeper
- Battery for the Real−Time−Clock
- Power On Self Test Decoder
- Temperature/Voltage hardware monitoring
- LED power and control indicators
- JTAG Test/Programing interface
- Coax outputs of the Realtime Control Pulses and Trigger inputs (IPSO 19 inch Unit only)
- BIS Bruker Identification System Flash PROM

Architecture

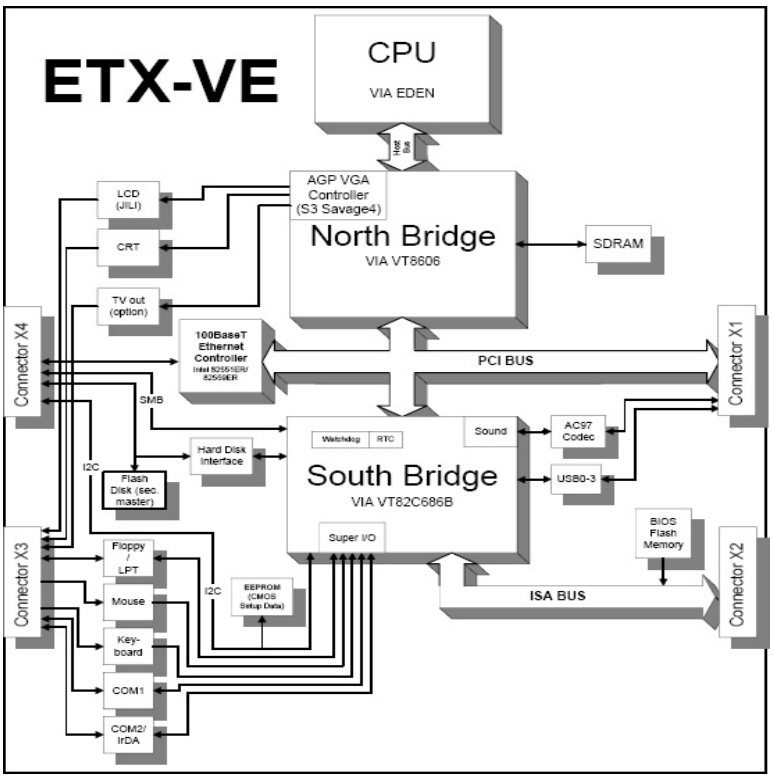
Figure6: IPSO Host of the “IPSO 19 inch Unit”

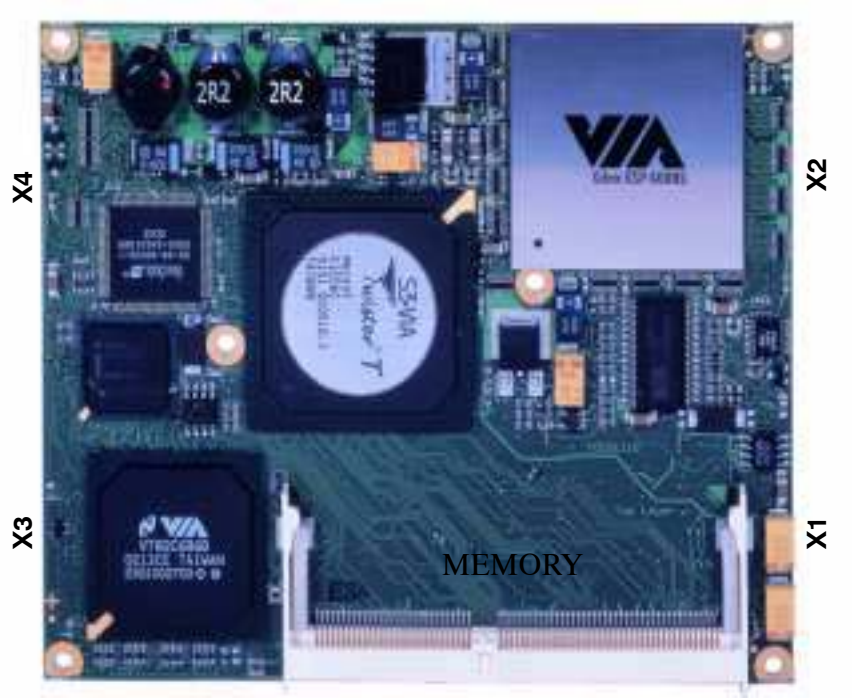


3. 1. IPSO Host Controller (ETX−Module)

The IPSO Host boards are designed to use the Embedded Extended Technology (ETX) modules as Host Controller. All ETX modules feature a standardized form factor and a standardized connector layout that carry a specified set of signals.

Figure7: Host Controller “ETX VE4” from Kontron





VGA
COM1+2
LPT/Floppy

X4

X2

ISA Bus

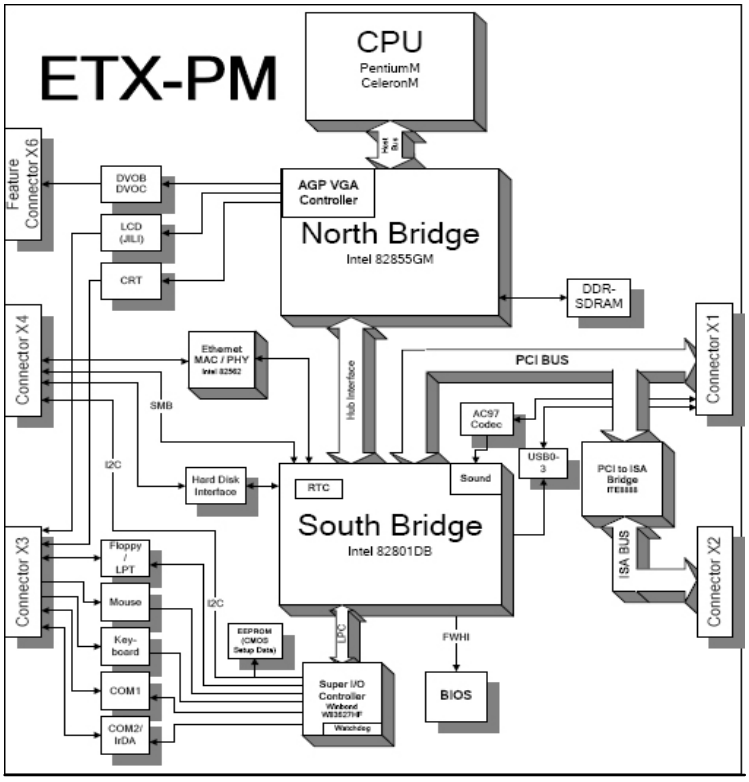
EIDE1+2
Ethernet 10/100 MBit/s
SMB Bus
I2C Bus
Power Management

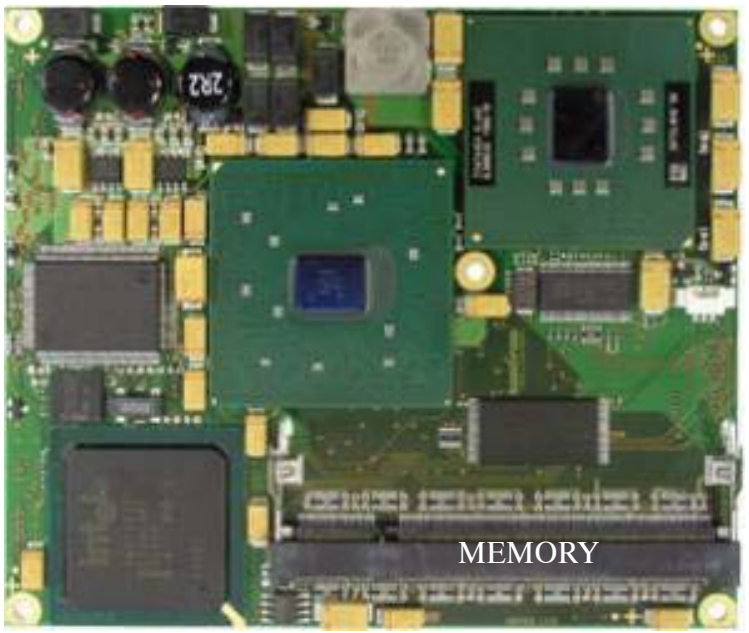
X3

X1

PCI Bus
4xUSB

Figure8: Host Controller “ETX PM” from Kontron





VGA
COM1+2
LPT/Floppy

X4

X2

ISA Bus

EIDE1+2
Ethernet 10/100 MBit/s
SMB Bus
I2C Bus
Power Management

X3

X1

PCI Bus
4xUSB

Environmental Specifications

All ETX Modules include a heat−spreader plate assembly on the top side. It is NOT a heat sink. The aluminum slugs and thermal pads on the underside of the heat−spreader assembly implement thermal interfaces between the heat spreader plate and the major heat−generating components on the ETX module. Under worst−case conditions, the cooling mechanism must maintain an ambient air and heat−spreader plate temperature of 60° C or less.

Models

Table6: Selected Types of ETX−Modules

	ETX−P1	ETX−VE4	ETX−PM
Revisions	Layout 121, BIOS Rev. 120	Layout 111, BIOS Rev. 110	BIOS Rev. 122
Manufacturer	Kontron		
Component:	Intel Platform using Ali Aladdin chip set V M1541, M1543C and Pentium MMX 266MHz processor	VIA Eden Platform using Twister chip set and ESP4000 400MHz processor	Intel Celeron M processor 800MHz, L2 cacheless
CPU Clock	266 MHz	400 MHz	C3 800 MHz
BIOS	Phoenix BIOS 4.0 Release 6.0, Kontron BIOS (MOD5R113) or (MOD9R111)	Phoenix BIOS 4.0 Release 6.0, Kontron BIOS (MOD9R111)	Phoenix BIOS 4.0 Release 6.01 Kontron BIOS (MOD9R122)
Used DRAM Modules	One SDRAM−SO−DIMM, 144−Pin, 3,3−Volt; 64MB, 128MB, 256MB	One SDRAM−SO−DIMM, 144−Pin, 3,3−Volt; 64MB, 128MB, 256MB, 512MB	One DDR−SO−DIMM, 200−Pin, 2,5−Volt; 256MB, 512MB, 1GB
Flash Disk on Module	16MB IDE Flash Disk as IDE2 master devices	no	no
Video Controller:	ATI Rage Mobility	Savage S4 (VT8606)	Intel 855GME
Ethernet Controller:	Intel 82559ER	Intel 82551ER	Intel 82562
USB Interfaces	0, 1, 2, 3;	0, 1, 2, 3;	0, 1, 2, 3
5V−Power, full	2,0 A	1,9 A	2,4 A
5V−Power, standby	1,4 A	1,4 A	1,28 A
5V−Power, suspend	0,9 A	0,8 A	0,31 A

Layout dependend conditions of choice

The following attributes are not covered by the ETX Standard. But the have to be defined in PCB layout and logic and therefor must not be ignored in selecting the ETX module.

Table7: IPSO Host, predefined ETX requirements

ETX Features which have to meet the Host layout	Necessary at “Bus 0” on IPSO Host
ADxx lines which are supported by the BIOS and ETX for usage on IPSO Host	AD19+AD20
Which REQ/GRANT pairs must be unused on the module and free to be used by the IPSO Host	REQ/GRANT_0 REQ/GRANT_1

BIOS

The module is equipped with a Phoenix BIOS, which is located in an onboard Flash EEPROM. The device has 8−bit access. Faster access (16 bit) is provided by the shadow RAM.

All IPSO Host Controllers are diskless and require some special BIOS settings:

- Remote Program Load ROM of onboard LAN Controller = Enabled and
- LAN boot priority of OS = At first position!

Table8: BIOS adjustments

Entry	Meaning	Phönix BIOS 4.0, Rel. 6.0	Phönix BIOS 4.0, Rel. 6.1
Kontron−Version		MOD9R111	MODRB122
Network boot support?		yes	yes
Display Control → Flat Panel Type		Auto Detect	Auto Detect
PNP OS Installed	PCI Bridge Support	no	no
Onboard LPT		enable	enable
Legacy USB Support	Global, Interface 0+1, extern	enable	enable
On Chip USB 2 Device	Interface 2+3, intern to Slot A+B	disable	disable
PCI Configuration → PCI IRQ Line1	IRQ select for Line “w”	Auto Select	Auto Select
PCI Configuration → PCI IRQ Line2	IRQ select for Line “x”	Auto Select	Auto Select
PCI Configuration → PCI IRQ Line3	IRQ select for Line “y”	Auto Select	Auto Select
PCI Configuration → PCI IRQ Line4	IRQ select for Line “z”	Auto Select	Auto Select

For more BIOS settings refer to the Appendix or the Kontron *”ETX−VE User’s Guide, Document Revision 2.0”* on *www.kontron.com* . The BIOS can be updated or restored by using a special procedure in−factory only.

3. 2. PCI Bus

Features

- Conforms to PCI Specification Revision 2.1
- 32−bit, 33−MHz
- Voltage range of signals is (0,...,5)V or (0,...,3,3)V dependent on bus number and configuration. Details below.
- Bus [00], [01] are used on ETX Module
- Bus [00] is continued off the module to IPSO Host without using a bridge on the module

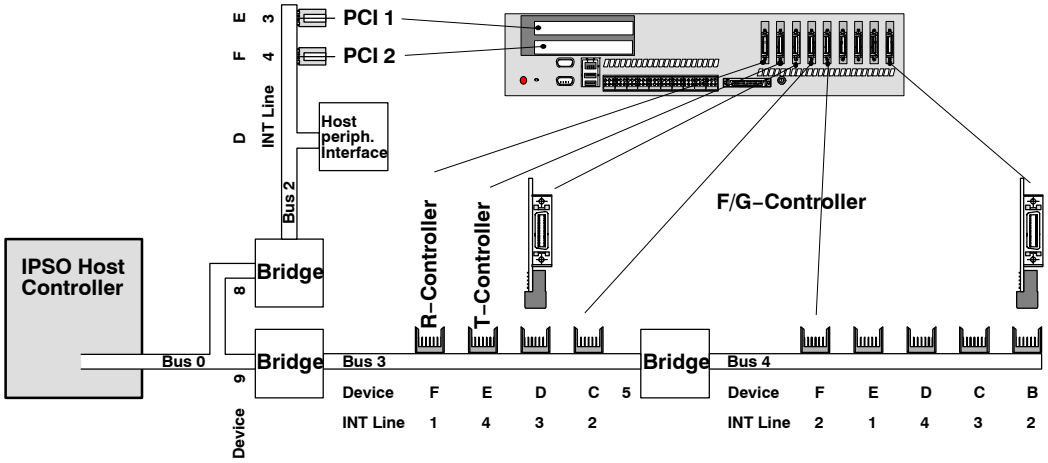
Structure of IPSO 19” Unit

Table9: Voltage level of signals in several bus segments

Designed levels of bus system [V]					Necessary levels of devices [V]			
Bus segment	Layout	max. send	tolerates	requires	Device	tolerates	requires	must send
Bus [00]	H3P2690E/F/G	5	5	3.3	VE4	5	5	3.3
	H3P2690H	3.3	5	3.3	PM	3.3	3.3	3.3

Designed levels of bus system [V]					Necessary levels of devices [V]			
Bus segment	Layout	max. send	tolerates	requires	Device	tolerates	requires	must send
Bus [02]	all	5	5	3.3	RS232	5	3.3/5	3.3
Bus [03]		3.3	5	3.3	Rx/TxCtrl	3.3	3.3	3.3
Bus [04]		3.3	5	3.3	TxCtrl	3.3	3.3	3.3

Figure9: Host bus of the IPSO 19” Unit



- At Bus [02]: The Host peripheral Interface (PLX, dev 0d.0) and two Standard PCI slots as devices 0e.0, 0f.0
- At Bus [03]: The PCI/PCI Bridge as device 05.0 and 4 Tx/Rx PCI slots as devices 0c.0, 0d.0, 0e.0, 0f.0
- At Bus [04]: 5 Tx PCI slots as devices 0b.0, 0c.0, 0d.0, 0e.0, 0f.0

The LINUX command `lspci -t` prints the following tree picture of that structure:

```
-[00]-+-00.0
      +-01.0-[01]----00.0
      +-02.0
      +-07.0
      +-07.1
      +-07.2
      +-07.4
      +-07.5
      +-08.0-[02]----0d.0
      \-09.0-[03-04]--+-05.0-[04]--
```

Comment: [00] is a PCI Bus name
00.0 is a PCI Device name

Note: Inserting PCI cards with on−board bridges implies adding further bus segments which can in turn change the bus numbers!

Device dependend allocation of Signals

Table10: PCI device allocation of special signals in the IPSO 19” Unit

Bus	Dev	Slot	Pin to Signal			
			IDSEL	CLK	INTA at line	REQ/GNT#
0	8	Slot 1 of ETX Bridge→ Bus2	AD19	PCICLK1	–	0
0	9	Slot 2 of ETX Bridge→ Bus3	AD20	PCICLK2	–	1
2	D	Host peripheral Interface (PLX)	B_AD29	B_CLK2	x	slave device only
	E	Stand. Slot PCI1	B_AD30	B_CLK0	y	B_REQ/B_GNT0
	F	Stand. Slot PCI2	B_AD31	B_CLK1	z	B_REQ/B_GNT1
3	5	Bridge→ Bus4	S_AD21	S_CLK4	–	REQ/GNT2
3	F	rcon R	S_AD31	S_CLK0	w	S_REQ/S_GNT0
3	E	tcon A	S_AD30	S_CLK1	z	S_REQ/S_GNT1
3	D	con B	S_AD29	S_CLK2	y	S_REQ/S_GNT2
3	C	con C	S_AD28	S_CLK3	x	S_REQ/S_GNT3
4	F	con D	A_AD31	A_CLK0	x	A_REQ/A_GNT0
4	E	con E	A_AD30	A_CLK1	w	A_REQ/A_GNT1
4	D	con F	A_AD29	A_CLK2	z	A_REQ/A_GNT2
4	C	con G	A_AD28	A_CLK3	y	A_REQ/A_GNT3
4	B	con H	A_AD27	A_CLK4	x	A_REQ/A_GNT4

PCI Bus Signals

Standard PCI Connector

The signal assignment to most of the connector pins is fixed as in the following table by the “PCI Local Bus Specification”. The assignment to some pins depends on the device address behind of that connector or the signal level environment. They are marked as follows:

Green shadowed pins: The device address (INTi, IDSEL) or the request priority (REQ, GNT) dictate the assigned signal

Blue hatched vertical: The level of the signal voltage (5 or 3.3 Volt) requires that voltage at all of these pins.

Red hatched diagonal: All of these pins are reserved for future use. They must not be used at connectors for standard PCI cards.

Table11: Signals at the Standard PCI Connector, 32 bit, 5 or 3.3 Volt

PCI Standard Connector 5V / 3.3V Environment								
Pin	Row B	Pin	Row A		Pin	Row B	Pin	Row A
1	–12V	1	TRST		32	AD17	32	AD16
2	TCK	2	12V		33	CBE2#	33	3,3V
3	GND	3	TMS		34	GND	34	FRAME#
4	TDO	4	TDI		35	IRDY#	35	GND

PCI Standard Connector 5V / 3.3V Environment								
Pin	Row B	Pin	Row A		Pin	Row B	Pin	Row A
5	VCC	5	VCC		36	3,3V	36	TRDY#
6	VCC	6	INTA#		37	DEVSEL#	37	GND
7	INTB#	7	INTC#		38	GND	38	STOP#
8	INTD#	8	VCC		39	LOCK#	39	3,3V
9	PRSNT1	9	res		40	PERR#	40	SDONE
10	res	10	IO–5/3V		41	3,3V	41	SB0#
11	PRSNT2	11	res		42	SERR#	42	GND
12	GND	12	GND		43	3,3V	43	PAR
13	GND	13	GND		44	CBE1#	44	AD15
14	res	14	res		45	AD14	45	3,3V
15	GND	15	PCIRST#		46	GND	46	AD13
16	PCICLK	16	IO–5/3V		47	AD12	47	AD11
17	GND	17	GNT#		48	AD10	48	GND
18	REQ#	18	GND		49	GND	49	AD9
19	IO–5/3V	19	res		50	free	50	free
20	AD31	20	AD30		51	free	51	free
21	AD29	21	3,3V		52	AD8	52	CBE0#
22	GND	22	AD28		53	AD7	53	3,3V
23	AD27	23	AD26		54	3,3V	54	AD6
24	AD25	24	GND		55	AD5	55	AD4
25	3,3V	25	AD24		56	AD3	56	GND
26	CBE3#	26	IDSEL		57	GND	57	AD2
27	AD23	27	3,3V		58	AD1	58	AD0
28	GND	28	AD22		59	IO–5/3V	59	IO–5/3V
29	AD21	29	AD20		60	ACK64= PULLUP0	60	REQ64= PULLUP1
30	AD19	30	GND		61	VCC	61	VCC
31	3,3V	31	AD18		62	VCC	62	VCC

IPSO 19” Unit: Rx/Tx–Connectors at Bus3 and 4; IPSO–Rx and IPSO–Tx

There are 9 CPCI slots of it 4 at the bus [03] and 5 at the bus [04]. The signal assignment to most of the Compact PCI connector pins is fixed as in the following table and very nearly to “CPCI Local Bus Specification”. For details slot interrupt routing show Table: INTA wiring on PC–Module “ETX–P1” and IPSO Host of the IPSO 19inch Unit.

Table12: Pin destinations of signals at the reserved pins of ST10–ST13

Different destination at bus [03] of ST10,...,ST13 connectors					
Pin	Row A	Row B	Row C	Row D	Row E
1	+5,0V		TRSTB_A*	USBPWR_R/A–C	+5,0V
2	TCKB_A	+5,0V	TMSB_A	TDOB	TDIB_A
3	INTA_R/A–C*	INTB_R/A–C*	INTC_R/A–C*	+5,0V	INTD_R/A–C*
4	+2,5V	GND	+3,3V	+1,4V_D	+1,4V_D
5	+2,5V	BRSVP1B5	S_RST*	GND	S_GNT0–3*
6	S_REQ0–3*	GND	+3,3V	S_CLK0–3	S_AD31
7	S_AD30	S_AD29	S_AD28	GND	S_AD27
8	S_AD26	GND	+3,3V	S_AD25	S_AD24
9	S_CBE3*	S_IDSEL_R/A–C*	S_AD23	GND	S_AD22
10	S_AD21	GND	+3,3V	S_AD20	S_AD19
11	S_AD18	S_AD17	S_AD16	GND	S_CBE2*

Different destination at bus [03] of ST10,...,ST13 connectors					
Pin	**Row A**	**Row B**	**Row C**	**Row D**	**Row E**
15	+3,3V	S_FRAME*	S_IRDY*	GND	S_TRDY*
16	S_DEVSEL*	GND	+3,3V	S_STOP*	S_LOCK*
17	+3,3V	S_SDONE*	S_SBO*	GND	S_PERR*
18	S_SERR*	GND	+3,3V	S_PAR*	S_CBE1*
19	+3,3V	S_AD15	S_AD14	GND	S_AD13
20	S_AD12	GND	+3,3V	S_AD11	S_AD10
21	+3,3V	S_AD9	S_AD8	S_M66EN	S_CBE0*
22	S_AD7	GND	+3,3V	S_AD6	S_AD5
23	+3,3V	S_AD4	S_AD3	+5,0V	S_AD2
24	S_AD1	+5,0V	+3,3V	S_AD0	S_ACK64*
25	+5,0V	+USB_R/A-C	-USB_R/A-C	+3,3V	+5,0V

Table13: Pin destinations of signals at the reserved pins of ST14–ST18

Different destination at bus [04] of ST14–18 connectors					
Pin	**Row A**	**Row B**	**Row C**	**Row D**	**Row E**
1	+5,0V		TRSTB_B*	USBPWR_D-H	+5,0V
2	TCKB_B	+5,0V	TMSB_B	TDOB	TDIB_B
3	INTA_D-H*	INTB_D-H*	INTC_D-H*	+5,0V	INTD_D-H*
4	+2,5V	GND	+3,3V	+1,4V_D	+1,4V_D
5	+2,5V	BRSVP1B5	A_RST*	GND	A_GNT0-4*
6	A_REQ0-4*	GND	+3,3V	A_CLK0-4	A_AD31
7	A_AD30	A_AD29	A_AD28	GND	A_AD27
8	A_AD26	GND	+3,3V	A_AD25	A_AD24
9	A_CBE3*	A_IDSEL_D-H*	A_AD23	GND	A_AD22
10	A_AD21	GND	+3,3V	A_AD20	A_AD19
11	A_AD18	A_AD17	A_AD16	GND	A_CBE2*
15	+3,3V	A_FRAME*	A_IRDY*	GND	A_TRDY*
16	A_DEVSEL*	GND	+3,3V	A_STOP*	A_LOCK*
17	+3,3V	A_SDONE*	A_SBO*	GND	A_PERR*
18	A_SERR*	GND	+3,3V	A_PAR*	A_CBE1*
19	+3,3V	A_AD15	A_AD14	GND	A_AD13
20	A_AD12	GND	+3,3V	A_AD11	A_AD10
21	+3,3V	A_AD9	A_AD8	A_M66EN	A_CBE0*
22	A_AD7	GND	+3,3V	A_AD6	A_AD5
23	+3,3V	A_AD4	A_AD3	+5,0V	A_AD2
24	A_AD1	+5,0V	+3,3V	A_AD0	A_ACK64*
25	+5,0V	+USB_D-H	-USB_D-H	+3,3V	+5,0V

Adapting the standard slots “PCI 1” and “PCI 2” to PCI Bus “2”

IPSO 19inch Unit: The IPSO PCI Board (H12524)

The IPSO PCI Board is attached via the PCI bus connector ST44. Due to the fact that its reserved pins had to been used for the additional signals dedicated to the standard slots PCI1 and PCI2, ST44 is not qualified for insertion of any Standard PCI Card.

ST44 is dedicated for the insertion of H12524 only!

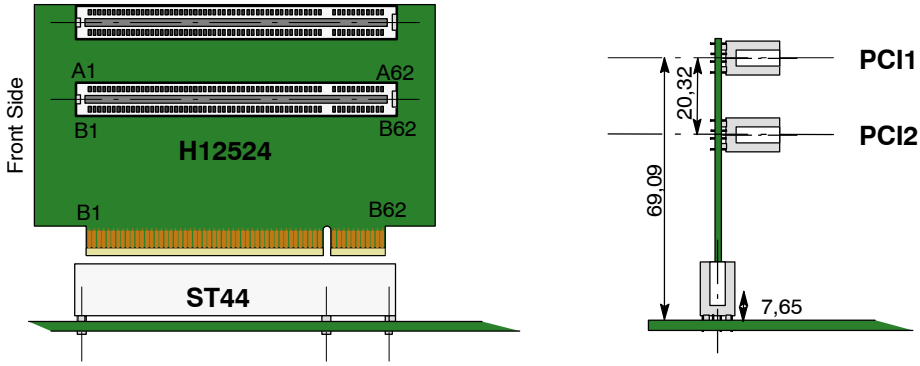
The following table shows only the anomalous signal wiring between ST44 and PCI1 respective PCI2

Table14: Pin destinations of signals at the reserved pins of ST44

ST44		Different destination at		ST44		Different destination at	
Pin	Row B	PCI 1	PCI 2	Pin	Row A	PCI 1	PCI 2
1	–12V			1	TRST		
2	TCK			2	12V		
3	GND			3	TMS		
4	TDO			4	TDI		
5	VCC			5	VCC		
6	VCC			6	y	A6	B8
7	z	B7	A6	7	w	A7	B7
8	x	B8	A7	8	VCC		
9	PRSNT1			9	TDO	B4	B4
10	REQ1		B18	10	IO–5/3V		
11	PRSNT2			11	res		
12	GND			12	GND		
13	GND			13	GND		
14	CLK1		B16	14	GNT1		A17
15	GND			15	PCIRST#		
16	CLK0	B16		16	IO–5/3V		
17	GND			17	GNT0	A17	
18	REQ0	B18		18	GND		
19	IO–5/3V			19	res		
20	AD31			20	AD30		
21	AD29			21	3,3V		
22	GND			22	AD28		
23	AD27			23	AD26		
24	AD25			24	GND		
25	3,3V			25	AD24		
26	CBE3#			26	IDSEL		
27	AD23			27	3,3V		
28	GND			28	AD22		
29	AD21			29	AD20		
30	AD19			30	GND		
31	3,3V			31	AD18		

All other pins are connected at PCI1 and 2 to the same destination pin as at ST44.

Figure10: Adapter “IPSO PCI Board”, H12524



PCI Devices

Outside the ETX−Module, there are only two different PCI interface devices which are used numerously:

- The DSP TMS320C6415 with PCI interface from TI
- The PCI target controller “PCI9030” from “PLX Technology” as Host Peripheral Interface

The PCI Interface of DSP “C6415”

Address Mapping

Table15: Access ranges of the DSP C6415

External Bus Access				To DSP internal			
Space	**Access type**	**Address**		**Address**	**Range**	**Destination**	
Memory	prefetchable Memory	Bit [31::22]	<Base0>	<DSPP>	The whole memory range is accessible through this 4 Mbyte Window		
		Bit [21::0]	AD [21::0]				
					64 MB	0x600−63F	EMIFB 0
					64 MB	0x640−67F	EMIFB 1
					64 MB	0x680−6BF	EMIFB 2
					64 MB	0x6C0−6FF	EMIFB 3
					256 MB	0x800−8FF	EMIFA 0: MEM
					256 MB	0x900−9FF	EMIFA 1: FIFO
					256 MB	0xA00−AFF	EMIFA 2
					256 MB	0xB00−BFF	EMIFA 3
8 MB Reg. Memory	Single Access non−prefetchable Register	Bit [31::23]	<Base1>	$[0000\ 0001\ 1]_2$	Fixed 8 Mbyte Register Window: 0x0180... bis 0x01FF...		
						0x01C00000	11 Register
		Bit [22::0]	AD [22::0]			0x01C20000	3 Register
						0x01C1FFF0	HSR reg
						0x01C1FFF4	HDCR reg
						0x01C1FFF8	DSPP reg
I/O	Single Access non−prefetchable Register	Bit [31::4]	<Base2>		I/O Space		HSR HDCR DSPP
		Bit [3::0]	AD [3::0]				

The Host Peripheral Interface (HPI)

The Host Peripheral Interface uses the PCI Target bridge PLX 9030. This device connects the Local Bus of the “Host Peripheral Interface” to the PCI Bus and supports read and write accesses from PCI to Local Bus.

The Local Bus of the HPI is connected to following devices:

- IPSO Configuration Register, containing hardware information
- FLASH PROM, containing BIS information (BIS=Bruker Information System)

- JTAG Interface, making the JTAG chain accessible to the software and allowing reprogramming of the hardware logic by the system itself.

Furthermore to the HPI, the PLX 9030 is used at the PCI Bus of IPSO on the PCI Standard Devices “IPSO DPP1” and “IPSO DPP2”. The Configuration Space of these 3 devices can be recognized by the different content of their “Subsystem ID Registers”. The different Configuration Spaces of the PLX 9030 are stored in 4−Kbyte Serial EEPROMs of type “93CS66L”. These PROMs are read by the PLX 9030 when the PCI reset is deasserted. The PROM contents can be created using the “PLXMon” software and stored using the JTAG−Tool of GOEBEL.

The contents of the PCI configuration space registers can be checked in the print out of the command `lspci -x`, typed in a LINUX shell.

Table16: Configuration Space of the “Host Peripheral Interface”, PLX

Hex Addr “xy”	x0	x1	x2	x3	x4	x5	x6	x7	x8	x9	xA	xB	xC	xD	xE	xF
0y	b5	10	30	90	03	01	90	02	0a	00	80	06	08	00	00	00
1y	00	00	26	e8	01	90	00	00	00	00	30	e8	00	00	22	e8
2y	00	00	21	e8	00	00	20	e8	00	00	00	00	00	00	00	02
3y	00	00	00	00	40	00	00	00	00	00	00	00	0a	01	00	00

Table17: Meaning and 4−byte data of the HPI Configuration space

HPI PCI Configuration Registers					
Offset	Register	Value	Offset	Register	Value
0x00	Dev/Vendor ID	0x903010b5	0x3c	Int. Pin/Line	0x000001ff
0x04	PCI/Cmd Status	0x00100000	0x40	PM Capabilities	0x48014801
0x08	Class Code/Rev	0x0680000a	0x44	PM Cntrl/Status	0x00000000
0x2c	Subsystem ID/Subvendor ID	0x02000000	0x48	HS Cntrl/NCP	0x00004c06
0x34	New Cap Pointer	0x00000040	0x4c	VPD Cntrl/NCP	0x00000003

The 16−bit Subsystem ID is stored at addresses 0x2F and 0x2E. The Subsystem ID for IPSO PCI devices using the PLX 9030 is:

Table18: PLX Subsystem ID of IPSO devices

	IPSO DPP1	IPSO DPP2	IPSO Host Port Interface
PLX Subsystem ID	0x0100	0x0101	0x0200

This is default PLX EEPROM register set (**IMB00AB05.dat**) after power−on condition.

Table19: IPSO19”/AQS PLX Memory Space Register

PLX Memory Space0 Registers		
Offset	Register	Value
0x28	Descriptor	0x00400002
0x00	Range	0x00ff00000
0x14	Remap	0x00000001

PLX Memory Space1 Registers		
Offset	Register	Value
0x2c	Descriptor	0x50400040
0x04	Range	0x00ff00000
0x18	Remap	0x00000001

PLX Memory Space2 Registers		
Offset	Register	Value
0x30	Descriptor	0x50400040
0x08	Range	0x00ff00000
0x1c	Remap	0x00000001

PLX Memory Space3 Registers		
Offset	**Register**	**Value**
0x34	Descriptor	0x50400040
0x0c	Range	0x00ff00000
0x20	Remap	0x00000001

Table20: IPSO19”/AQS PLX Chip Select Register

PLX Chip Select Registers		
Offset	**Register**	**Value**
0x3c	CS0 Base	0x00000000
0x40	CS1 Base	0x00000000
0x44	CS2 Base	0x00000000
0x48	CS3 Base	0x00000000

Table21: IPSO19”/AQS PLX Control Register

PLX Control Registers		
Offset	**Register**	**Value**
0x4c	Int Cntrl/St	0x00300040
0x50	Eep/trgt Ctrl	0x00780000
0x54	GP I/O	0x00249000
0x70	PM Select	0x00000000
0x74	PM Scale	0x00000000

Table22: IPSO19”/AQS PLX Expansion ROM Register

PLX Expansion ROM Registers		
Offset	**Register**	**Value**
0x38	Descriptor	0x00000000
0x10	Range	0x00000000
0x24	Remap	0x00010000

Hardware Configuration Register

The Configuration Register indicates configuration of IPSO boards. It is a fix wired 16 Bit register mapped in Space 0 of the PLX9030 .

Table23: IPSO hardware configuration register

IPSO hardware configuration register	
IPSO 19”	b 0000 0000 0000 0000
IPSO AQS	b 0000 0000 0000 0001

Bruker Identification System Flash PROM

The Flash PROM is mapped in Space 3 of the PLX9030 device. It contains following informations and can be read with the “IPSO Web Administration Tool”:

- Device type
- Part number
- Serial number

- EC Level
- Name
- Production date
- Firmware version
- Flash write count

Table24: IPSO Flash Signal description

Signal	Description
Flash_CS*	Flash Chip Select. When asserted low, the flash PROM is forced to enter a read or write cycles.
Flash_WR*	Flash Write Signal. When asserted low, the flash PROM is forced to write access.
Flash_OE*	Flash Output Enable Signal. When asserted low, the flash PROM is forced to read access. Is driven low automatically when the PCI9030 owns the local bus.

PLX JTAG Interface

The JTAG Interface is used for the IPSO Firmware Update and accessible by PLX General Purpose I/O Port (for more details show *IPSO Firmware Update Manual*).

Figure11: PLX Gen. Purpose I/O Control and JTAG Interface (GPIO: 54h)

Bit	Description	Read/Write	Value after Reset	Initial value	Signal Name	I/O
0	GPIO0	Yes	0	0		
1	GPIO0 Direction	Yes	0	1		
2	GPIO0 Data	Yes	0	0		Output n/u
3	GPIO1	Yes	0	0		
4	GPIO1 Direction	Yes	0	1		
5	GPIO1 Data	Yes	0	1/0	TRST*	JTAG Output
6	GPIO2	Yes	0	0		
7	GPIO2 Direction	Yes	0	1		
8	GPIO2 Data	Yes	0	0		Output n/u
9	GPIO3	Yes	0	1		
10	GPIO3 Direction	Yes	0	1		
11	GPIO3 Data	Yes	0	1/0	Flash_CS*	Output
12	GPIO4	Yes	1	0		
13	GPIO4 Direction	Yes	0	1		
14	GPIO4 Data	Yes	0	1/0	Flash_WE*	Output
15	GPIO5	Yes	1	0		
16	GPIO5 Direction	Yes	0	1		
17	GPIO5 Data	Yes	0	1/0	TDI	JTAG Output
18	GPIO6	Yes	1	0		
19	GPIO6 Direction	Yes	0	1		
20	GPIO6 Data	Yes	0	1/0	TMS	JTAG Output
21	GPIO7	Yes	1	0		
22	GPIO7 Direction	Yes	0	1		

Bit	Description	Read/Write	Value after Reset	Initial value	Signal Name	I/O
23	GPIO7 Data	Yes	0	1/0	TCK	JTAG Output
24	Reserved	Yes	0	0		
25	GPIO8 Direc-tion	Yes	0	0		
26	GPIO8 Data	Yes	0	1/0	TDO	JTAG Input
27–31	Reserved	Yes	0h	0h		

Note: GPIO pins configured as output are driven only when the PCI9030 owns the local bus.
– **(*)** indicates low active signal
– **(1/0)** indicates high or low transaction

Table25: JTAG signal description

Signal	Description
TRST*	JTAG TAP reset. When asserted low, the TAP controller is asynchronously forced to enter a reset state, which in turn asynchronously initializes other test logic. An unterminated trst_l produces the same result as if it were driven high. The TAP controller must be reset before the chip can function in normal operating mode.
TMS	JTAG test mode select. Signal tms causes state transitions in the test access port (TAP) controller. An undriven tms has the same result as if it were driven high.
TCK	JTAG boundary–scan clock controlling the JTAG logic.
TDI	JTAG serial data in. Signal tdi is the serial input through which JTAG instructions and test data enter the JTAG interface. The new data on tdi is sampled on the rising edge of tck. An unterminated tdi produces the same result as if tdi were driven high.
TD0	JTAG serial data out. Signal tdo is the serial output through which test instructions and data from the test logic.

PCI Interrupt Routing

The BIOS checks during the configuration phase of the boot process the bus structure and the addresses of the devices found. Based on these results it deduced the interrupt wiring and an swered the question, “to which interrupt line of `w, x, y` or `z` is a device connected to with its interrupt pin “A” (INTA) (“B”, “C” or “D” if implemented). With this knowledge, the BIOS configures the interrupt router and defines the IRQ level of any device in the system.

Connection of PCI Devices to the INT–Lines

The following table indicates which PCI interrupt line out of “w, x, y and z” is connected to pin INTA of each PCI device.

Table26: INTA wiring on “ETX–P1” and IPSO Host of the IPSO–19U

ETX–P1 INT Routing (on module)					Circular INT Routing (on Host)								
INT line	Device on Bus1		Device on Bus0		INT line	Device on Bus0		Device on Bus2		Device on Bus3		Device on Bus4	
			0	Host–Bridge→ Bus0	w			0					
w	0	VGA	1	PCI–Bridge→ Bus1	x			1		0			
z	1		2	ETH	y			2		1		0	
w	2		3	Audio	z			3		2		1	
	3		4		w			4		3		2	
	4		5		x			5		4		3	

ETX–P1 INT Routing (on module)					Circular INT Routing (on Host)								
INT line	**Device on Bus1**		**Device on Bus0**		**INT line**	**Device on Bus0**		**Device on Bus2**		**Device on Bus3**		**Device on Bus4**	
	5		6		y			6		5	PCI–Bridge→ Bus4	4	
	6		7	ISA–Bridge	z			7		6		5	
	7				w	8	Slot1: PCI–Bridge→ Bus2	8		7		6	
	8				x	9	Slot2: PCI–Bridge→ Bus3	9		8		7	
	9				y	A	Slot3:free	A		9		8	
	A				z	B	Slot4:free	B		A		9	
	B		C		w			C		B		A	
	C		D		x			D		C	Slot C: FCtrl2	B	Slot H: FCtrl7
	D		E		y			E	PCI–Slot 1	D	Slot B: FCtrl1	C	Slot G: FCtrl6
	E		F		z			F	PCI–Slot 2	E	Slot A: TCtrl	D	Slot F: FCtrl5
	F		10	IDE	w					F	Slot R: RCtrl	E	Slot E: FCtrl4
			11		x							F	Slot D: FCtrl3
			12		y								
			13		z								
			14		w								

Routing of the PCI INT−Lines to prioritized IRQs of the X86−architecture

Table27: INT line assignment

Priority	PC cascaded INT Controller		ETX on−module devices	Routable, dependend on BIOS and equipment		
				ETX−P1; Phönix BIOS	ETX−VE4; Phönix BIOS	ETX−PM; Phönix BIOS
highest	IRQ 0		Timer			
	IRQ 1		Keyboard			
	IRQ2	IRQ 8	RTC			
		IRQ 9	ETH, VGA, USB	PCI INTw: RCtrl, FCtrl4		
		IRQ 10		PCI INTy: FCtrl1, FCtrl6		
		IRQ 11		PCI INTz: TCtrl, FCtrl5		
		IRQ 12	PS/2 Mouse			
		IRQ 13	FPU			
		IRQ 14	IDE1			
		IRQ 15	IDE2			
	IRQ 3		COM 2			
	IRQ 4		COM 1			
	IRQ 5		Audio	PCI INTx: FCtrl2, FCtrl3, FCtrl7		
	IRQ 6		Floppy			
lowest	IRQ 7		Parallel Port			

3. 3. System Management Bus (SMB)

The System Management Bus (SMBus) is a two−wire interface through which various system component chips can communicate with each other and with the rest of the system. It is based on the principles of operation of I2C*.

Function

The Winbond IC W83782D stimultaneously monitor following temperatures and voltages:

- Temperature of ETX Module
- Temperature between Power regulators (IPSO 19” Host only)
- Temperature of Stratix (IPSO 19” Host only)
- Temperature of ACQ DSPs (IPSO AQS Host only)
- 3.3V, 5.0V, 5V_SB,−5V,−12V,12V,VBat

Structure

Devices

Each device that uses the System Management Bus has a unique address called the *Slave Address.* The following slave addresses are reserved by I2C specification and thus cannot be used by any devices of the devices on this particular interface:

Table28: SMB Device identification – Slave Address

Slave Address Bits 7–1	R/W bit Bit 0	Description
0000 000	0	General Call Address
0000 000	1	Start Byte
0000 001	X	CBUS Address
0000 010	X	Address reserved for different bus format
0000 011	X	Reserved for future use
0000 1XX	X	Reserved for future use
1111 0XX	X	10 Bit Slave addressing
1111 1XX	X	Reserved for future use

In addition the following address are reserved for the System Management Bus:

Table29: SMB reserved slave Address

Slave Address	Description
0001 000	SMB Host
0001 100	SMB Alert Response Address
1100 001	SMB Device Default Address
0101 000	reserved for Access.bus host
0110 111	reserved for Access.bus default address
1001 1XX	Unrestricted address

Table30: ETX–VE reserved SMB slave address

Slave Address Bits 7–1	SMB Device	Description
0001 001	SMART_CHANGER	Not to be used with any SM Bus device except a charger
0001 010	SMART_SELECTOR	Not to be used with any SM Bus device except a selector
0001 011	SMART_BATTERY	Not to be used with any SM Bus device except a battery
1001 110	Temperature Sensor (LM84)	Onboard temperature sensor. Do not connect off board.?
1010 000	SPD	SDRAM EEPROM
1101 001	Clock generator	Do not use under any circum-stances.
0101 101	Reserved	Do not use

Table31: IPSO reserved SMB slave address

Slave Address Bits 7–0	SMB Device	Description
00101 010	IPSO WINBOND	Temperature/Voltage Control

Table32: IPSO Winbond SMB first serial slave address

Slave Address 7–3	Bit 2/Pin45	Bit 1/Pin46	Bit 0/Pin 47
00101	0	1	0

Note: The Winbond IC W83782D Pin 43 must be set to high.

3. 4. Reset and Power–ON

There are 3 sources of reset functions with different effects:

- The Power–ON/OFF button
- The Reset button
- The Warm–Reset–Bit in the HSR register

Reset Logic

Figure12: Effect of Reset Buttons

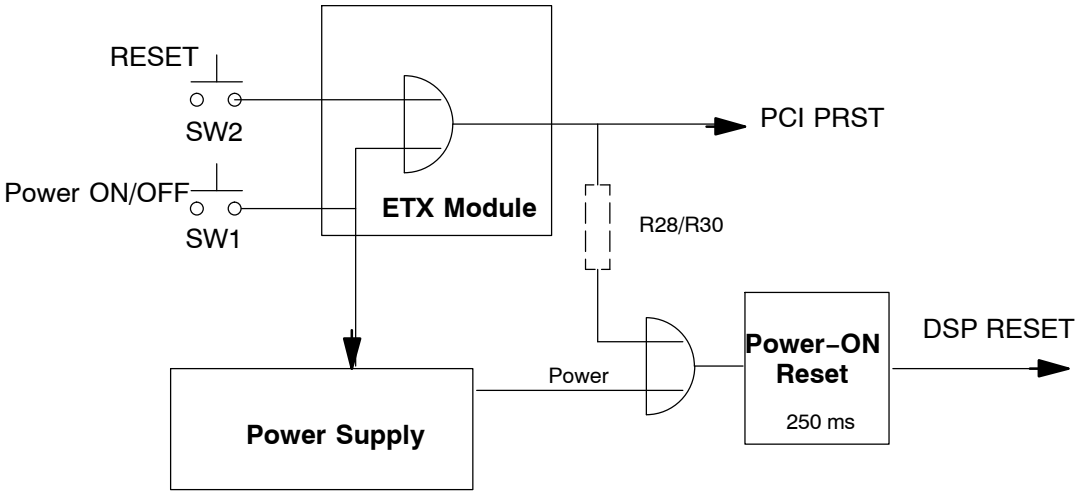


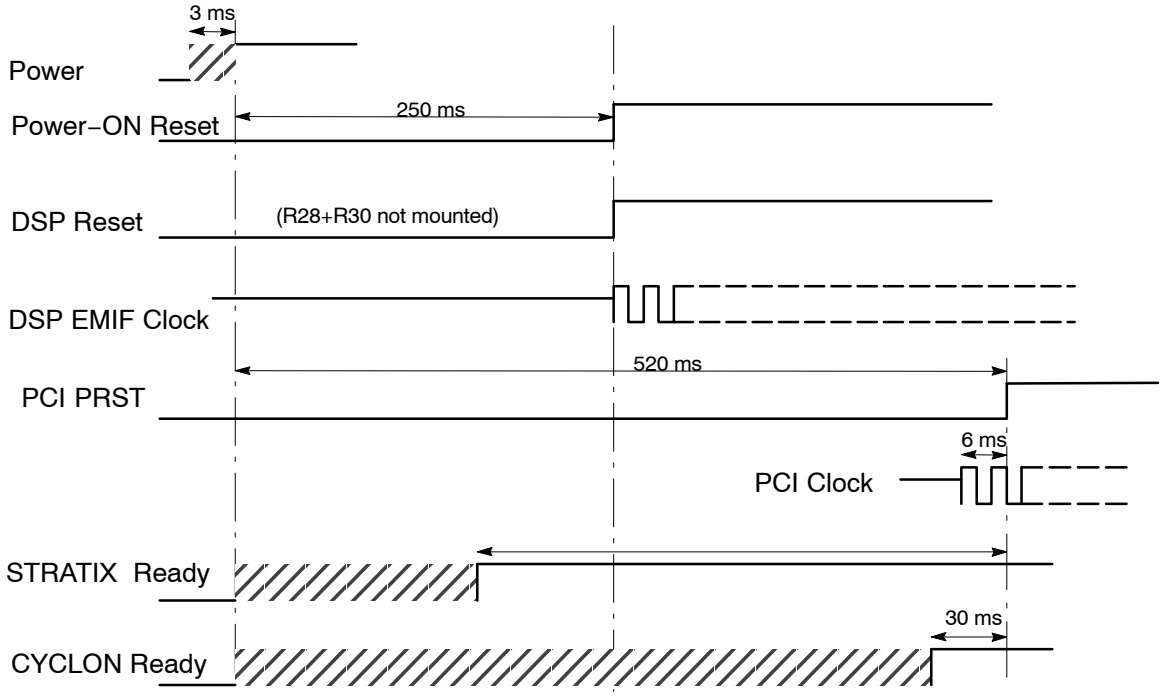
Table33: Reset Functions

RESET Sources	DSP RESET Controls		
	WARM RESET	DSP pin $\overline{\text{RESET}}$=0	PCI $\overline{\text{PRST}}$=0
SW1: Power ON/OFF		x ↓	x ↓
SW2: Reset			x ↓
DSP PCI IO–Reg HDCR	x ↓		
Controlled Functions			
Reset of PC–Module		x	x
Sample of DSP Config Pins		x	
DSP ConfigReg Reset			x
DSP ConfigReg read from EEPROM			x
Reset of DSP PCI IO–Reg		dependend on Bit#	

	WARM RESET	DSP pin $\overline{\text{RESET}}$=0	PCI $\overline{\text{PRST}}$=0
Controlled Functions			
Reset of DSP Memory mapped Reg	x	x	dependend on Bit#
DSP PCI FIFO Reset	(x)?		x
DSP Core Reset	x		
DSP Peripheral Logic Reset	x		
DSP awaking from power down modes	x		

Reset Timing

Figure13: Power−On Reset Timing

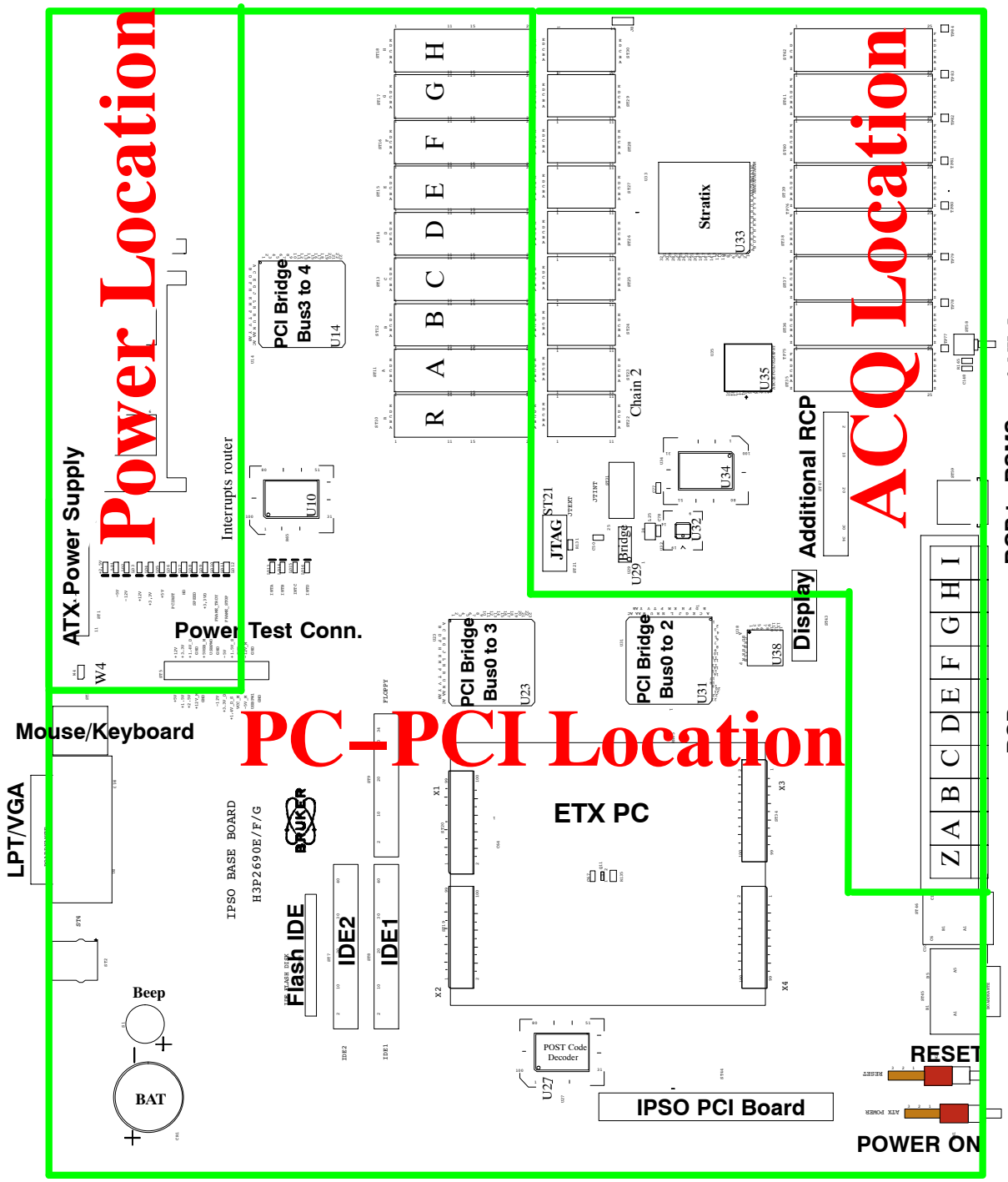


3. 5. Engineering Design

IPSO Base Board of the IPSO 19” model, H12519

Form

Figure14: IPSO Base Board, H12519 and its connector locations



Ports

tty0/tty1	RS232 Interface
ETH	10/100 Mbit Ethernet Interface

USB — USB 1.0; e.g. useable for Mouse and Keyboard

RCP — Application specific Real Time Clock pulses
19 additional RCP signals without Coax locations are kept attachable at connector ST47 inside the 19–inch–case.
The pin assignment of RCP signals is included in chapter “1”.

Display — Connector for Post Code Hex and LED devices

IPSO PCI B. — Connector for the “Standard PCI Slot” adapter (H12524)

IDE — Standard Interface to Hard Disks, if any.
Hard Disks are non–mandatory options.

Flash IDE — Interface to to a Flash–HD, if any.
Flash–HD is a non–mandatory option.

LPT — PC Standard Parallel port

VGA — PC Standard Interface for graphical monitors.
A Monitor at IPSO is a non–mandatory option but necessary to check and modify the BIOS settings.

Mouse/Keyb. — PC Standard PS/2 Mouse and Keyboard Interfaces

ATX Power — PC Standard Power Supply Connector

JTAG Structure

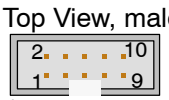


Figure15: Pin count of the JTAG connectors

Table34: JTAG pre bridge connect. (19U, H12519 ST21; AQS, H12547 ST20)

Pin #	Signal	Pin #	Signal
1	TRST*	6	JTAG Power +5V
2	Cable Detection	7	TMS
3	TDO	8	GND
4	GND	9	TCK
5	TDI	10	GND

Table35: JTAG connect. after bridge (19U H12519 ST21; AQS H12547 ST19)

Pin #	Signal	Pin #	Signal
1		6	GND
2	Cable Detection	7	TMSL1
3	TDOL1	8	GND
4	GND	9	TCKL1
5	TDIL1	10	GND

Table36: IPSO 19” Host, H12519 JTAG structure

IC	JTAG Chain 1		JTAG Chain 2		JTAG Chain 3	
	IN	OUT	IN	OUT	IN	OUT
U34	TDIL1	TD1A				
U32	TD1A	TDOL1				

IC	JTAG Chain 1		JTAG Chain 2		JTAG Chain 3	
	IN	OUT	IN	OUT	IN	OUT
U33			TDIL2	TD2A		
U35			TD2A	TDOL2		
U14					TDIL3	TD3A
U10					TD3A	TD3B
U27					TD3B	TD3C
U23					TD3C	TD3D
U31					TD3D	TD3E
U38					TD3E	TDOL3

Power

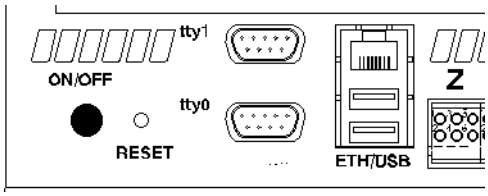
Table37: Power requirements of IPSO 19” Host, H12519

Part–No.	Assembly		+5V	Σ +5 V	+3,3V	+12V	+5VSB	–12V
H12519	IMB	ETX VIA 400Mhz + IMB		2,5 A	2,5 A	0,1	(1,8A)	0,1
H12519	IMB	ETX PM 800Mhz + IMB		2,8 A	2,5 A	0,1	(1,66A)	0,1

3. 6. Connectors and Pin Allocation

PC Standard Interface Connectors

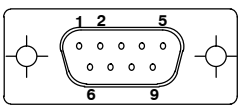
Figure16: Location of the tty, ETH and USB ports at the IPSO 19inch Unit



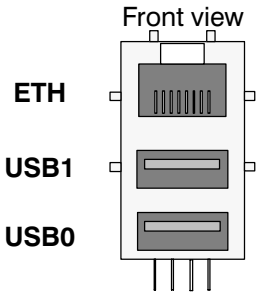
tty0 and tty1 ports (RS232)

Table38: RS232 signals of ports tty0 and tty1, male

RS232 port tty0/tty1			
Pin	Signal	Pin	Signal
1	DCD1	2	DSR1
3	RXD1	4	RTS1
5	TXD1	6	CTS1
7	DTR1	8	RI1
9	GND		



Combined Ethernet and USB Port connector



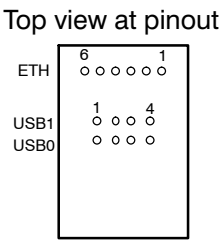


Table39: Ethernet Port

Ethernet Port Connector			
Pin #	**Signal**	**Pin #**	**Signal**
1		2	TxD+
3	TxD–	4	RxD+
5	RxD–	6	

Table40: USB Connectors Signal Assignment

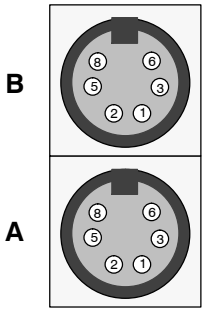
USB Port 0 connector				USB Port 1 connector			
Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
1	VCC_USB0	2	USB0–	1	VCC_USB1	2	USB1–
3	USB0+	4	GND_USB0	3	USB1+	4	GND_USB1

Keyboard, Mouse connectors (PS/2)

The location of these connectors is inside the IPSO case. Attaching a cable to them at the front panel is not possible. The IPSO AQS has to be pulled out of the rack and supplied with power by a standard ATX extension cable.

Table41: Signal Assignment of the Keyboard and Mouse Connectors, female

Keyboard connector B				Mouse connector A			
Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
1	KB_DAT	2		1	MS_DAT	2	
3	GND	5	VCC_KB	3	GND	5	VCC_KB
6	KB_CLK	8		6	MS_CLK	8	



Connectors of Parallel Port (LPT) and Analog Video output (VGA)

The location of these connectors is inside the IPSO case. Attaching a cable to them at the front panel is not possible. The IPSO AQS has to be pulled out of the rack and supplied with power by a standard ATX extension cable.

Figure17: Parallel port and VGA connector, both female

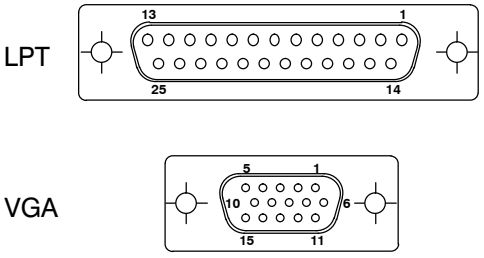


Table42: Pin Assignment of Parallel Port and VGA Port

Parallel Port Connector					Analog Video (VGA) Port Connector			
Pin #	**Signal**	**Pin #**	**Signal**		**Pin #**	**Signal**	**Pin #**	**Signal**
1	STB#	2	AFD#		1	ROUT	2	GOUT
3	PA0	4	ERR#		3	BOUT	4	CK_DDC_OUT
5	PA1	6	INIT#		5	GND	6	Shield
7	PA2	8	SLIN#		7	Shield	8	Shield
9	PA3	10	GND		9	DDC_PWR	10	GND
11	PPA4	12	GND		11		12	DDC_DATA_OUT
13	PPA5	14	GND		13	HSYNC	14	VSYNC
15	PPA6	16	GND					
17	PPA7	18	GND					
19	ACK#	20	GND					
21	BUSY#	22	GND					
23	PE#	24	GND					
25	SLCT#	26	GND					

IDE1, IDE2 connectors

The location of these connectors is inside the IPSO case. Attaching a cable to them at the front panel is not possible. The IPSO AQS has to be pulled out of the rack and supplied with power by a standard ATX extension cable.

The Flash Disc connector is connected in the same way to the signals of Secondary IDE2. Its pin distance is 2mm instead of 0.1 inch.

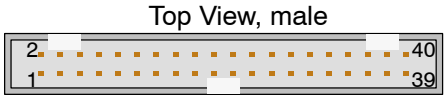


Figure18: Pin count of the IDE connectors

Table43: Signal Assignment of IDE Connectors

Primary IDE1 connector				Secondary IDE2/Flash IDE connector			
Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
1	HDRST#	2	GND	1	HDRST#	2	GND
3	PIDE_D7	4	PIDE_D8	3	SIDE_D7	4	SIDE_D8
5	PIDE_D6	6	PIDE_D9	5	SIDE_D6	6	SIDE_D9
7	PIDE_D5	8	PIDE_D10	7	SIDE_D5	8	SIDE_D10
9	PIDE_D4	10	PIDE_D11	9	SIDE_D4	10	SIDE_D11
11	PIDE_D3	12	PIDE_D12	11	SIDE_D3	12	SIDE_D12
13	PIDE_D2	14	PIDE_D13	13	SIDE_D2	14	SIDE_D13
15	PIDE_D1	16	PIDE_D14	15	SIDE_D1	16	SIDE_D14
17	PIDE_D0	18	PIDE_D15	17	SIDE_D0	18	SIDE_D15
19	GND	20		19	GND	20	
21	PIDE_DRQ	22	GND	21	SIDE_DRQ	22	GND
23	PIDE_IOW#	24	GND	23	SIDE_IOW#	24	GND
25	PIDE_IOR#	26	GND	25	SIDE_IOR#	26	GND
27	PIDE_RDY	28		27	SIDE_RDY	28	
29	PIDE_AK#	30	GND	29	SIDE_AK#	30	GND
31	PIDE_INTR	32		31	SIDE_INTR	32	
33	PIDE_A1	34		33	SIDE_A1	34	
35	PIDE_A0	36	PIDE_A2	35	SIDE_A0	36	SIDE_A2
37	PIDE_CS1#	38	PIDE_CS3#	37	SIDE_CS1#	38	SIDE_CS3#
39	PK5V	40	GND	39	SK5V	40	GND
				41	VCC (Flash only)	42	VCC (Flash only)
				43	GND (Flash only)	44	

ATX Power connector

Figure19: ATX Power connector

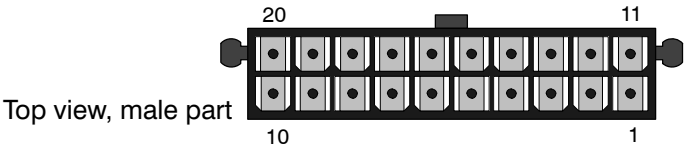


Table44: ATX Power Supply Signal Assignment

Pin #	Signal	Pin #	Signal
1	3,3V	11	3,3V
2	3,3V	12	–12V
3	COM	13	COM
4	5V	14	PS–ON
5	COM	15	COM
6	5V	16	COM
7	COM	17	COM
8	PW–OK	18	–5V
9	5VSB	19	5V
10	12V	20	5V

IPSO Power Test connector

Figure20: Power Test Connector

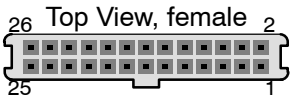


Table45: Power Test Connector ST5 Signal Assignment (IPSO 19” only)

Pin #	Signal	Pin #	Signal
1	+12V	14	–12V
2	+5.0V	15	–5.0V
3	+3.3V	16	+3.3_DV
4	+1.5V	17	+1.5_SV
5	1.4_DV	18	+1.4_D_SV
6	+2.5V	19	GND
7	GND	20	VCC_M
8	+12_MV	21	–12_MV
9	+5SBV	22	–5.0_MV
10	GND	23	GND
11	+USBPW	24	+USBPW1
12		25	
13	GND	26	GND

4. Controller IPSO–Tx

Versions

Location	Name	Part#	EC#	FW#	Increments	Software Req.
IPSO 19”	IPSO TxController, 2–MB, TMS320C6415	H12538F1	00			
IPSO 19”	IPSO TxController, 2–MB, TMS320C6415	H12538F1	03		FIFO Termination	
IPSO 19”	IPSO TxController, 16–MB, TMS320C6415	H12538F2	00		Deskew, 16–MB	
IPSO 19”	IPSO TxController, 128–MB, TMS320C6455	H12538F3	00		128–MB, TMS320C6455	

Concerned

Part# 86868 LVDS Cable, 1m

Features

- The TxController can be configurated by software to fulfill one of three different tasks in the system:
  –as F–Controller (FCtrl) generating the frequency parameter stream
  –as G–Controller (GCtrl) generating the Gradient stream and
  –as T–Controller (TCtrl) generating the RCP stream
- Each TxController outputs a stream of 48–bit words at a clock rate of 80 MHz per word
- Transferral of a complete set of frequency parameters requires two words.
- The time resolution of parameter switching in any combination of Frequency, Phase, Amplitude is 12.5 nsec.
- The minimal duration of any combination of parameters is 25 nsec.
- Gradient channels require one word per gradient.
- The maximal number of addresses for different gradients (the max. number of gradient channels) is 1k.
- A constant time delay between the outputs of the different TxControllers may be adjusted to any number of 80MHz clock cycles up to 2^{29}x12.5nsec
- The timing of each TxController is controlled by its part of a sequencer.
- The sequencer parts of all TxControllers and their means of communication (AQ–Bus) are accommodated in one piece of silicon which is known as “The Sequencer”.

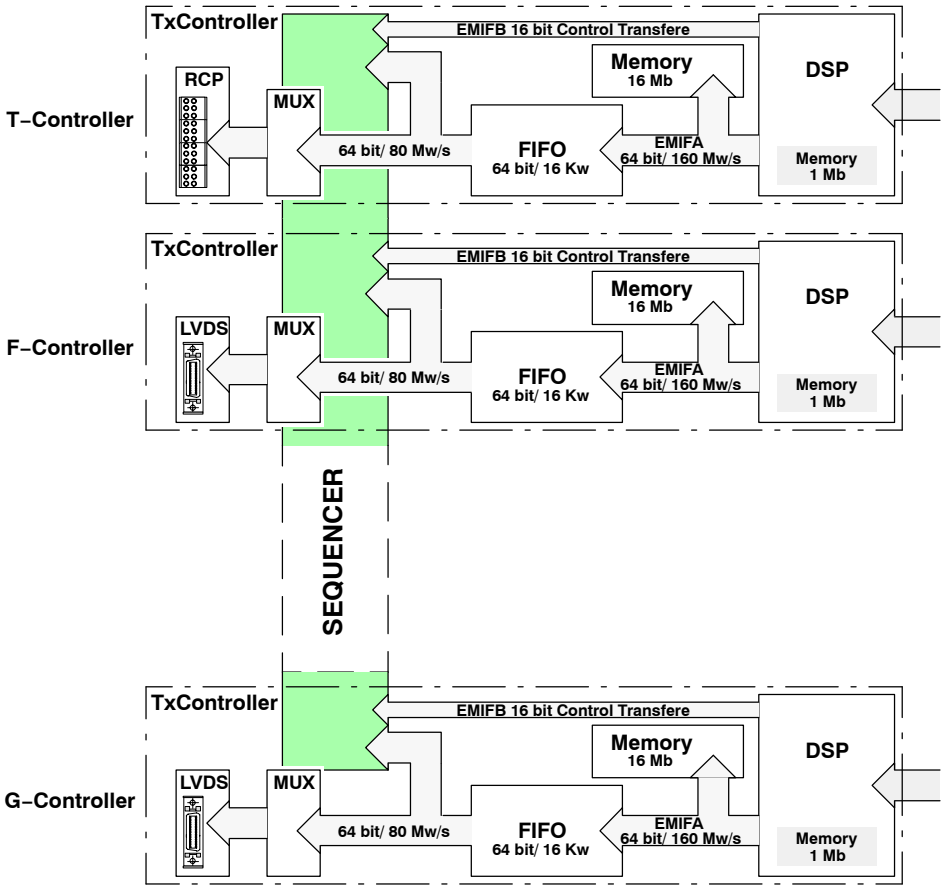
Operation

The controller consists of a DSP with memory, FIFO, output logic and interfaces to the system bus and the Sequencer. The DSP gets its code from the Host Controller, generates the parameter sequences and writes them into the FIFO. Its most important task is to keep the FIFO full. The Sequencer (once started) reads the words out of the FIFOs of all controllers, realizes the defined timing in each channel and controls the outputs.

The global functions of the Sequencer (e.g. START, STOP, SUSPEND, RESUME and so on) are part of the Sequencer logic of the T−Controller. Therefore a T−Controller has to be in the system to carry out any type of acquisition.

Architecture

Figure21: The TxController as T−, F− and G−Controller



4. 1. Structure of Output Data

According to the respective task of the TxController (as F−Controller, G−Controller or T−Controller), the bits of the 64−bit FIFO words are combined in a different way and bear different information. In case of the T−controller, some of the FIFO bits control the RCP outputs at the Coax−Connectors.

4. 1. 1. F−Controller

In the F−controller, a FIFO data set consists of two 64−bit words A+B. The bits 1 to 33 of the A word hold the control and delay information of that channel needed by the “Sequencer”. The remaining bits of both words contain the control information for the “SGU”. These 96 bits are multiplexed to two 48−bit words which are transmitted back−to−back through the LVDS interface to the “SGU”.

FIFO Word Structure

Table46: Word A in the FIFO of F−Controller (64Bit DSP → FIFO FORMAT)

Bit	64	...	55	54	53	...	38	37	36	35	34	33	32	...	2	1
Field	Register_Data REG 9::0			SH_ VAL	Amplitude SHAPE 15::0			free				OUT	Sequencer Control+Duration			A
Number	10			1	16			4				1	31			1

Table47: Word B in the FIFO of F−Controller (64Bit DSP → FIFO FORMAT)

Bit	64	63	62	61	60	59	58	57	56	55	54	...	39	38	37	36	35	...	2	1
Field	REG_ VAL 1::0		PLS gate	PA gate	A gate	NCO_sel 2::0			PH_VA L 1::0		PHASE 15::0			F_VAL 2::0			F_DATA 33::0			B
Number	2		3			3			2		16			3			34			1

LVDS Word Structure

Table48: Wort A at LVDS−Interface (Transfer FCTRL to SGU)

Bit	48	47	46	45	44	43	42	...	33	32	...	17	16	...	1
Field	PAR	SYN	WID	PLS	PA	A	REG 9::0			PHASE 15::0			SHAPE 15::0		
Number	1	1	1	3			10			16			16		

Table49: Wort B at LVDS−Interface (Transfer FCTRL to SGU)

Bit	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	...	1
Field	PAR	SYN	WID	NCO_SEL 2::0			REG_VAL 1::0		F_VAL 2::0			PH_VAL 1::0		SH_ VAL	F_DATA 33::0		
Number	1	1	1	3			2		3			2		1	34		

Table50: Bit Fields of the F−Controller Output Word

Field	Value	Description
F_DATA 33::0		34 Bit Frequency information
SHAPE 15::0		16 Bit Amplitude information
PHASE 15::0		16 Bit Phase information
REG 9::0		10 Bit Register data
PLS, PA, A		3 Bit Gate information
SH_VAL		1 Validbit of Amplitude information
PH_VAL 1:0		2 Validbit of Phase information
F_VAL 2:0		3 Validbit of Frequency
REG_VAL 1::0		2 Validbit of Register data
NCO_SEL 2::0		3 Select bits
WORD_ID(WID)		Bit 46 in each Wort
	0	Word A
	1	Word B

Field	Value	Description
SYNCHRO		Reflects the current state of the 20−MHz reference clock at transmitter
PARITY		The even parity bit, created from Bit 1 to 46

Idle State

The LVDS interface is continuously sending. In the idle state (if no valid words have to be transmitted) the interface sends repeatedly the default word “0x200000000007”

Bit	48	47	46	45	44	43	42	...	33	32	...	17	16	...	1
Field	PAR	SYN	WID	Default Word of the Idle State											
Value	0	x	1	0 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0111											

4. 1. 2. G−Controller

In the G−controller, a FIFO data set can consists of two or more 64−bit words A+B1+B2+... . The bits 1 to 33 of the A word hold the control and delay information of that channel needed by the “Sequencer”. The remaining B words contain the Gradient−Data which are multiplexed to the 48−bit Gradient Words and transmitted through the LVDS interface to the Gradient Amplifier.

Either Gradient words contain a NG bit (!NG=0) and no data (!VALID=1) or data (!VALID=0) and no NG (!NG=1). The word with the NG bit sets the time at which all the Gradient Data, transferred since the previous NG, will be active.

FIFO Word Structure

Table51: A−Wort at FIFO output

Bit	64	...	35	34	33	32	...	2	1
Field	reserved			NG	OUT	Sequencer Control+Duration			A/B
Number	30			1	1	31			1

Table52: B−Wort at FIFO output

Bit	64	...	48	47	...	44	43	...	38	37	...	22	21	...	18	17	...	6	5	4	3	2	1
Field	reserved			MSB Address						MSB Data						Data (res)			res.		LAST	VALID	A/B
				ADD<9::6>			ADD<5::0>			DATA <19::0>						gnd			gnd				
Number	17			4			6			16			4			12			1	1	1	1	1

LVDS Word Structure

Table53: Gradient Word at LVDS interface, 48 Bit, 80 MHz

Bit	48	47	...	44	43	...	38	37	...	22	21	...	18	17	...	6	5	4	3	2	1
Field	PAR	MSB Address						MSB Data						Data (res)			(res)		!LAST	!VALID	!NG
		ADD<9::6>			ADD<5::0>			DATA <19::0>						gnd			gnd				
Number	1	4			6			16			4			12			1	1	1	1	1

Table54: Bit Fields of the G−Controller Words

Field	Value	Description
A/B		Word ID
	0	A−Word
	1	B−Word
OUT		Sequencer Information
	1	Means that the following B words contain data which has to be transferred via the LVDS (NG=1 or Valid=1)
		OUT is high active
	0	No transmit of A or B content via LVDS; only bit 1 to 33 of A word contain valid information
!NG		Next−Gradient−Bit, High−Active in FIFO, Low−Active at LVDS−Interface
	0	This A word generates a Gradient word which contains NG only, no data (!VALID=1).
	1	This word must contain !VALID=0 and Gradient data
!VALID		Gradient Data Valid−Bit; High−Active in FIFO, Low−Active at LVDS−Interface
	0	This word contains Gradient data and no “Next Gradient”; !NG=0 in the same word would be a fatal error.
	1	No Gradient data in this Word
PAR		Parity bit; Even Parity of Bit1 to 47
!LAST	0	Indicates the last word of the Gradient data set with !NG=0 or !VALID=0; High−Active in FIFO, Low−Active at LVDS−Interface

Idle State

The LVDS interface is continuously sending. In the idle state (if no valid words have to be transmitted) the interface sends repeatedly the default word “0x200000000007” with Valid and NG not active.

Bit	48	47	46	45	44	43	42	...	33	32	...	17	16	...	1
Field	PAR	SYN	WID	Default Word of the Idle State											
Value	0	x	1	0 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0111											

4. 1. 3. T−Controller

In the T−controller, a FIFO data set consists of two 64−bit words A+B. The bits 1 to 33 of the A word hold the control and delay information of that channel needed by the “Sequencer”. The remaining bits of both words contain the control information for the RCP signals.

High= 5 Volt
Low= 0 Volt

These 67 bits of “setnmr 0, 3 and 4”are connected to the Coax−Outputs and gain control at the same time

FIFO Word Structure

Table55: FIFO A−Word

Bit	64	63	62	61	60	59	58	57	...	36	35	34	33	32	...	2	1
Field	res			setnmr0 (34,33,32)			setnmr4 (31)	res			free		OUT	Sequencer Control + Duration			A/B
Number	6						1	22			2		1	31			1

Table56: FIFO B−Word

Bit	64		34	33		2	1
Field	setnmr4 (30,...,0)			setnmr3 (31,..,0)			A/B
Number	31			32			1

Table57: Control Fields of the T−Controller FIFO Words

Field	Value	Description
A/B		Word ID
	0	A−Word
	1	B−Word
OUT		Sequencer Information
	1	Means that the RCP outputs will be updated with the state of the setnmr−bits (OUT is “High”−Active in the FIFO)
	0	No update of the RCP outputs

4. 2. Software Interface

All resources of the TxController except the FIFO can be accessed by the software running local on the DSP or by the software that runs on the Host−Controller via the PCI bus. Due to the 32−bit interface of the PCI bus the FIFO is accessible only by the DSP.

Both address rooms (DSP+Host−Controller) are spanned by 32−bit addresses. An address window into the address room of each DSP is arranged in the address room of the Host−Controller. The arrangement of these windows is defined by the PCI base register and the DSP−Page register of each DSP.

4. 2. 1. PCI Addresses

The content of the Base−register (<Base>) is defined by the BIOS of the Host−Controller.

The content of the DSPP−Registers (<DSPP>) defines the software running on the Host−Controller. The DSPP−Register is accessible via the Nonprefetchable−Range.

Table58: Relation between PCI−Addresses and local addresses

	4 MByte Prefetchable Range		8 MByte Nonprefetchable Range	
	Bit [31::22]	Bit [21::0]	Bit [31::23]	Bit [22::0]
PCI Address	<Base0>	AD [21::0]	<Base1>	AD [22::0]
Local Address	<DSPP>		0000 0001 1	

4. 2. 2. Local Address Layout

Table59: Memory Map of the DSP 6415

Local Hex Address Range	Block Size (Bytes)	Bus	Data Bus Width (Bytes)	Description	Utilization
000x xxxx	1M	Internal	8	Onchip RAM	
0180 0000 − 0183 FFFF	256K	Internal		EMIFA Config. Register	

Local Hex Address Range	Block Size (Bytes)	Bus	Data Bus Width (Bytes)	Description	Utilization
0184 0000 – 0187 FFFF	256K	Internal		L2 Cache Config. Register	
0194 0000 – 0197 FFFF	256K			Timer 0 Register	
0198 0000 – 019B FFFF	256K			Timer 1 Register	
019C 0000 – 019F FFFF	256K			Interrupt Select Register	
01A0 0000 – 01A3 FFFF	256K			Enhanced DMA Register	
01A8 0000 – 01AB FFFF	256K	Internal		EMIFB Config. Register	
01AC 0000 – 01AF FFFF	256K	Internal		Timer 2 Register	
01B0 0000 – 01B3 FFFF	256K	Internal		GPIO Register	
01C0 0000 – 01C3FFFF	256K			PCI Register	
6000 0000 – 63FF FFFF	64M	EMIFB CE0	2	External RAM	Register
6400 0000 – 67FF FFFF	64M	EMIFB CE1	2	External RAM	Register
6800 0000 – 6BFF FFFF	64M	EMIFB CE2	2	External RAM	BIS Flash Prom
6C00 0000 – 6FFF FFFF	64M	EMIFB CE3	2	External RAM	
8xxx xxxx	256M	EMIFA CE0	8	External RAM	RAM
9xxx xxxx	256M	EMIFA CE1	8	External RAM	FIFO 16Kx64
Axxx xxxx	256M	EMIFA CE2	8	External RAM	
Bxxx xxxx	256M	EMIFA CE3	8	External RAM	

4. 2. 3. Content of the DSP Configuration Registers

Table60: EMIFA Configuration Register

Local Hex Address	Acronym	Value	Description
1800048	CE0SEC	00000042	EMIFA CE0 Space Secondary Control
1800044	CE1SEC		EMIFA CE1 Space Secondary Control
		00000060	TxController with 2 MByte SRAM
		00000064	TxController with 16 MByte SDRAM
1800050	CE2SEC	unmodified	EMIFA CE2 Space Secondary Control
1800054	CE3SEC	unmodified	EMIFA CE3 Space Secondary Control
1800000	GBLCTL		EMIFA global Control
		00012024	TxController with 2 MByte SRAM
		00010034	TxController with 16 MByte SDRAM
1800008	CE0CTL		EMIFA CE0 Space Control
		FFFFFFE3	TxController with 2 MByte SRAM
		FFFFFFD3	TxController with 16 MByte SDRAM
1800004	CE1CTL	FFFFFFE3	EMIFA CE1 Space Control

Local Hex Address	Acronym	Value	Description
1800010	CE2CTL	FFFFFFB3	EMIFA CE2 Space Control
1800014	CE3CTL	FFFFFFB3	EMIFA CE3 Space Control
1800018	SDCTL		EMIFA SDRAM Control
		0248f000	TxController with 2 MByte SRAM
		47228000	TxController with 16 MByte SDRAM
180001C	SDTIM		EMIFA SDRAM Refresh Control
		00000000	TxController with 2 MByte SRAM
		0000094C	TxController with 16 MByte SDRAM
1800020	SDEXT		EMIFA SDRAM Extension
		00175F3F	TxController with 2 MByte SRAM
		0005052B	TxController with 16 MByte SDRAM

Table61: EMIFB Configuration Register

Local Hex Address	Acronym	Value	Description
1A80000	GLBCTL	00012024	EMIFB global Control
1A80008	CE0CTL	5055C11D	EMIFB CE0 Space Control, Register
1A80004	CE1CTL		EMIFB CE1 Space Control, Register
		5055C11D	on TCTRL
		FFFFFFBF	on FCTRL and GCTRL
1A80010	CE2CTL	2A22E80A	EMIFB CE2 Space Control, BIS Flash Prom
1A80014	CE3CTL	FFFFFFBF	EMIFB CE3 Space Control, not used

All EMIF Memory Mapped Register which are not mentioned are filled at Power−up with a default value. Therefor they have no meaning with respect to the configuration of the TxController.

Table62: GPIO Configuration Register

Local Hex Address	Acronym	Value	used as	Description
01B00000	GPEN	0x1FF		GPIO Bit Enable; Usage of the GPIO Pin GP0,...,GP8 as IO Pin
01B00004	GPDIR	0xE		Direction of GPIO Pins adjusted as:
		0	SGU Status “Ask me”,	GP0 Input on TCTRL, not applied on F− and GCTRL
		−	not applied	GP1 Output
		−	not applied	GP2 Output
		−	not applied	GP3 Output
		1 → 0	DSP EXT_INT4 Sequencer Error Interrupt	GP4 Input
		1 → 0	DSP EXT_INT5 Emergency Stop Interrupt	GP5 Input
		1 → 0	DSP EXT_INT6 FIFO allmost empty, the FIFO contains less than 33 words	GP6 Input
		1 → 0	DSP EXT_INT7 FIFO allmost full, the FIFO can accept less than 31 words	GP7 Input

Local Hex Address	Acronym	Value	used as	Description
		0	Emergency Stop active	GP8 Input on TCTRL, not applied on FCTRL and GCTRL
01B00008	GPVAL	0xFF		GPIO Value Register, Output Value of GPIO

4. 2. 4. Memory at EMIFA

Table63: Type of external Memories used on the TxControllers

Local Hex Address	Size [MByte]	Word [Byte]	Type	Bandwidth [MByte/s]	Type of Controller	Identification
8000 0000 – 801F FFFF	2	8 Byte	SRAM	1280	TxCtrl H12538	imbf=FFFF or 0000 and slot_brdv=XFXX or X0XX
8000 0000 – 80FF FFFF	16	8 Byte	SDRAM	1280	TxCtrl H12538F1 H12538F2	imbf=FFFF or 0000 and slot_brdv=X1XX
					AQS–ACQ H12549	imbf=0001 and t_brdv=0000

4. 2. 5. FIFO at EMIFA

The FIFO is filled by the DSP using the signal CE1 and address “0x9xxx xxx”. Its content is read by the Sequencer.

Table64: Type of FIFOs used on the TxControllers

Local Hex Address	Size [Kbyte]	Word [Byte]	Type	Bandwidth [MByte/s]	Type of Controller	Identification
9xxx xxxx	128	8 Byte		1280	TxCtrl H12538	slot_brdv=XFXX or X0XX
					TxCtrl H12538F1 H12538F2	slot_brdv=X1XX
					AQS–ACQ H12549	t_brdv=0000

4. 2. 6. Flash Prom at the EMIFB Bus

EMIF bus properties accessing the BIS Flash Prom:

Bus width: 2 Byte, data bit 7,...,0 implemented, data bit 15,...,8 not implemented; therefor the Prom occupied the double address room.

Cycle operation: synchronal

Cycle duration ca. 85 sneak for the write cycle and 270 nsec for the read cycle.

Table65: Type of Flash Proms used on the TxControllers

Local Hex Address	Size [KByte]	Word [Byte]	Type	Type of Controller	Identification
6800 0000 – 6801 FFFF	64	1 Byte		TxCtrl H12538	slot_brdv=XFXX or X0XX
				TxCtrl H12538F1 H12538F2	slot_brdv=X1XX
6800 0000 – 6801 FFFF at T-Controller only	64	1 Byte		AQS–ACQ H12549	t_brdv=0000

4. 2. 7. Registers at the EMIFB Bus

All registers of the TxController itself and its registers inside the Sequencer are serviced via the EMIFB with following properties:

Bus width: 2 Byte, data bit 15,...,0

Cycle operation: Asynchron, ready controlled

Cycle duration About 144 nsec for the write cycle and 120 nsec for the read cycle

Address Layout on EMIFB space CE0: Common Control Register

Table66: Ctrl. Regs. common on F–, G– and T–Controller, EMIFB, space CE0

Acronyms	Local Address	Function	Mode R/W	Bit
rtrig	60000000	External Trigger and FIFO Output	R	15–0
mflag	60000004	Flag Register (LFLG, FFLG, MFLG)	W	2–0
fifores	60000008	FIFO Reset Control	W	xxxx
seqsts	6000000C	Sequencer & FIFO Status Register	R	15–0
delaya	60000010	write/read Delay Register A	W/R	15–0
delayb	60000014	write Delay Register B	W	15–0
seqlst	60000018	Sequencer local start	W	xxxx
seqres	6000001C	Reset of the Sequencer	W	xxxx
seqctl	60000020	Sequencer Interrupt Control Register	W	8–0
seqint	60000024	Sequencer Interrupt Register	W/R	15–0
rcpout	60000028	enable/disable RCP Output	W	Bit 0
fpgavsn	6000002C	Version of FPGA	R	15–0
chanconf	60000030	Channel Configuration	R	15–0
slot_brdv	60000038	Slot and Board Version of FCtrl/GCTRL	R	15–0

Table67: Output Ctrl. Regs. on F– and G–Controller, EMIFB, space CE0

Acronyms	Local Address	Function	Mode R/W	Bit
selfg	60000034	select GCtrl or FCtrl Function	W	0
semif	60000058	select FIFO or register set to LVDS output	W	0
dstrb	6000005C	generate Data valid Strobe	W	x
srgs	600000A4	Select Register Set for read back	W	0
NGS	60000060	generate Next Gradient Signal	W	x
goutA	60000064	Bypass Register A	R/W	15–0
goutB	60000068	Bypass Register B	R/W	15–0
goutC	6000006C	Bypass Register C	R/W	15–0
foutD	60000098	Bypass Register D	W	15–0
foutE	6000009C	Bypass Register E	W	15–0
foutF	600000A0	Bypass Register F	W	15–0
lvds_dsk	600000A8	LVDS Deskew	R/W	1–0

Address Layout on EMIFB space CE0: RCP Output Register and Version Register

Table68: RCP Output and Version Reg. on T–Controller, EMIFB, space CE0

Acronyms	Local Address	Function	Mode R/W	Bit
t_brdv	6000003c	Board Version of IPSO AQS ACQ	R/–	15–0
rcpout	60000028	Disable/Enable RCP Outputs	–/W	0
tout4	60000040	TCtrl Output Reg. 4	R/W	5–0
tout3	60000044	TCtrl Output Reg. 3	R/W	15–0
tout2	60000048	TCtrl Output Reg. 2	R/W	15–0
tout1	6000004C	TCtrl Output Reg. 1	R/W	15–0
tout0	60000050	TCtrl Output Reg. 0	R/W	15–0
selrcp	60000054	Select FIFO or tout–Registers as RCP source	–/W	0
fpgavsn	6000002C	Read Version of Sequencer FPGA	R/–	15–0

Address Layout on EMIFB space CE1: AQ–Bus Control Register and spin rotation counter control

Table69: AQ–Bus Control Registers on T–Controller, EMIFB, space CE1

Acronyms	Local Address	Function	Mode R/W	Bit
seqstart	64000078	Start the Sequencer	–/W	xxxx
seqstop	6400007C	Stop the Sequencer	–/W	xxxx
aqst_clr	64000074	Release AQSTART (Sequencer Stop)	–/W	xxxx
seqsus	64000080	Suspend of the Sequencer	–/W	xxxx
seqrsm	64000084	Resume of the Sequencer	–/W	xxxx
sustrig	64000088	select Trigger for Suspend	–/W	2–0
synctrig	6400008C	Synchronize Trigger with the Next–Value Clock	–/W	3–0
lgcnt	64000090	Load Next–Value Counter	–/W	15–0
emstop	64000070	Set Emergency Stop	–/W	Bit 0
reserve gl_chanconf	64000094	Read Gl. Channel Configuration temp. currently not used	R/–	15–0
srtrsel	640000AC	Spin Rotation Trigger select	–/W	3–0
srcen	640000B0	Spin Rotation counter enable read sr_counter control Signal	W R	Bit 0 15–0
src1	640000B4	read Spin Rotation counter1	R	15–0
src2	640000B8	read/write Spin Rotation counter2	R/W	15–0

4. 2. 7. 1. Registers of common use on all TxCtrl–Functions

Register Description: Control Registers on EMIFB, space CE0

Read external Trigger (rtrig)

rtrig	60000000	Read external Trigger and FIFO Output	R	15–0

TRIG1–4 are the external trigger signals. Their state can be checked by access to these registers.

Bit 4 to Bit 15 are used by the test software only. The FIFO ID and the FIFO outputs Bit 21 to Bit 31 can be read via these bits.

Bit	15		5	4	3	2	1	0
Field	Fifo Data Out Bit31 – Bit21			FIFO Word ID	TRIG 4	TRIG 3	TRIG 2	TRIG 1

Sequencer Flag Register (mflag)

mflag	60000004	Flag Register (LFLG, FFLG, MFLG)	W	2–0

The register contains the Flags which define the functional priority and dependency of this channel.

The state of these flags can be read via 0x6000000C.

Bits	15		3	2	1	0
Field	Not implemented			MFLG	FFLG	LFLG
Reset State				0	0	0

Table70: Sequencer Flag Register

Field	Value	Description
MFLG FFLG LFLG		Master Flag First Flag Last Flag Configured as Master (111), a channel can only be reconfigured by changing the Flags with subsequent ’SEQRES’. These Flags are not cleared by ’SEQRES’. After Power–up are all Flags = 0 (Slave)
MFLG FFLG LFLG	000	Slave Controller; Its Delay Register contains a greater value as the Master Controller
	001	Last Slave Controller; with largest Delay Register content
	010	Illegal code
	011	Illegal code
	100	Independent Controller Its Delay Register contains the same value as the Master Controller
	101	Independent but for Wait; Its Delay Register contains the same value as the Master Controller; A Wait is finished by the Last Slave.
	110	Master Controller when there are not Slaves in the system
	111	Master Controller with dependent Slaves

FIFO Reset Device Code (fifores)

fifores	60000008	FIFO Reset Control	W	xxxx

Writing to this address (no data) clears the internal FIFO counters and the FIFO Flag Logic (= clear of contents)

Sequencer & FIFO Status Register (seqsts)

seqsts	6000000C	Sequencer & FIFO Status Register	R	15–0

This register contains the operational state of that channel.

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fields																

Table71: Sequenzer & FIFO Status Register

Field	Value	Description
Bit15		Master Flag, MFLG
Bit14		First Flag, FFLG
Bit13		Last Flag, LFLG
Bit 12		FIFO output ready
	0	Output ready to be read, FIFO contains at least one word
	1	FIFO empty
Bit11		FIFO Half Full Flag
	0	FIFO contains more than 4096 words
	1	FIFO contains less than 4096 words
Bit10		PAE, Flag of FIFO almost empty; threshold adjusted to 32 words
	0	FIFO contains less than 33 word, EXT_INT6 of the DSP is activated
	1	FIFO contains more than 32 words
Bit9		PAF, Flag of FIFO almost full; threshold adjusted to 31 words
	0	The FIFO can accept less than 31 further words, EXT_INT7 of the DSP is activated
	1	The FIFO can accept more than 31 further words
Bit8		FIFO input ready
	0	Input ready, FIFO not full
	1	FIFO full
Bit7		State of the AQSTART signal of the AQ−Bus Since setting the Start−FF can be synchronized with the Next−Value Clock, Bit7=0 can be delayed after seqstart by a full clock period (at least 1 microseconds).
	0	AQSTART active, Start−FF set
	1	AQSTART inactive, Start−FF reset
Bit6		SLEEP_ST, controller specific sleep state after reading of a sleep instruction
	0	awake
	1	sleeping
Bit5		Stop−Window signal of the AQ−Bus
	0	Stop−Window set; The Master−Controller has halted and calls on all Slaves to stop at the next Stop instruction
	1	No Stop from Master
Bit4		Decision−Window signal of the AQ−Bus
	0	Decision−Window set, The Master−Controller has decided on IF or ELSE, shows the result with Bit3 and calls on all Slaves to do the same at their next IF/ELSE instruction
	1	No decision from Master
Bit3		IF/ELSE signal of the AQ−Bus showing the Master’s decision
	0	Decision for IF
	1	Decision for ELSE
Bit2		Controller specific WAIT status after reading a WAIT instruction
	0	No WAIT
	1	WAIT

Field	Value	Description
Bit1		Suspend–Window signal of the AQ–Bus
	0	The Master–Controller has gone into the suspend mode (halted) and calls on all Slaves to stop at their next SUSPEND instruction, to set Bit0=1 of this register, to set the DSP interrupt EXT_INT4
	1	No Suspend situation
Bit0		Controller specific Suspend status
	0	No Suspend
	1	Suspend

Sequencer Delay Register (delaya, delayb)

delaya	60000010	write/read Delay Register A	W/R	15–0
delayb	60000014	write Delay Register B	W	12–0

The content of the delay counter defines the independent start delay of this channel in steps of 12,5nsec. The maximal delay is 6,5sec. The counter contains 29 bits. Therefor, the two register locations A+B are required to write to the counter.

Register A can also be read to provide a test facility.

Bit	15	14	13	12		0	15		0
Field	not used			Register B			Register A		
	not used			29 Bit Delay Register					

Sequencer local Start Device Code (seqlst)

seqlst	60000018	Sequencer local start	W	xxxx

Writing to the “Sequencer Local Start” address (no data) puts this Sequencer part from IDLE to RUN state and enables this channel to follow the global acquisition start instruction “AQ-START”.

After Power–up, Reset or in case of an error interrupt, the Sequencer part of this channel enters the IDLE state and any AQSTART is cleared. Resuming the normal operation requires “selqst” in each channel followed by “AQSTART”.

Sequencer Reset Device Code (seqres)

seqres	6000001C	Reset of the Sequencer	W	xxxx

Writing to the “Sequencer Reset” address (no data) puts this Sequencer part from RUN to IDLE state and disables this channel to follow the global acquisition start instruction “AQ-START”. The operating duration and the control and status register of this channel are cleared.

Resuming the normal operation requires “selqst”.

AQSTART is not affected by “seqres”.

Table72: Control of Sequencer RUN/IDLE

Field	Value	Causal Event	Condition	Description
Local SEQ	IDLE → RUN	Write to seqlst	–	Sequencer part of this channel enabled for AQSTART
	RUN → IDLE	Write to seqres Write to seqstop Write to aqst_clr Reset	–	Sequencer part of this channel disabled for AQSTART

Sequencer Interrupt Control Register (seqctl)

seqctl	60000020	write Sequencer Intr. Control Register	W	8–0

This register operates as the Interrupt Mask Register for interrupts 0 to 8. Set to “high” enables the respective source to interrupt the DSP.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	not used							Int 8	Int 7	Int 6	Int 5	Int 4	Int 3	Int 2	Int 1	Int 0
Reset State	not used							0	0	0	0	0	0	0	0	0

Table73: Sequencer Interrupt Control Register

Field	Value	Description
Interrupt 0	1	Programmed Interrupt (high active)
Interrupt 1	1	STOP Interrupt (high active)
Interrupt 2	1	Illegal Instruction Interrupt
Interrupt 3	1	Illegal configuration of the channel
Interrupt 4	1	Suspend Interrupt
Interrupt 5	1	ILLEGAL WORD Interrupt
Interrupt 6	1	Empty FIFO Interrupt
Interrupt 7	1	IF_ELSE Interrupt
Interrupt 8	1	Error Interrupt nested if else sequence

Sequencer Interrupt Register (seqint)

seqint	60000024	write/read Sequencer Interrupt Status Register	W/R	15–0

The register shows the state of the interrupt sources. An interrupt is active if the corresponding bit is high.

The sources of bit 0 t0 8 activate the EXT_INT4 (GP4) of the DSP if the respective bit in the “Sequencer Interrupt Control Register” is set.

Writing a “1” to any of these bits clears the state of the corresponding source.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	Int_Vec				Int 11	Int 10	Int 9	Int 8	Int 7	Int 6	Int 5	Int 4	Int 3	Int 2	Int 1	Int 0

Table74: Sequencer Interrupt Status Register

Field	Value	Description
Interrupt 0	1	Programmed Interrupt (high active), out of the Pulse Program
Interrupt 1	1	STOP Interrupt (high active)

Field	Value	Description
Interrupt 2	1	Illegal Instruction Interrupt
Interrupt 3	1	Illegal configuration of the channel
Interrupt 4	1	Suspend Interrupt
Interrupt 5	1	ILLEGAL WORD Interrupt
Interrupt 6	1	Empty Fifo Interrupt
Interrupt 7	1	If_ELSE Interrupt
Interrupt 8	1	Error Interrupt nested if_else sequence
Interrupt 9	x	unused
interrupt 10	1	programmed Stop Status (high active)
Interrupt 11	1	AQSTOP error Status (high active)
Int_Vec Bit 12	1	programmable Interrupt vector Bit(0) (high active)
Int_Vec Bit 13	1	programmable Interrupt vector Bit(1) (high active)
Int_Vec Bit 14	1	programmable Interrupt vector Bit(2) (high active)
Int_Vec Bit 15	1	programmable Interrupt vector Bit(3) (high active)

Read Channel configuration Register (chanconf)

chanconf	60000030	Channel Configuration	R	15–0

The bits of the “Channel Configuration Register” provide informations about the version of the instaled controller, its function and mounting option.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	Board Function			Version						FCTRL Channel			External Config. Bit			

Table75: Channel Configuration Register

Field	Value	Description
External Config. Bits		Details of “Board Function”:
		On F–Controller and G–Controller: Bit 0 and 1 provide the type of the device connected via LVDS
	xx00 xx01 xx10 xx11	Bit 2+3 are reserved DPP connected GCUTYPE=11 SGU connected Gradient Amp connected GCUTYPE=10 nothing connected
	xx00 xx01 xx10 xx11	On T–Controller of IPSO AQS ACQ: Bit 0 and 1 provide the type of installed RCP–Adapter (HR or FTMS) Bit2+3 are unused reserved ACQ with FTMS Adapter ACQ with HR Adapter No Adapter
FCtrl Channel		Provides the channel number 1 to 8 of this FCtrl On TCtrl and RCtrl is the FCtrl Channel= 0. GCtrl takes a subsequent number

Field	Value	Description
	111	F−Controller1
	110	F−Controller2
	101	F−Controller3
	100	F−Controller4
	011	F−Controller5
	010	F−Controller6
	001	F−Controller7
	000	F−Controller8 or TCtrl, RCtrl
Version		
		On Fx−Controller:
	000001	Indicates the logic version of the output multiplex device (FPGA EP1C6F256).
Board Function		Indicates the function of this channel.
	000	TCtrl
	001	FCtrl
	010	GCtrl
	100	RCtrl

Slot−Board Vers. Register from FCTRL, GCTRL or TCTRL (slot_brdv)

slot_brdv	60000038	PCI SLot and Board Version of a TxController	R	15−0

The register contains the slot address and the hardware version of a TxController

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	Slot Add.				Board Revision				Board Subrevision							

Table76: Slot−Board−Version Register

Field	Value	Description
Board Revision		
	0000	IPSO−TX with 2MB external RAM+TMS320C6415; H12538F1
	0001	IPSO−TX with 16MB external RAM+TMS320C6415; H12538F2
	0002	IPSO−TX with 128MB external RAM+TMS320C6455; H12538F3
Board Subrevision	00000000	8 bit number for future use
Slot−Add		Slot address of this controller
	0001	Slot 1
	0010	Slot 2
	0011	Slot 3
	0100	Slot 4
	0101	Slot 5
	0110	Slot 6
	0111	Slot 7
	1000	Slot 8
	1001	Slot 9

4. 2. 7. 2. Registers used on F−Controller and G−Controller

Register Description: Output Control Register on EMIFB, space CE0

Select GCTRL or FCTRL function (selfg)

selfg	60000034	select GCtrl or FCtrl Function	W	0

1−bit register for configuration of this TxController as F−Controller or G−Controller.

This register is not affected by the Sequencer reset.

Field	Value	Description
		The state is indicated by a LED at the front panel below the LVDS connector. Default after Power−up is Bit<0> = 0: FCtrl
Write to Bit 0	0	Command cff: Tx as F−Controller ; LED=green
	1	Command cfg: Tx as G−Controller; LED=orange

Select FIFO or EMIF−Bypass Registers to feed the LVDS (semif)

semif	60000058	select FIFO or register to become source of the LVDS output	W	0

1−bit register switching the LVDS output from FIFO to a set of registers (gout, fout) and vice versa.

Field	Value	Description
		Default after Power−up is Bit<0> = 0: FIFO connected to LVDS
Bit 0	0	Connects FIFO to LVDS; Reset State
	1	Connects the EMIFB registers goutA, goutB, goutC, foutD, foutE, foutF to LVDS

The Bypass Register Set (goutA – goutC , foutD – foutF)

goutA	60000064	Bypass Register A	R/W	15−0
goutB	60000068	Bypass Register B	R/W	15−0
goutC	6000006C	Bypass Register C	R/W	15−0
foutD	60000098	Bypass Register D	W	15−0
foutE	6000009C	Bypass Register E	W	15−0
foutF	600000A0	Bypass Register F	W	15−0

Bypassing the FIFO and the Sequencer, the software on DSP can transmit the content of these pre loaded registers via LVDS.

The transmit process is triggered by “dstrb” (see below).

The content of all registers can be read back and checked (see below)

Function	Condition	Description
Write to dstrb	semif=1 selfg=0	Transmitting the content of goutA, −B, −C and foutD, −E, −F as 2 words A+B in F−Controller format for the SGU The bits 46, 47, 48 are hardware controlled
Write to dstrb	semif=1 selfg=1 goutA<1>=1 goutA<0>=0	Transmitting the content of goutA, −B, −C as 1 Gradient data word in G−Controller format
Read from goutA, goutB, goutC	selgf=0 semif=1 srgs=0	Provides the content of gout−Register A, B, C
Read from goutA, goutB, goutC	selgf=0 semif=1 srgs=1	Provides the content of fout−Register D, E, F
Read from goutA, goutB, goutC	selgf=0 semif=0	Provides the content of the FIFO output

Figure22: Bypass Registers goutA, goutB, goutC to LVDS as SGU−A−Word

LVDS Bit	48	47	46	45	44	43	42	...	33	32	...	17	16	...	1
gout	not applied			goutC 12::0						goutB 15::0			goutA 15::0		
Meaning on SGU	PAR	SYN	WID =0	PLS	PA	A	REG 9::0			PHASE 15::0			SHAPE 15::0		

Figure23: Bypass Registers foutD, foutE, foutF to LVDS as SGU−B−Word

Bit	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	...	17	16	...	1
fout	not applied			foutF 12::0													foutE15::0			foutD15::0		
Meaning on SGU	PAR	SYN	WID =1	NCO_SEL 2::0			REG_VAL 1::0		F_VAL 2::0			PH_VAL 1::0		SH_VAL	F_DATA 33::0							

Figure24: Bypass Regs. goutA, goutB, goutC to LVDS, Gradient−Data−Word

Bit	48	47	...	44	43	...	38	37	...	33	32	...	18	17	16	...	6	5	4	3	2	1
gout	na	goutC 15::0									goutB 15::0				goutA 15::0							
Meaning on Grad. Amp.	PAR	MSB Address						MSB Data						Data (res)				(res)		LAST	VALID	NG
		ADD<9::6>		ADD<5::0>				DATA <19::0>						gnd				gnd				

Generate Data valid Strobe (dstrb)

dstrb	6000005C	generate Data valid Strobe	W	x

Writing to this address (no data) sends one or two words out of the gout−registers and fout−registers respectively via the LVDS port (if the registers are selected, addr 60000058):

Function	Condition	Description
Write to dstrb	semif=1 selfg=0	Transmitting the content of goutA, −B, −C and foutD, −E, −F as 2 words A+B in F−Controller format for the SGU The bits 46, 47, 48 are hardware controlled
Write to dstrb	semif=1 selfg=1 goutA<1>=1 goutA<0>=0	Transmitting the content of goutA, −B, −C as 1 Gradient data word in G−Controller format

Generate Next Grad Signal (ngs)

ngs	60000060	generate Next Gradient Signal	W	x

Writing to this address (no data) sends one Next Gradient word out of the gout−registers via the LVDS port (if the registers are selected, addr 60000058):

Figure25: Bypass Regs goutA, goutB, goutC to LVDS, Next Gradient Word

Bit	48	47	...	33	32	...	17	16	...	3	2	1
gout	na	goutC 15::0			goutB 15::0			goutA 15::2			n.a.	
Field	PAR	not allocated								!LAST	1	0

Function	Condition	Description
Write to nsg	semif=1 selfg=1	Transmitting the content of goutA, –B, –C as Next Gradient word in G–Controller format

Select Register Set (srgs)

srgs	600000A4	Select Register Set for read back	W	0

This 1–bit register selects the register goutA, –B, –C or fout–D, –E, –F for reading back of its content, both via the addresses of the gout register 60000064, –68, –6C:

Field	Value	Description
		Default after Power–up, sequencer reset “seqres” and Reset is Bit<0> = 1: foutA, –B, –C selected
Bit 0	0	Connects the outputs of the registers goutA, goutB, goutC to EMIFB
	1	Connects the outputs of the registers foutD, foutE, foutF to EMIFB

LVDS Deskew Operation (lvds_dsk)

lvds_dsk	600000A8	LVDS Deskew	R/W	1–0

The register is provided for controlling the Deskew–Process of the LVDS transmitter. Deskew initiates sending a test sequence which enables the receiver to compensate the delay difference between the line pairs of the cable. To be successful, Deskew needs also to be enabled at the receiver.

Deskew is not important if the cable is shorter than 3 meters.

Deskew is carried out after Power–up and should also be carried out by a software command (which one ?) if the LVDS connection have been interrupted without subsequent Power–up.

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fields	not applied														DSK_Flag	LVDS_DSK

Table77: LVDS Deskew Register

Field	Value	Description
LVDS_DSK		R/W
	1	Deskew not active; normal data send mode; this is the state after Reset or Power–up
	0	Deskew Command; process active, sending test sequence
DSK_Flag		R/–
	1	Deskew not yet carried out after last Power–up or last line interrupt
	0	Deskew have been carried out; state reached by LVDS_DSK=0;

4. 2. 7. 3. Registers used on T–Controller only

Register Description: RCP Output Register and Version Register on EMIFB, space CE0

Read Board Vers. Register via TCTRL (t_brdv)

t_brdv	6000003c	Board Version of IPSO AQS ACQ	R	15–0

The revision number makes important hardware features identifiable.

So far valid for IPSO AQS ACQ only

Bits	15		8	7		0
Fields	Board Rev			Sub Rev		

Table78: Board Version Register t_brdv

Field	Value	Description
Board Rev		R/–
	00	IPSO 19”: Default IPSO AQS: ACQ Board with 5 Controllers and 16 MByte RAM+TMS320C6415; H12549
	02	IPSO AQS: ACQ Board with 5 Controllers and 128 MByte RAM+TMS320C6455; Hxxxxx
Sub Rev		R/–
	00	IPSO 19”: Default IPSO AQS: ACQ Board with 5 Controllers and 16 MByte RAM+TMS320C6415; H12549 ACQ Board with 5 Controllers and 128 MByte RAM+TMS320C6455; Hxxxxx

Disable/Enable RCP Outputs (rcpout)

rcpout	60000028	Disable/Enable RCP Outputs	–/W	0

1–bit register to enable or disable (high impedance state) the RCP outputs (Coax).

The RCP outputs are disabled after Power–up or Reset. They are pulled to 5–Volt.

This register has no function, if the TxCtrl is used as F–Controller or G–Controller

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fields	not applied															rcpout

Table79: Register rcpout

Field	Value	Description
rcpout		–/w
	0	RCP outputs active
	1	RCP outputs inactive; State after Reset, Power–On and commando rcpdis

RCP Output Register 0–4 (tout0 –tout4)

tout4	60000040	TCTRL Output Reg. 4	R/W	5–0
tout3	60000044	TCTRL Output Reg. 3	R/W	15–0
tout2	60000048	TCTRL Output Reg. 2	R/W	15–0
tout1	6000004C	TCTRL Output Reg. 1	R/W	15–0
tout0	60000050	TCTRL Output Reg. 0	R/W	15–0

Normally the RCP outputs are controlled by the bit stream of the FIFO output bits. Using register ”selrcp”, the RCP’s can be disconnected from the FIFO and connected to the RCP

Output Registers. This requires presetting the registers with the desired value. This can be done when the RCP’s are in high impedance state (after Power−up or if rcpout=1).

The register contents can be read back via their outputs if rcpout=1 (see below).

Table80: Relations between tout−registers, FIFO−words and setnmr−words

Bit	15	...	6	5	4	3	2	1	0	15	...	0	15	...	0	15	...	0	15	...	0
Register	not applied			tout4						tout3			tout2			tout1			tout0		
FIFO Word	not applied			A (64,...,58)						B (64,...2)											
setnmr	not applied						setnmr0 (34,33,32)			setnmr4 (31,...,0)						setnmr3 (31,...,0)					
RCP out	not applied			69	68	67	66	65	64	63	...	48	47	...	32	31	...	16	15	...	0

Table81: T−Controller Output Register tout0,...,tout4

Function	Condition	Description
Write to tout0,..,tout4	selrcp=1 rcpout = x	setting the registers without any effect to the RCP outputs
Write 0 to selrcp		Switching the source of the RCP outputs from FIFO to tout0,...,4
Read from tout0,...,tout4	rcpout = 1	Reading the contents of tout0,...,4

Select FIFO or RCP tout−Register (selrcp)

selrcp	60000054	Select FIFO or tout−Registers as RCP source	−/W	0

1−bit register to select the tout−Registers or the FIFO outputs to be the source for the RCP outputs (Coax).

After changing the selection to the FIFO, the RCP outputs keep the contents of the tout−registers up to the time when the Sequencer sends the next RCP data word out of the FIFO.

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fields	not applied															selrcp

Table82: Register rcpout

Field	Value	Description
selrcp		−/w
	0	tout−registers selected as RCP source
	1	FIFO selected as RCP source; Default state after Reset and Power−On

Read Version of Sequencer FPGA (fpgavsn)

fpgavsn	6000002C	Read Version of Sequencer FPGA	R/−	15−0

A read access of this address delivers the version of the Sequencer logic (Stratix FPGA)

The default value is 0x0001.

Table83: Sequencer Program Version

Field	Value	Description
fpgavsn	0001	Default or first shipped version

Register Description: AQ−Bus Control Register on T−Controller, EMIFB, sr_counter, space CE1

The following registers control the global AQ−Bus functions. These functions affect all controllers in the system.

These registers are exclusively accessible on the TxController operating as T−Controller.

Start Sequencer (seqstart)

seqstart	64000078	Start the Sequencer	−/W	xxxx

A write access to this address (without data) sets the Start Flag and consequently activates the AQSTART signal of the AQ−Bus which initiates all controllers to start.

Setting the Start Flag is synchronized with the 20−MHz clock and the Next−Value clock of the Gradient channel.

Stop Sequencer Device Code (seqstop)

seqstop	6400007C	Stop the Sequencer	−/W	xxxx

A write access to this address (without data) clears the Start Flag and consequently clears the AQSTART signal of the AQ−Bus which initiates all controllers to stop.

The partial sequencers of all controllers stop and interrupt their respective DSPs (DSP EXT_INT4).

Clear AQSTART (aqst_clr)

aqst_clr	64000074	Clear AQSTART (Sequencer Stop)	−/W	xxxx

Just like seqstop, a write access to this address (without data) clears the Start Flag and consequently clears the AQSTART signal of the AQ−Bus which initiates all controllers to stop and to interrupt their respective DSPs (DSP EXT_INT4).

aqst_clr is also carried out by Power−up and Reset.

Table84: Control of AQSTART

Field	Value	Causal Event	Condition	Description
AQSTART	1 → 0	Write to seqstart	RUN	All partial Sequ. being in RUN mode, start working
	0 → 1	Write to seqstop	−	All partial Sequ. stop and enter the IDLE state; next RUN state not until Write to seqlst; DSP EXT_INT4 initiated
	0 → 1	Write to aqst_clr Reset	−	All partial Sequ. stop and enter the IDLE state; next RUN state not until Write to seqlst; DSP EXT_INT4 initiated; EXRDEN is set inactive;

Suspend Sequencer (seqsus)

seqsus	64000080	Suspend of the Sequencer	−/W	xxxx

A write access to this address (without data) sets the SUSP_RES (suspend/resume) signal of the AQ−Bus to “1”. This causes two actions:

1. It initiates the Sequencer of the "Master" channel to stop when the next suspend instruction occurs.
2. It sets the SUSPEND_WINDOW signal of the AQ−Bus to "1".

Subsequently, every Sequencer of a slave channel stops and enters the "suspend" state when it receives a instruction which is labeled as a "suspend instruction" from the FIFO. Necessary condition is SUSP_RES=1 and SUSPEND_WINDOW=1.

After Power−up or Reset (SEQRES) is SUSP_RES=1 (suspend state).

Resume Sequencer (seqrsm)

seqrsm	64000084	Resume of the Sequencer	−/W	xxxx

A write access to this address (without data) clears the SUSP_RES (suspend/resume) signal of the AQ−Bus to "0".

This causes the Sequencer of all channels to count down their respective delay counters and resume reading instructions out of the FIFO. This operation starts simultaneously with a low−to−high slope of the 20−MHz clock and the Next Value clock.

Table85: Control of Suspend/Resume

Field	Value	Causal Event	Condition	Description
SUSP_RES	0 → 1	Write to seqsus Reset	suspend Instr.	Master Sequencer stops and sets SUSPEND_WINDOW
		suspend Instr.	SUSP_RES=1 SUSPEND_WINDOW=1	Slave Sequencers stop at next suspend instruction
	1 → 0	Write to seqrsm	–	All Sequencers resume their operation

Select Suspend Trigger (sustrig)

sustrig	64000088	select Trigger for Suspend	−/W	2−0

Writing data to this register selects an external Trigger Signal or the write access to seqsus and seqrsm as initiator for suspend/resume

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fields	not applied													SUSP source		

Table86: Register of Suspend Trigger Select

Field	Value	Description
SUSP source		
	000	Write access to seqsus and seqrsm
	001	External trigger Trig1
	010	External trigger Trig2
	011	External trigger Trig3
	100	External trigger Trig4
	101	Write access to seqsus and seqrsm
	110	Write access to seqsus and seqrsm
	111	Write access to seqsus and seqrsm

Load Next−Value Counter (lgcnt)

lgcnt	64000090	Load Next−Value Counter	−/W	15−0

Writing data to this register determines the time period “T” of the Next−Value clock (GCLK). This clock is generated by a 16−bit counter driven with 20−MHz.

Following, the time period T is adjustable between 100ns and 6,553ms and:

$$T = (n+1) \times 100ns$$

The default period after Power−up is 10µs.

Together with the 20−MHz clock, the Next−Value clock is also used to synchronize AQ-START and SUSP_RES.

Figure26: Next−Value Counter

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fields	MSB							“n”								LSB

Trigger signal synchronization (synctrig)

synctrig	6400008C	Synchronize Trigger with the Next−Value Clock	−/W	3−0

Writing data to this register selects the external Trigger Signals to become synchronized with the 20−MHz clock and the Next−Value clock.

The trigger signal is selected by a “1” at its respective position.

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fields	not applied												Trig4	Trig3	Trig2	Trig1

Emergency Stop Register (emstop)

emstop	64000070	Set Emergency Stop	−/W	Bit 0

Writing a “1” to bit0 of this register initiates the SGU_RES (SGU reset) signal and sets for the DSP of this channel the interrupt EXT_INT5 and the status signal SGURES_ST=0 (SGU reset status) at the Global IO−pin GP8.

SGU_RES is a wired−OR signal and can be activated by external devices too. In this case, SGURES_ST is set to “1” instead of “0”.

Table87: Function of Emergency Stop

Field	Value	Causal Event	Condition	Description
SGURES	1 → 0	Internal activated by Write 0 to emstop		SGURES=0 (active) SGURES_ST=0 (DSP Global IO−Pin GP8) DSP EXT_INT5 active
		External activated		SGURES=0 (active) SGURES_ST=1 (DSP Global IO−Pin GP8) DSPEXT_INT5 active
	0 → 1	Internal deactivated by Write 1 to emstop, Reset	External not activated	SGURES=1 SGURES_ST=1 (DSP Global IO−Pin GP8)

Synchronization of Pulse Program by Spin Rotor Signal

This logic is implemented to support the software and the pulse program in dealing with following tasks:

1. To ascertain the revolution speed of the spinner.

2. To count the number of turns.

3. To synchronize the puls sequence with the rotation of the spinner and its position.

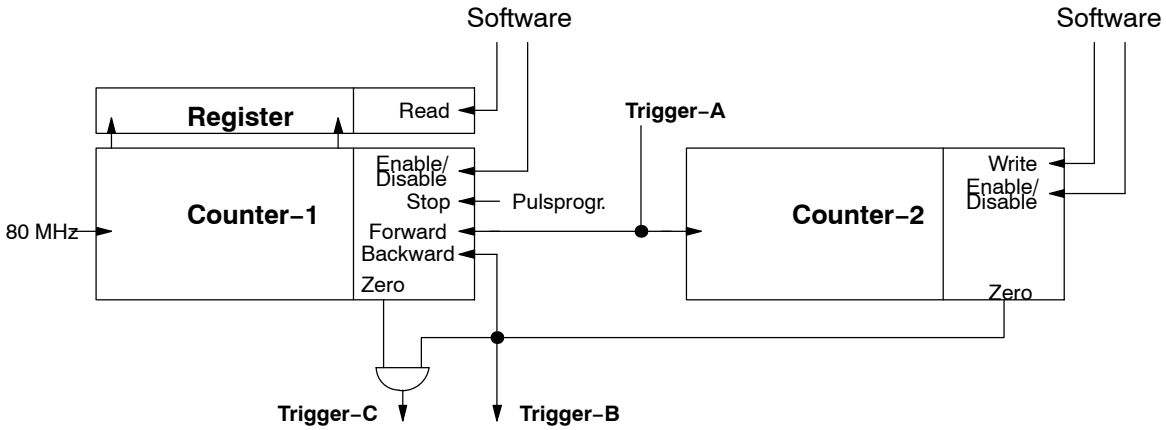
4. To stop the pulse sequence and start it again at the same position of the spinner after a predefined number of spinner−turns have elapsed. The position is measured as the number of 80−MHz clock cycles with respect to a trigger pulse representing the fixed zero−crossing of the spinner.

The logic uses two 16−bit counters (counter−1, counter−2), a read register and a signal called Trigger−A.

The logic provides the signals Trigger−B and Trigger−C.

Any external trigger signal out of Trig1,...,Trig4 has to be selected as Trigger−A, −B and −C.

Figure27: Counter logic



Functional attributes of signals and recourses:

Trigger−A:	Pulse signal representing the zero−crossing of the spinner, selcted out of Ext. Trigger 1,...,4
Trigger−B:	Predefined number of spinner revolutions reached, internal used
Trigger−C:	Predefined number of spinner revolutions and start position of next pulse sequence reached, internal used
Counter−1:	Counts 80−MHz clock cycles, forward between two zero−crossings or forward from zero−crossing up to stop and backward down to zero
Counter−2:	Counts the predefined spinner revolutions, backward down to zero
Register, src1:	Holds and provides the value of counter−1 sampled at the last zero−crossing of the spinner.

Spin Rotation trigger select (srtrsel)

srtrsel	640000AC	Spin Rotation trigger select	−/W	Bit 0−3

The assignment of the trigger signals Trig1,...,Trig4 to Trigger−A can be selected by a write to this register.

The setting of srtrsel0,...,srtrsel3 can be read back via the register “srcen”

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fields	not applied												srtrsel 3–0			

Table88: Select Reg. for external trigger source of Rotor synchronisation

Field	Value	Description
SRTRSEL	X000	Ext. Trig1 –> SR Counter Trig. input
	X001	Ext. Trig2 –> SR Counter Trig. input
	X010	Ext. Trig3 –> SR Counter Trig. input
	X011	Ext. Trig4 –> SR Counter Trig. input
	X100	Ext. Trig1 –> SR Counter Trig. input; SR Counter Trig. output –> Int. Trig1
	X101	Ext. Trig2 –> SR Counter Trig. input; SR Counter Trig. output –> Int. Trig2
	X110	Ext. Trig3 –> SR Counter Trig. input; SR Counter Trig. output –> Int. Trig3
	X111	Ext. Trig4 –> SR Counter Trig. input; SR Counter Trig. output –> Int. Trig4
	0XXX	Trigger–B (SR Counter2 Out) –> Int. TrigX
	1XXX	Trigger–C (SR Counter1 and Counter2) Out –> Int. TrigX

Spin Rotation Counter enable (srcen)

srcen	640000B0	Write srcen	–/W	Bit 0
		Read srcen	R	Bit15–0

Setting Bit–0 of this register enables or disables the counters and the logic. After Power–up, the state of Bit–0 is “0”, disabled and the counters are cleared.

Reading “srcen” gives back the states of the enable bit, the trigger select bits and the trigger status bits.

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fields	not applied							synctrig 3–0				srtrsel 3–0				srcen

Table89: Rotation Counter Enable

Field	Value	Causal Event	Condition	Description
scren	0	Power–up		Disabled
	0 → 1	Write 1 to srcen		Enabled
	1 → 0	Write 0 to srcen		Disabled

Spin Rotation Counter–1 (register src1)

src1	640000B4	read Spin Rotation counter 1	–/R	Bit 15–0

Counter–1 increments with the 80–MHz clock and is cleared at each zero–crossing of the spinner. If stopped out of the pulse program, it keeps the content, switches to the backward mode and starts decrementing if the Counter–2 reaches zero.

Up to the Stop of the pulse program, the register “scr1” will be updated with the content of Counter–1 at each zero–crossing of the spinner. Therefor, the content “N” of scr1 is representing revolution speed of the spinner (befor the Stop):

The time for one revolution is: T = (N+1) x 12,5 nsec

T can be measured between T_{min} = 25 nsec and T_{max} = 819.18 µsec

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fields	MSB	src1: Value of Counter−1 at previous zero−crossing														LSB

Table90: Rotation Counter−1

Field	Value	Causal Event	Condition	Description
src1	0	Power−up		Disabled+cleared
	0	srcen=1	before Stop	Counter−1 is incrementing up to zero−crossing of the spinner
	N	zero−crossing	before Stop srcen=1	Content of Counter posted to src1; Counter−1 cleared and incrementing again up to zero−crossing of the spinner
	N of previous zero−crossing	Stop from pulse program	after Stop srcen=1	Counter stops with content "n", (0 < n < N) and keeps "n" up to Counter−2 reaches zero.
	N	Counter−2 = 0	after Stop srcen=1	Counter−1 decrements down to zero
	N	Counter−1 = 0	after Stop srcen=1 Counter−2 = 0	Trigger−C starts the pulse program again

Spin Rotation counter2 Register(src2)

src2	640000B8	read/write Spin Rotation counter 2	W/R	Bit 15−0

Counter−2 decrements a preset value of spinner revolutions which it assumed from its preregister src2. Counter−2 starts at Stop for Counter−1, stops when it reaches zero and is reloaded with the content of scr2 when Counter−1 is reaching zero.

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fields	MSB	src2: value of Counter−2														LSB

Table91: Rotation Counter−2

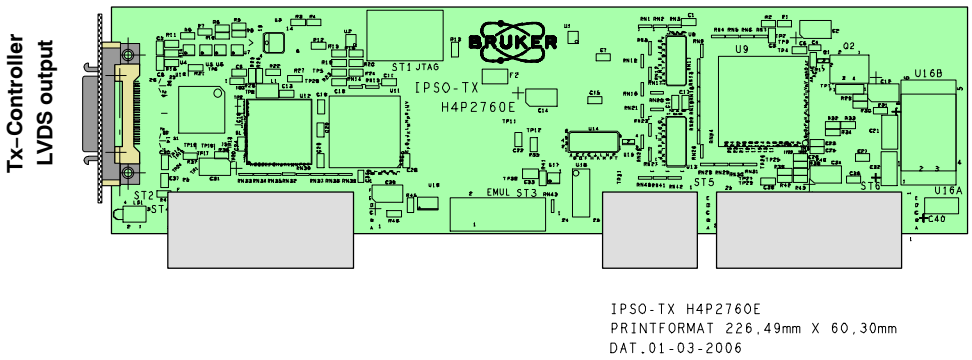
Field	Value	Causal Event	Condition	Description
src2	0	Power−up		Disabled+cleared
	0	srcen=1	before Stop	Counter−2 halted and not set
	R	Write to src2	before Stop srcen=1	Counter−2 set to a number of spinner revolutions to be carried out after Stop from pulse program
	R > r > 0	Stop of Counter−1 from pulse program	after Stop srcen=1	Counter−2 decrements at each zero−crossing of the spinner
	0	Counter−2 = 0	after Stop srcen=1	Counter−2 reaches zero and starts Counter−1 to count backwards

4. 3. Engineering Design

IPSO–Tx of the IPSO 19” model

Dimensions

Figure28: TxController Board of the IPSO 19” Unit



Ports

Data Output

- Low voltage, low noise LVDS input via 8 balanced data lines and one clock line
- Transfer rate 80 mega–words per second (480 Mbyte/s)
- Word width 48 bit

Requirements of Power

Part–No.	Assembly	+5V	+3,3V	+12V	+5VSB	–12V
H12538F2	TxController	0,6 A	0	0	0	0
H12538F3	TxController	? A	0	0	0	0

The connector of this port is located at the solder (back) side of the PCB. So several adapters with different cable connectors can be mounted next to this board.

This port comprises the following signals:

JTAG Structure and BBIS–EEPROM

For programming and testing during production, the TxControllers provide a JTAG interface to 3 JTAG Chains. Furthermore, the application software reads the board information (type, version, serial#, EC level) via this interface.

The DSP can be accessed by an emulation software via a separate connector and the Parallel Port of a PC.

Another separate connector allows bypassing the bridge and the direct access of Chain 3.

Table92: JTAG Structure on IPSO TxController Board of the IPSO 19” Unit

Connector	Stxxx	Stxxx
JTAG Bridges	Uxx, Addr=0xX	U18, Addr=0x2

Connector	–	ST??	ST??	–	ST??	ST??
JTAG Chain	**Chain1**	**Chain2**	**Chain3**	**Chain1**	**Chain2**	**Chain3**
Devices					U9:DSP	U3:EEPROM
						U12:FPGA
						U11:FIFO

4. 4. Pin allocation of Connectors

LVDS Connector

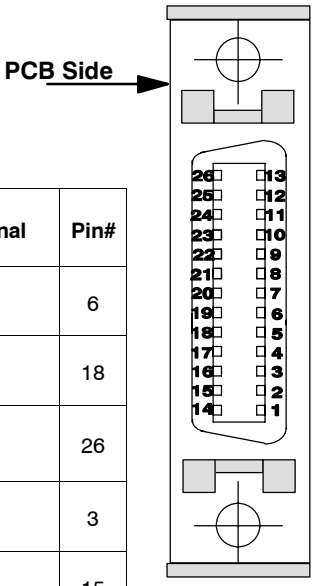


Figure29: Pin location of the 48–Bit LVDS Connector at PCB

Table93: Cable and Pin Assignment

Function	Type of Wire	Transmitter Signal	Receiver Signal	Pin#
signal: Differential Pair of the received serial transmit clock connected to the corresponding inputs of the transmitter	twisted + shielded	TxCLK_P	RxCLK_P	6
		TxCLK_M	RxCLK_M	18
shield: Common drain wire of all separate shields, connected to CHASSIS		LVDS Gnd		26
signal: Differential Pair of the received serial data stream connected to the corresponding inputs of the transmitter	twisted + shielded	TxIN_P0	RxIN_P0	3
		TxIN_M0	RxIN_M0	15
shield		LVDS Gnd		26
signal	twisted + shielded	TxIN_P1	RxIN_P1	4
		TxIN_M1	RxIN_M1	16
shield		LVDS Gnd		26
signal	twisted + shielded	TxIN_P2	RxIN_P2	5
		TxIN_M2	RxIN_M2	17
shield		LVDS Gnd		26
signal	twisted + shielded	TxIN_P3	RxIN_P3	9
		TxIN_M3	RxIN_M3	21
shield		LVDS Gnd		26
signal	twisted + shielded	TxIN_P4	RxIN_P4	10
		TxIN_M4	RxIN_M4	22
shield		LVDS Gnd		26
signal	twisted + shielded	TxIN_P5	RxIN_P5	11
		TxIN_M5	RxIN_M5	23
shield		LVDS Gnd		26
signal	twisted + shielded	TxIN_P6	RxIN_P6	12
		TxIN_M6	RxIN_M6	24
shield		LVDS Gnd		26

Function	Type of Wire	Transmitter Signal	Receiver Signal	Pin#
signal	twisted + shielded	TxIN_P7	RxIN_P7	13
		TxIN_M7	RxIN_M7	25
shield		LVDS Gnd		26
USB signal pair, left open	twisted + shielded	USB+		1
		USB−		14
Shield of the USB signal pair, connected to CHASSIS		USB Gnd		2
signal: connected to bit1 of register “chanconf” on F− and G−Controller	individual	CHANNEL_DETECT0		7
signal: connected to bit0 of register “chanconf” on F− and G−Controller	individual	CHANNEL_DETECT1		20
VCC of USB power, left open	individual	USB pwr		19
GND of USB power, connected to GND	individual	USB gnd		8
common shield of the entire bundle	Shield	CHASSIS		body

CHASSIS:

Chassis is a separate plane in the PCB layer stack. This plane is stacked close by the ground plane, giving a very tight capacitive (only capacitive) and low inductance coupling to GND. The chassis plane is screwed together with the external chassis along the front edge near the connectors and the line drivers.

This solution reduces the digital noise at that point and the noise which is picked up by the driver and carried to the outside. In addition this avoids parasitic current through the GND plane which could be caused by potential differences of the remote device.

DS_OPT, Deskew optimization:

DS_OPT of the transmitter is triggered after power up and under software intervention.
At the receiver this pin should be configuerable to High or Low which would enable or disable the receiver to optimize the skews.

5. RxController

Versions

Location	Name	Part#	EC#	FW#	Increments	Software Req.
IPSO 19”	IPSO RxController	H12532				
IPSO 19”	IPSO RxController	H12532F1			Flash	
PCI Bus	PCI RxController	H12565			Flash	

Concerned

Part# 86868 LVDS Cable, 1m

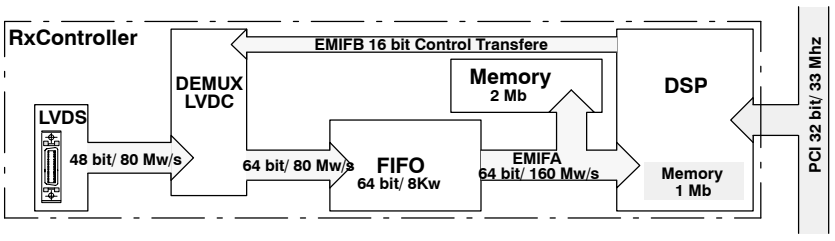
Part# DRU−M

Features

- The RxController is able to receive 48−bit words via its LVDS−Input at a clock rate of 80 MHz if connected to a TxController and at a rate of 100 MHz if connected to a DRU−M
- Rx measures the time distance of each Tx A−Word from the previous one and stores this value as a number of receive clock cycles in the upper 16−Bit of the 64−Bit receive FIFO word.
- Receive FIFO for 8KWords of 64 bit connected to the EMIFA bus of the DSP
- 64−bit DSP TMS320C6415 with 1MByte on−chip RAM, EMIFA, EMIFB, SDRAM and PCI−32Bit/33Mhz , interface
- External RAM of 2MByte/16MByte connected to the EMIFA bus
- EMIFA data bandwith of 160 MWords of 64 bits
- Separate EMIFB bus for control functions
- FLASH PROM for board and revision information

Architecture

Figure30: The RxController



Operation

The RxController is designed to receive data words of 48−bits sent by the IPSO−TxController or the DRU.

These data words are received on 8 line pairs in a serialized form. They are transferred to parallel words in the LVDS receiver and delivered to the LVDC (FPGA)at a clock rate of 80−MHz (FCtrl,

GCtrl) or 100−MHz (DRU). In the LVDC, the words are checked (validity and parity) and assigned with a time stamp fed into the FIFO. In case of a parity error, the parity flag in the Status Register is set and hold up to the FIFO will be cleared.

The 3 possible data sources (FCtrl, GCtrl, DRU) send in different formats. Therefor, 3 receiving modes have been implemented in the LVDC and selected depending on the recognized source.

The 48−bit words are stored in a FIFO which is 64−bit wide. The upper 16 bits of the FIFO words are used to hold the time stamps of each word. This time information gives the distance to the preceding word measured in numbers of clocks. The type of words which are measured and get the stamp depend on the receiving mode.

In the FCtrl mode the A−words are used. In the GCTRL−mode the distance between two NG−words is counted. In the DRU−mode, the counting starts with each Control−Word and ends at the following Control− or Data−Word.

The FIFO words can be processed by the DSP, transferred to its local memory or via the PCI Bus.

The control and status register can be accessed by the DSP via the EMIFB bus. All registers and both memories of the RxController can also be accessed by any other controller via the PCI Bus.

5. 1. Structure of input words at the LVDS−Receiver and the FIFO

Dependent on the connected data source and the associated receiving mode, the RxController checks the validity and the parity of the incoming words (A−, B−words in FCtrl mode; Gradient data and NG−words in GCtrl mode; Data− and Control words in DRU mode).

The resulting error status and the FIFO status can be read on the EMIFB bus.

5. 1. 1. Words from F−Controller

A data package from the F−Controller consists of 2 Words (A+B) in adjacent clock cycles. The TIME value in the upper 16 bits of the FIFO word is the number of clock cycles between the previous A−Word and this one.

Table94: F−Ctrl words at output of LVDS receiver and FIFO (F−Ctrl Mode)

Bit		64	...	49	48	47	46	45	...	1
Word A	**At LVDS**	not used			PAR	SYNC	WID	Data from F−Controller		
Word B		not used			PAR	SYNC	WID	Data from F−Controller		
Word A	**At FIFO**	TIME value, low part			PAR	SYNC	WID	Data from F−Controller		
Word B		TIME value, high part			PAR	SYNC	WID	Data from F−Controller		

Table95: Bit Fields of the F−Controller Output Word

Field	Value	Description
WORD_ID(WID)		Bit 46 in every word
	0	Word A
	1	Word B
SYNC		Reflects the current state of the 20−MHz reference clock at transmitter
PARITY		The even parity bit, created from Bit 1 to 46

5. 1. 2. Words from G−Controller

A Gradient switching package from the G−Controller consists of a variable number of Gradient data words and 1 Next−Gradient word. Usually, these words are transmitted in adjacent clock cycles but this is not necessary.

The TIME value in the upper 16 bits of the FIFO word is the number of clock cycles between the previous Next−Gradient word and this one.

Table96: G−Ctrl words at output of LVDS receiver and FIFO (G−Ctrl Mode)

Bit		64	...	49	48	47	...	3	2	1
Next Gradient	**At LVDS**	not applied			Parity	not allocated			!VALID	!NG
Gradient data		not applied			Parity	Gradient			!VALID	!NG
Next Gradient	**At FIFO**	TIME value, low part			Parity	not allocated			!VALID	!NG
Gradient data		TIME value, high part			Parity	Gradient			!VALID	!NG

Table97: Bit Fields of the G−Controller Output Word

Field	Value	Description
!VALID:!NG		These bits identify the Gradient data words and the Next−Gradient words which activate the Gradients transmitted since the previous Next−Gradient word
	00	Not allowed, erroneous combination
	01	Gradient data word
	10	Next−Gradient word
	11	Idle cycle without data
PARITY		The even parity bit, created form Bit 1 to 47

5. 1. 3. Words from the DRU

Table98: DRU words at output of LVDS receiver and FIFO (DRU Mode)

Bit		63	...	48	47	46	...	2	1	0
DRU Control Word	**At LVDS**	not applied			Parity	DRU Control Information			1	0
DRU Data Word		not applied			Parity	DRU Data			0	1
DRU Control Word	**At FIFO**	Time value, low part			Parity	DRU Control Information			1	0
DRU Data Word		Time value, high part			Parity	DRU Data			0	1

Table99: Bit Fields of the DRU−Controller Output Word

Field	Value	Description
!Data::!CTRL		These bits identify the DRU data words and the control words (Data and Header/ Trailer information
	00	Not allowed, erroneous combination
	01	Data word
	10	Control word
	11	Idle cycle without data
PARITY		The even parity bit, created form Bit 1 to 47

5. 2. Software Interface

Nearly all resources of the RxController can be accessed by both, software running local or software running on the Host Controller. Only the FIFO is excluded from this. The FIFO can be accessed by the DSP only.

Both address ranges, local DSP and global PCI bus, are defined by 32−bit addresses. The access from the PCI range into many local ranges is possible through address windows, 2 ones dedicated

to each controller. This is a 4−MByte window (for prefetchable accesses) and a 8−MByte window (for nonprefetchable accesses). The segmentation of the PCI address range to the window spaces the controllers is carried out by the BIOS and fixed by defining the content of all PCI−Base registers.

Every window can be moved through the local address range by modifying the content of the DSP page register (DSPP).

5. 2. 1. PCI Addresses

The content of the Base0 register is defined by the BIOS of the Host Controller.

The content of the DSPP register can be written by the software running on the Host Controller. This register can be reached through the nonprefetchable window.

Table100: Relations between PCI− and local addresses on R−Controller

	4 MByte Prefetchable Range		8 MByte Nonprefetchable Range	
	Bit [31::22]	**Bit [21::0]**	**Bit [31::23]**	**Bit [22::0]**
PCI Address	<Base0>	AD [21::0]	<Base1>	AD [22::0]
Local Address	<DSPP>		0000 0001 1	

5. 2. 2. Local Address Layout

Table101: Memory Map of the DSP 6415 on R−Controller

Local Hex Address Range	Block Size (Bytes)	Bus	Data Bus Width (Bytes)	Description	Utilization
000x xxxx	1M	Internal	8	Onchip RAM	
0180 0000 – 0183 FFFF	256K	Internal		EMIFA Config. Register	
0184 0000 – 0187 FFFF	256K	Internal		L2 Cache Config. Register	
0194 0000 – 0197 FFFF	256K			Timer 0 Register	
0198 0000 – 019B FFFF	256K			Timer 1 Register	
019C 0000 – 019F FFFF	256K			Interrupt Select Register	
01A0 0000 – 01A3 FFFF	256K			Enhanced DMA Register	
01A8 0000 – 01AB FFFF	256K	Internal		EMIFB Config. Register	
01AC 0000 – 01AF FFFF	256K	Internal		Timer 2 Register	
01B0 0000 – 01B3 FFFF	256K	Internal		GPIO Register	
01C0 0000 – 01C3FFFF	256K			PCI Register	
6000 0000 – 63FF FFFF	64M	EMIFB CE0	2	External RAM	Register
6400 0000 – 67FF FFFF	64M	EMIFB CE1	2	External RAM	
6800 0000 – 6BFF FFFF	64M	EMIFB CE2	2	External RAM	BIS Flash Prom
6C00 0000 – 6FFF FFFF	64M	EMIFB CE3	2	External RAM	

Local Hex Address Range	Block Size (Bytes)	Bus	Data Bus Width (Bytes)	Description	Utilization
8xxx xxxx	256M	EMIFA CE0	8	External RAM	RAM
9xxx xxxx	256M	EMIFA CE1	8	External RAM	
Axxx xxxx	256M	EMIFA CE2	8	External RAM	
Bxxx xxxx	256M	EMIFA CE3	8	External RAM	FIFO 16Kx64

5. 2. 3. Content of the DSP Configuration Registers

Table102: EMIFA Configuration Register

Local Hex Address	Acronym	Value	Description
1800048	CE0SEC	00000042	EMIFA CE0 Space Secondary Control
1800044	CE1SEC	unmodified	EMIFA CE1 Space Secondary Control
1800050	CE2SEC	unmodified	EMIFA CE2 Space Secondary Control
1800054	CE3SEC	00000040	EMIFA CE3 Space Secondary Control
1800000	GBLCTL	00012724	EMIFA global Control RxController with 2 MByte SRAM
1800008	CE0CTL	FFFFFFE3	EMIFA CE0 Space Control RxController with 2 MByte SRAM
1800004	CE1CTL	unmodified	EMIFA CE1 Space Control, not used
1800010	CE2CTL	unmodified	EMIFA CE2 Space Control, not used
1800014	CE3CTL	FFFFFFE3	EMIFA CE3 Space Control, FIFO
1800018	SDCTL	0248f000	EMIFA SDRAM Control RxController with 2 MByte SRAM
180001C	SDTIM	003F05DC	EMIFA SDRAM Refresh Control RxController with 2 MByte SRAM
1800020	SDEXT	00175F3F	EMIFA SDRAM Extension RxController with 2 MByte SRAM

Table103: EMIFB Configuration Register

Local Hex Address	Acronym	Value	Description
1A80000	GLBCTL	00012324	EMIFB global Control
1A80008	CE0CTL	5055C11D	EMIFB CE0 Space Control, Register
1A80004	CE1CTL	FFFFFFBF	EMIFB CE1 Space Control, not used
1A80010	CE2CTL	2A22E80A	EMIFB CE2 Space Control, BIS Flash Prom
1A80014	CE3CTL	FFFFFFBF	EMIFB CE3 Space Control, not used

Table104: GPIO Configuration Register

Local Hex Address	Acronym	Value	used as	Description
01B00000	GPEN	0x1FF		GPIO Bit Enable; Usage of the GPIO pins GP0,...,GP8 as IO pins
01B00004	GPDIR	0xE		Direction of GPIO Pins adjusted as:
		–	not applied	GP0 Input
		–	not applied	GP1 Output
		–	not applied	GP2 Output
		–	MCBSP2 enable of serial PCI Config Prom	GP3 Output
		–	not applied	GP4 Input
		–	not applied	GP5 Input
		1	FIFO full	GP6 Input, EXT_INT6 of the DSP
		0	FIFO not full	GP6 Input, EXT_INT6 of the DSP
		–	not applied	GP7 Input
		–	not applied	GP8 Input
01B00008	GPVAL	0xBE		GPIO Value Register, Output Value of GPIO

5. 2. 4. Memory at EMIFA, space CE0

The external RAM of the DSP has a word width of 64−bit. It is connected to the DSP via the EMIFA bus with a band width of 160 MWords per second.

Table105: Type of external Memories used on the RxControllers

Local Hex Address	Size [MByte]	Word [Byte]	Type	Bandwith [MByte/s]	Type of Controller	Identification
8000 0000 – 801F FFFF	2	8 Byte	SRAM	1280	RCtrl H12532	imbf=FFFF or 0000 and slot_brdv=XFXX or X0XX
					RCtrl embed. in AQS−Host H12547	imbf=0001

5. 2. 5. FIFO at EMIFA, space CE3

The FIFO (IDT72V3670) can store 8−KWords of 64 bits each. The multiplex logic LVDC fills the FIFO and the DSP reads the words out via EMIFA with a band width of 160 MWords per second.

Every FIFO word includes the received data of 48 bits and a time stamp of 16 bits.

Table106: Type of FIFOs used on the RxControllers

Local Hex Address	Size [KByte]	Word [Byte]	Type	Bandwith [MByte/s]	Type of Controller	Identification
B000 0000 – B00F FFF8	128	8 Byte	IDT72V3670	1280	RCtrl H12532	imbf=FFFF or 0000 and slot_brdv=XFXX or X0XX
					RCtrl embed. in AQS−Host H12547	imbf=0001

5. 2. 6. Flash Prom at the EMIFB Bus, space CE2

Access features to the BIS Flash Prom:

Bus width: 2 Byte, Data bit 7,...,0 implemented, Datenbit 15,...,8 not implemented; therefor this doubles the occupied address room

Control of access: Number of clock cycles

Duration of access ca. 85 nsec for write and 270 nsec for read access

Table107: Type of Flash Proms used on the RxControllers

Local Hex Address	Size [KByte]	Word [Byte]	Type	Type of Controller	Identification
6800 0000 – 6801 FFFF	64	1 Byte		RCtrl H12532	imbf=FFFF or 0000 and slot_brdv=XFXX or X0XX
Flash Prom is part of AQS–Host H12547 and not connected to DSP of RCtrl		1 Byte		RCtrl embed. in AQS–Host H12547	imbf=0001

5. 2. 7. Registers at the EMIFB Bus, space CE0

All registers are accessed via the EMIFB bus.

Access features to the registers:

Bus width: 2 Byte, Data bit 15,...,0 implemented

Control of access: Ready controlled

Duration of access ca. 144 nsec for write and 120 nsec for read access

Address Layout

Table108: Device Codes on EMIFB (CE0 space), existent on RCtrl

Register	Local Address	Function	Mode R/W	Bits
ctrl	60000000	Control Register	W	1, 0
fifores	60000004	FIFO Reset	W	–
sts	60000008	Status Register	R	15–0
channel	6000000A	Channel Register	R/W	3–0
chanconf	60000030	Channel Configuration	R	15–0
slot_brdv	60000038	SLot and Board Version	R	15–0

Every read access to other addresses of the EMIFB bus than presented in this table delivers the content of the Status Register (sts).

5. 2. 7. 1. Register Description

Control Register (ctrl)

ctrl	60000000	Control Register	W	0

The receiving mode can be set by modifying these two bits.

A read of the status register (sts) delivers the current selection.

Bits	15		2	1	0
Field	Not implemented			mod1	mod0
Reset State				0	1

Table109: Control Register

Field	Value	Description
mod(1::0)		Modus of Operation
	X1	RCtrl connected to a F−Controller
	00	RCtrl connected to a G−Controller
	10	RCtrl connected to a DRU

FIFO Reset (fifores)

fifores	60000004	FIFO Reset	W	–

Writing to this register without data resets counters and flags of the FIFO and resulting in a clear of the content.

The FIFO is also cleared by Power−up and a PCI−Reset.

Channel Register (channel)

channel	6000000A	Channel Register	R/W	3−0

The channel number of the FxController to which the software wants the RCtrl to be connected to is written (by the software) into this register.

The content of this register is shown at the front display. This is advantageous in test applications with multiple RxControllers.

The register is implemented in version=2 and so on (seen in chanconf).

Bits	15		4	3	2	1	0
Field	Not implemented			chan			
Reset State				0	0	0	0

Table110: Channel Register

Field	Value	Description
chan(3::0)	0000	Reset State
	0001	Connect RxController to a FxController out of nine
	...	
	1001	

Channel Configuration Register (chanconf)

chanconf	60000030	Channel Configuration	R	15−0

The bits of the Channel Configuration Register provide information about versions, functions and options.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	Board Function			Version						FCTRL Channel			External Config. Bit			

Table111: Channel Configuration Register

Field	Value	Description
External Config. Bit (3::0)		“Board Function” specific meaning:
		On RxController:
	1111	IPSO RxController, H12532
	1110	PCI RxController, H12565
FCtrl Channel (6::5)		Indicates the FCtrl channel from 1 to 8. On TCTRL,GCtrl and RCtrl is FCtrl Channel= 0
	111	F−Controller1
	110	F−Controller2
	101	F−Controller3
	100	F−Controller4
	011	F−Controller5
	010	F−Controller6
	001	F−Controller7
	000	F−Controller8 or TCTRL GCtrl, RCtrl
Version (12::7)		“Board Function” specific meaning:
		On RxController: Version of the “LVDC” FPGA
	000001	LVDC−Version 1 on IPSO RxController (H12532), without BIS Flash Prom and without Channel Register
	000010	LVDC−Version 2 on the RxControllers with Flash and Channel Register and existent as IPSO− (H12532F1) and PCI RxController (H12565)
Board Function (15::13)		Indicates the function of the channel.
	000	TCTRL
	001	FCtrl
	010	GCtrl
	100	RCtrl

Slot−Board Vers. Register (`slot_brdv`)

`slot_brdv`	60000038	PCI SLot and Board Version of a TxController	R	15−0

This register contains the slot address in the IPSO 19”−Unit and the hardware version.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	Slot Add.				Board Revision				Board Subrevision							

Table112: Slot−Board−Version Register

Field	Value	Description
Board Revision (11::8)		4−bit number of the RCtrl board version
	0000	IPSO RxController with 2MB external RAM
	0001	IPSO RxController with 2MB external RAM and Flash
	0010	IPSO RxController with 16MB external RAM and Flash
Board Subrevision (7::0)		Identification of any Subrevision
	00000000	

Field	Value	Description
Slot–Add (15::12)		Slot address, relevant in the “IPSO 19” Unit”
	0001	Slot 1
	0010	Slot 2
	0011	Slot 3
	0100	Slot 4
	0101	Slot 5
	0110	Slot 6
	0111	Slot 7
	1000	Slot 8
	1001	Slot 9
	1111	Default at the RxController embedded in IPSO AQS Host, H12547
	1011	Default at the PCI RxController, H12565

Status Register (sts)

sts	60000008	Status Register	R	7–0

The Status register is read only. It contains the FIFO flags, the Mode control bits and the transfer error bits.

The register enters its reset state after Power–up, Reset and a Write to the fifores–address.

Bit	15	...	9	8	7	6	5	4	3	2	1	0
Fields	not applied			WERR	IR	PAF	OR	PAE	HFL	mod1	mod0	PERR
Reset State				0	0	1	1	0	1	1	0	0

Table113: Status Register

Field	Value	Description
WERR		Word Error
	1	A sequence or control bit error occurred since last FIFO reset. The cause depends on the selected mode.
IR		FIFO input ready, connected to EXT_INT6 of the DSP
	0	Input ready, FIFO not full
	1	FIFO full
PAF		PAF, Flag of FIFO almost full; threshold adjusted to 32 words
	0	The FIFO can accept less than 32 further words
	1	The FIFO can accept at least 32 further words
OR		FIFO output ready
	0	Output ready to be read, FIFO contains at least one word
	1	FIFO empty
PAE		PAE, Flag of FIFO almost empty; threshold adjusted to 32 words
	0	FIFO contains less than 33 words
	1	FIFO contains more than 32 words
HFL		FIFO Half Full Flag
	0	FIFO contains more than 4096 words
	1	FIFO contains less than 4096 words
mod(1::0)		Mode of operation
	11	reserved
	10	F–Controller Mode: RCtrl connected to a F–Controller
	00	G–Controller Mode: RCtrl connected to a G–Controller
	01	DRU Mode: RCtrl connected to a DRU
PERR		Parity Error of an input word
	1	Error since last FIFO reset

5. 3. Data Acquisition and Time Measurement

Data Acquisition
The receiving speed is 80−MWords per second from the FxController and 100−MWords per second from the DRU.

Every received data word is checked for:

- being an empty or a valid data word, resulting in acceptance or rejection
- having the correct and expected position in the sequence, result is WERR of `sts`
- having the correct parity, result is PERR of `sts`

Sequence violations or parity errors set the error flags but do not avoid storing the word in the FIFO. This is to provide a complete image of the defective sequence.

The error flags are reset at Power−up, PCI−Reset or a write access to `fifores`.

Time Measurement
Every received word sequence consists of data−words and controlling key−words and idle or empty words. The stored sequence image (in the FIFO) includes only the key−words and their affiliated following data words of different number. There are no gaps.

Here, measurement of time means, counting the time distance of each key−word from the previous one as number of receiving clock cycles.

Key−words are:

- A−words of the sequence from the F−Controller
- NG−words of the sequence from the G−Controller
- Ctrl−words of the sequence from the DRU

Setting the receiving mode in the Control Register selects the right key−words.

The time distance is measured by a 32−bit counter. The low part of the 32−bit value will be stored together with the key−word in the empty upper 16 bits of the 64−bit FIFO.
Except for stream from the DRU, the upper part of the 32−bit value will be stored together with the next data word.

The word stream from the DRU provides no possibility to store the upper part of the counter. Therefor, the measurable time capacity is reduced to a 16−bit count.

With receiving the key−word, the counter is cleared and starts counting again at zero.

The maximum measurable time distance is:

- 53,687 seconds @ 80 MHz, FxController
- 655,36 microseconds @ 100 MHz, DRU

5. 3. 1. R−Ctrl operating in F−Controller Mode

All A−words and the one B−words which follows an A−word in the next clock period will be stored. All A−words get a time stamp.

Table114: Effect of Word−ID in F−Controller Mode

Identifier	Value	Accepted	WERR	Sequential Situation	Time Measuring
WID	0	yes	−	A−Word following a B−Word	Low part of timer inserted in this A−Word and timer cleared
	1	yes	−	B−Word following an A−Word	High part of timer inserted in this B−Word

Identifier	Value	Accepted	WERR	Sequential Situation	Time Measuring
	0	yes	0→ 1	A–Word following an A–Word	Low part of timer inserted in this A–Word and timer cleared
	1	no	–	B–Word following a B–Word	counting

5. 3. 2. R–Ctrl operating in G–Controller Mode

All NG–words (Next Gradient) and all Valid–words (Gradient data words) will be stored. There are no constraints regarding, succession, number or clock period.

Every NG–word gets a time stamp measured from the preceding NG–word.

Table115: Effect of Valid and NG bit in G–Controller Mode

Identifier	Value	Accepted	WERR	Description	Time Measuring
!Valid::!NG	00	yes	0→ 1	Undefined	Low part of timer inserted in this NG–Word and timer cleared
	01	yes	–	First Valid–Word following a NG–Word	High part of timer inserted in this Valid–Word
	01	yes	–	Valid–Word after first Valid–Word following a NG–Word	counting
	10	yes	–	NG–Word following an NG–Word	Low part of timer inserted in this NG–Word and timer cleared
	10	yes	–	NG–Word following an Valid–Word	Low part of timer inserted in this NG–Word and timer cleared
	11	no	–	Idle	counting

5. 3. 3. R–Ctrl operating in DRU Mode

All control words (!Ctrl=0) and all data words (!Data=0) will be stored.

There are streams of control words and, separated by idle words, back–to–back streams of data words. Every control word gets a time stamp measured from the preceding control word. Every data word gets a time stamp measured from the last preceding control word.

Table116: Effect of Data and Control bit in DRU Mode

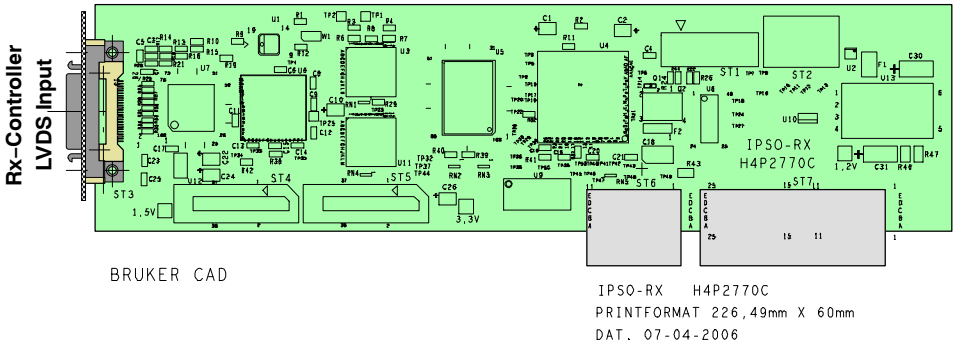
Identifier	Value	Accepted	WERR	Description	Time Measuring
!Data::!Ctrl	00	yes	0→ 1	Undefined	Low part of timer inserted in this word and timer cleared
	01	yes	–	Data–Word	Low part of timer inserted in this Data–Word, not cleared
	10	yes	–	Ctrl–Word	Low part of timer inserted in this Ctrl–Word and timer cleared
	11	no	–	Idle	counting

5. 4. Engineering Design

IPSO 19”–Unit

Form

Figure31: RxController of IPSO 19” Unit



Ports

Data Input

- Low voltage, low noise LVDS input via 8 balanced data lines and one clock line
- Transfer rate 80 to 100 million words per second
- Word width 48 bit

JTAG Structure

The implemented JTAG interface has 3 chains. JTAG is used to program the logic, read the BIS Prom and debug the DSP operation.

Table117: JTAG Structure on RxController of the IPSO 19”–Unit

Connector	Stxxx		
JTAG Bridge	Uxx, Addr=yy		
Connector	–	ST??	ST??
JTAG Chain	**Chain1**	**Chain2**	**Chain3**
Devices		Uxx:DSP	Uxx:FIFO1
			Uxx:FIFO2
			Uxx:FPGA
			Uxx:EEPROM (FPGA)

Requirements of Power

Table118: Currents

Part–No.	Assembly	+5V	+3,3V	+12V	+5VSB	–12V
H12532xx	RxController	0,6 A	0	0	0	0

5. 5. Pin allocation of Connectors

LVDS Input Connector

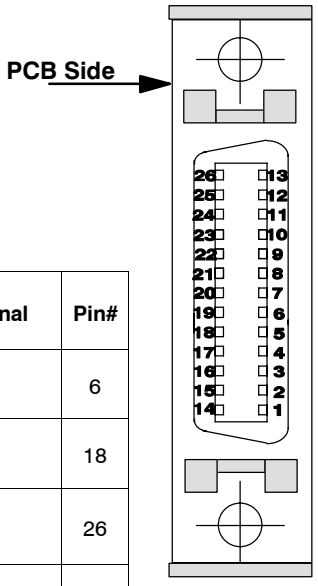


Figure32: Pin location of the 48–Bit LVDS Connector at PCB

Table119: Cable and Pin Assignment

Function	Type of Wire	Transmitter Signal	Receiver Signal	Pin#
signal: Differential Pair of the received serial transmit clock connected to the corresponding inputs of the transmitter	twisted + shielded	TxCLK_P	RxCLK_P	6
		TxCLK_M	RxCLK_M	18
shield: Common drain wire of all separate shields, connected to CHASSIS		LVDS Gnd		26
signal: Differential Pair of the received serial data stream connected to the corresponding inputs of the transmitter	twisted + shielded	TxIN_P0	RxIN_P0	3
		TxIN_M0	RxIN_M0	15
shield		LVDS Gnd		26
signal	twisted + shielded	TxIN_P1	RxIN_P1	4
		TxIN_M1	RxIN_M1	16
shield		LVDS Gnd		26
signal	twisted + shielded	TxIN_P2	RxIN_P2	5
		TxIN_M2	RxIN_M2	17
shield		LVDS Gnd		26
signal	twisted + shielded	TxIN_P3	RxIN_P3	9
		TxIN_M3	RxIN_M3	21
shield		LVDS Gnd		26
signal	twisted + shielded	TxIN_P4	RxIN_P4	10
		TxIN_M4	RxIN_M4	22
shield		LVDS Gnd		26
signal	twisted + shielded	TxIN_P5	RxIN_P5	11
		TxIN_M5	RxIN_M5	23
shield		LVDS Gnd		26
signal	twisted + shielded	TxIN_P6	RxIN_P6	12
		TxIN_M6	RxIN_M6	24
shield		LVDS Gnd		26

Function	Type of Wire	Transmitter Signal	Receiver Signal	Pin#
signal	twisted + shielded	TxIN_P7	RxIN_P7	13
		TxIN_M7	RxIN_M7	25
shield		LVDS Gnd		26
USB signal pair, left open	twisted + shielded	USB+		1
		USB–		14
Shield of the USB signal pair, connected to CHASSIS		USB Gnd		2
signal: left open	individual	CHANNEL_DETECT0		7
signal: left open	individual	CHANNEL_DETECT1		20
VCC of USB power, left open	individual	USB pwr		19
GND of USB power, connected to GND	individual	USB gnd		8
common shield of the entire bundle	Shield	CHASSIS		body

CHASSIS:

Chassis is a separate plane in the PCB layer stack. This plane is stacked close by the ground plane, giving a very tight capacitive (only capacitive) and low inductance coupling to GND. The chassis plane is screwed together with the external chassis along the front edge near the connectors and the line drivers.

This solution reduces the digital noise at that point and the noise which is picked up by the driver and carried to the outside. In addition this avoids parasitic current through the GND plane which could be caused by potential differences of the remote device.

DS_OPT, Deskew optimization:

DS_OPT of the transmitter is triggered after power up and under software intervention.
At the receiver this pin should be configurable to High or Low which would enable or disable the receiver to optimize the skews.

End of Document

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