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PCI R-Cntrl

PCI Rx Controller
Technical Manual

Version 001

think forward

NMR Spectroscopy

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DWG-Nr.: Z4D10605 - 001

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Contents

Introduction 1

The PCI Rx–Controller called PCI R–Cntrl with part number H12565 is a standard PCI expansion card. It is able to receive the data streams sent by:

- the Tx–Controllers configurated as F–Controller or as G–Controller;
- the DRU–M, part number Z105987.

The R–Cntrl is supervised by its software driver running under LINUX and utilized by the test programs of the “ipsotest”. Therefore it has to be mounted in the PCI environment of “IPSO Host”. This can be accomplished by using a PCI StarGen Bridge and an external PCI Box both delivered from “Hartmann Elektronik” (www.hardmann–elektronik.de), see below.

The mounted PCI R–Cntrl operate as the second R–Controller and so on, additionally to the built–in R–Controller in slot 1 of the “IPSO 19” Unit” or onboard of “IPSO AQS”.

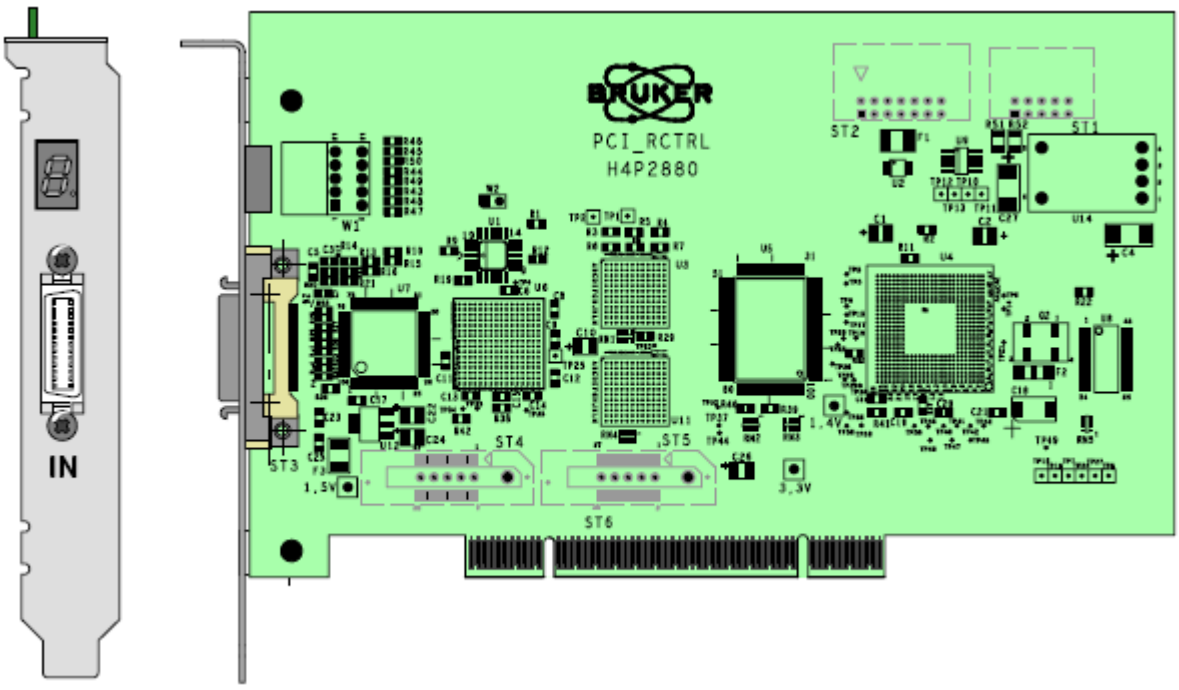

Figure 1.1. Rx-Controller Front and Top View

Features

- The Rx–Controller is able to receive 48–bit words via its LVDS input at a clock rate of 80 MHz if connected to a Tx controller and at a rate of 100 MHz if connected to a DRU–M.
- Rx measures the time distance of each Tx A–Word from the previous one and stores this value as a number of receive clock cycles in the upper 16–Bit of the 64–Bit receive FIFO.
- Receive FIFO for 8k Words of 64 bit connected to the EMIFA bus of the DSP
- 64–bit DSP TMS320C6415 with 1MByte on chip RAM, EMIFA, EMIFB, SDRAM and PCI–32Bit/33Mhz, interface.
- External RAM of 2MByte/16MByte connected to the EMIFA bus.
- EMIFA data band with of 160M Words of 64 bits.
- Separate EMIFB bus for control functions.
- FLASH PROM with board and revision information.

PCI Conditions *1.1*

Type of PCI Bus:	32 bit/ 33 MHz.
Length of the card:	Short, 176 mm.
PCI functions:	Single.
Number of interrupts:	One at IntA, pin A6.
PCI signal voltage:	The PCI R–Cntrl can be used in an 3.3 V environment. Received PCI signals have to be of 3.3 V–signaling. The PCI interface of the DSP is not 5 V tolerant. The level of PCI signals sent by the R–Cntrl are also between 0 and 3.3 V. This is why the PCI R–Cntrl should not be mounted in the 5 V–PCI slots of the “IPSO 19” Unit” or “IPSO AQS”.

Safety and Handling *1.2*

- Handling under ESD safety conditions is necessary. Don’t touch uncovered metal of PCB and connectors before discharging yourself!
- Do not connect a receiver to the LVDS connector of the controller in slot 2 of the IPSO 19” Unit. There will never be valid data.
- A LVDS cable should never be removed from or connected to a powered controller. Corrupted data could be sampled as valid.
- Do not connect more than one gradient amplifier to the same system.

Installing the PCI R-Controller *1.2.1*

Mounting the PCI R–Controller requires the following accessories:

Table 1.1. Accessories Required for Mounting the PCI R-Controller

Part Number	Drawing Number	Description
	LMH0 000 041 (LMB2200010)	Star Fabric PCI Extension Box, 3.3 V
	1H00 001 712 (1H00 001 7109)	Star Fabric PCI Bridge, 3.3 V
	F006.01305	Cat 5 RJ45–Cable, 5 meter
86868		48–Bit LVDS–Cable, 1 meter

The PCI R–Controllers have to be mounted in the external PCI extension box.

Because the RX–controller is a 3.3 V device, the extension box had to be configured to work with 3.3 V.

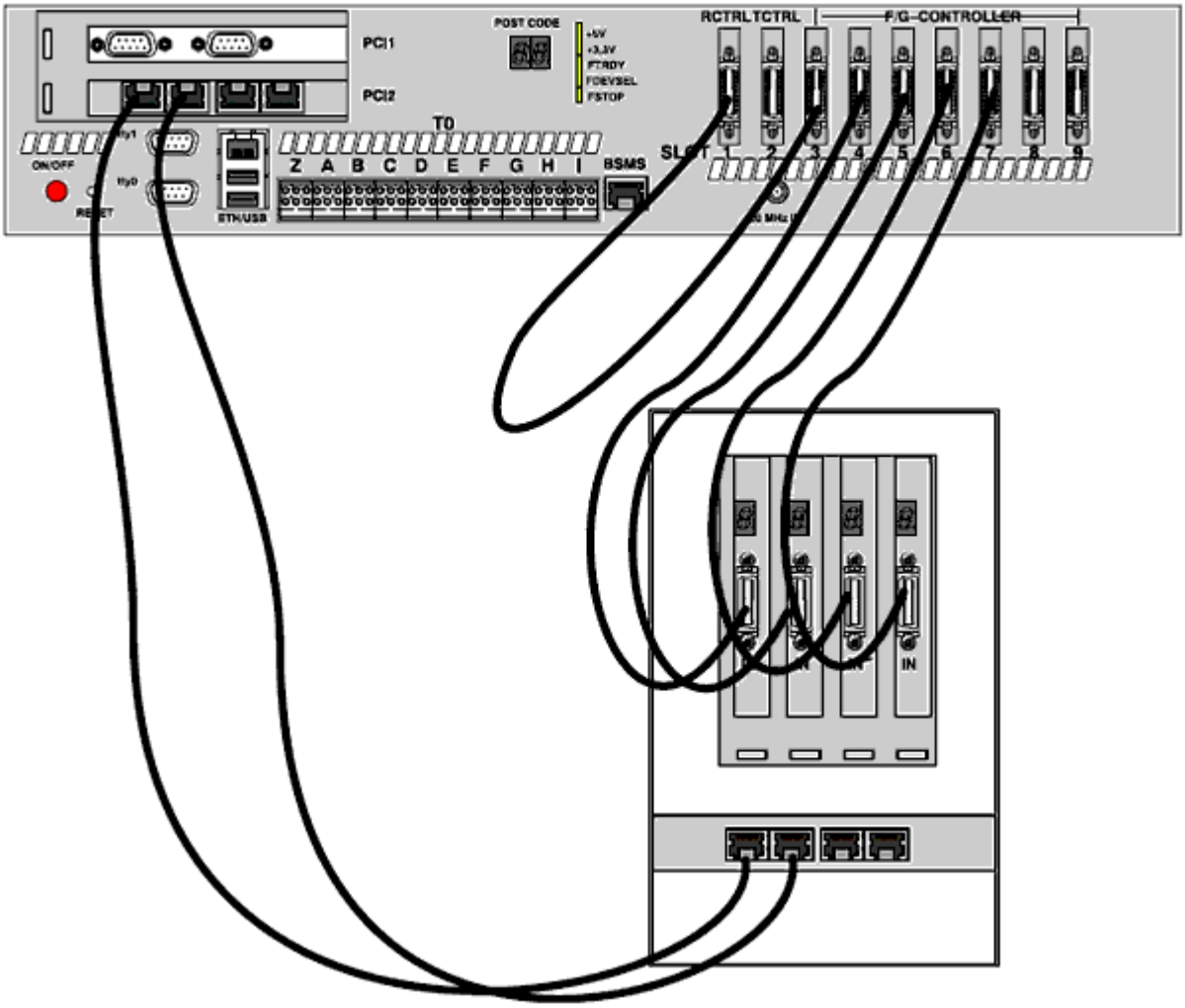

Figure 1.2. Connecting the External PCI Box to the IPSO

Checking the PCI Architecture after Booting with Linux

While booting, Linux checks the PCI topology and allocates a base address and a channel number to each R–Cntrl. The allocated number is indicated in the LED display. The default configuration can be changed in the ipsotest.

The Channel Display *1.3*

To get more oversight for wiring the R–Cntrl and T–Cntrl, the R–Cntrl indicates its logical number of channel. When Linux booting is completed, normally every controller indicates a different number. If a controller does not indicate a number, the R–Cntrl was not recognized as a known device.

The decimal point in the display indicates the correct FPGA firmware was loaded after power-up.

Ports *1.4*

LVDS Connector

The receiving data words enter the Rx-Controller via a LVDS interface with the following features:

- Input via 8 low voltage, low noise LVDS data lines and one clock line pair.
- Operating transfer rates of 80 to 100M words per second.
- Word width of 48 bits.

Currents and Voltages *1.5*

Table 1.2. Currents and Voltages

Part Number	+5 V	+3.3 V	+12 V	+5 V SB	-12 V
H12565	0	0.6 A	0	0	0

Disclaimer *1.6*

The PCI Rx-Controller should only be used for its intended purpose as described in this manual. Use of the controller for any purpose other than that for which it is intended is taken only at the users own risk and invalidates any and all manufacturer warranties.

Service or maintenance work must be carried out by qualified personnel.

Read this manual before operating the controller and corresponding unit. Pay particular attention to any safety related information.

Warnings and Notes 1.7

There are two types of information notices used in this manual. These notices highlight important information or warn the user of a potentially dangerous situation. The following notices will have the same level of importance throughout this manual.

Note: Indicates important information or helpful hints

WARNING: Indicates the possibility of severe personal injury, loss of life or equipment damage if the instructions are not followed.

Contact for Additional Technical Assistance 1.8

For further technical assistance on the BPSU36-2 unit, please do not hesitate to contact your nearest BRUKER dealer or contact us directly at:

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Reference Numbers

2

Table 2.1. Parts and Assemblies

Lower Group			Upper Group	
Part Number	**Drawing Number**	**Description**	**Part Number**	**Description**
H12564	H4P2880	PCI RxC PCB	H12565	PCI Rx-Controller
H12564F1	H4P2880A	PCI RxC PCB-long		Test version

Table 2.2. Accessories

Part Number	Drawing Number	Description
86868		48-Bit LVDS Cable, 1 meter

Production Status and Modifications 3

Introductory Status of the Product 3.1

Table 3.1. Introductory Status

Part Number	Name	Layout Number	Modification	Program File	Firmware	Jumper Setting
					no	no

Prog File

The name of the program file includes the layout number and the EC level.

Modifications of the Introduced Assemblies 3.1.1

Jumper Setting

There are no jumpers to be set or which can be erroneously modified.

PCI Bus

INT_A is used.

Firmware

There is no firmware stored on the Rx-Controller.

Modification History 3.2

No modifications have been made to date.

Description 4

Versions

Location	Name	Part Number	EC Number	Firmware	Increments	Software Requirements
PCI Bus	PCI Rx-Controller	H12565			Flash	

Concerned

Part Number 86868 LVDS Cable, 1 meter

Part Number Z105987 DRU-M

Architecture

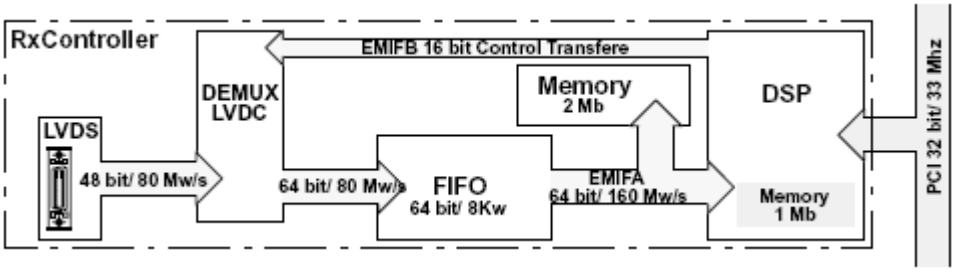


Figure 4.1. The Rx-Controller

Operation

The Rx-Controller is designed to receive data words of 48-bits sent by the IPSO Tx-Controller or the DRU.

These data words are received on 8 line pairs in a serialized form. They are transferred to parallel words in the LVDS receiver and delivered to the LVDC (FPGA) at a clock rate of 80 MHz (FCtrl, GCtrl) or 100 MHz (DRU). In the LVDC, the words are checked (validity and parity) and assigned with a time stamp fed into the FIFO. In case of a parity error, the parity flag in the status registries set and hold up to the FIFO will be cleared.

The 3 possible data sources (FCtrl, GCtrl, DRU) send in different formats. Therefor, 3 receiving modes have been implemented in the LVDC and selected depending on the recognized source.

The 48-bit words are stored in a FIFO which is 64-bit wide. The upper 16-bits of the FIFO words are used to hold the time stamps of each word. This time informa-

tion gives the distance to the preceding word measured in numbers of clocks. The type of words which are measured and get the stamp depend on the receiving mode.

In the FCtrl mode the A-words are used. In the GCtrl mode the distance between two NG words is counted. In the DRU mode, the counting starts with each Control Word and ends at the following Control or Data Word.

The FIFO words can be processed by the DSP, transferred to its local memory or via the PCI Bus.

The control and status register can be accessed by the DSP via the EMIFB bus. All registers and both memories of the Rx-Controller can also be accessed by any other controller via the PCI Bus.

Structure of Input Words at the LVDS Receiver and the FIFO *4.1*

Depending on the connected data source and the associated receiving mode, the Rx-Controller checks the validity and the parity of the incoming words (A, B words in FCtrl mode; Gradient data and NG words in GCtrl mode; Data and Control words in DRU mode).

The resulting error status and the FIFO status can be read on the EMIFB bus.

Words from F–Controller *4.1.1*

A data package from the F-Controller consists of 2 Words (A+B) in adjacent clock cycles. The TIME value in the upper 16 bits of the FIFO word is the number of clock cycles between the previous A-Word and this one.

Table 4.1. F–Controller words at output of LVDS receiver and FIFO (F–Controller Mode)

Bit		64	---	49	48	47	46	45	---	1
Word A	At LVDS	not used			PAR	SYNC	WID	Data from F-Controller		
Word B		not used			PAR	SYNC	WID	Data from F-Controller		
Word A	At FIFO	TIME value, low part			PAR	SYNC	WID	Data from F-Controller		
Word B		TIME value, high part			PAR	SYNC	WID	Data from F-Controller		

Table 4.2. Bit Fields of the F–Controller Output Word

Field	Value	Description
WORD_ID (WID)	0 1	46-bit in every word Word A Word B
SYNC		Reflects the current state of the 20 MHz reference clock at transmitter.
PARITY		Even parity bit, created form bit 1 to 46.

Words from G-Controller *4.1.2*

A Gradient switching package from the G–Controller consists of a variable number of Gradient data words and 1 Next Gradient word. Usually, these words are transmitted in adjacent clock cycles but this is not necessary.

The TIME value in the upper 16 bits of the FIFO word is the number of clock cycles between the previous Next Gradient word and this one.

Table 4.3. G–Controller Words at Output of LVDS Receiver and FIFO (G–Controller Mode)

Bit		64	---	49	48	47	---	3	2	1
Next Gradient	At LVDS	Not applied			Parity	Not allocated			!VALID	!NG
Gradient Data		Not applied			Parity	Gradient			!VALID	!NG
Next Gradient	At FIFO	TIME value, low part			Parity	Not allocated			!VALID	!NG
Gradient Data		TIME value, high part			Parity	Gradient			!VALID	!NG

Table 4.4. Bit Fields of the F–Controller Output Word

Field	Value	Description
!VALID:!NG	 00 01 10 11	These bits identify the Gradient data words and the Next–Gradient words which activate the Gradients transmitted since the previous Next–Gradient word Not allowed, erroneous combination Gradient data word Next–Gradient word Idle cycle without data
PARITY		The even parity bit, created from bit 1 to bit 47.

Words from the DRU *4.1.3*

Table 4.5. DRU Words at Output of LVDS Receiver and FIFO (DRU Mode)

Bit		63	---	48	47	46	---	2	1	0
DRU Control Word	At LVDS	Not applied			Parity	DRU Control Information			1	0
DRU Data Word		Not applied			Parity	DRU Data			0	1
DRU Control Word	At FIFO	TIME value, low part			Parity	DRU Control Information			1	0
DRU Data Word		TIME value, high part			Parity	DRU Data			0	1

Table 4.6. Bit Fields of the DRU–Controller Output Word

Field	Value	Description
!Data..!Ctrl		These bits identify the DRU data words and the control words (Data and Header/Trailer information
	00 01 10 11	Not allowed, erroneous combination Data word Control word Idle cycle without data
PARITY		The even parity bit, created form bit 1 to 47.

Software Interface *4.2*

Nearly all resources of the Rx-Controller can be accessed by both software running locally or software running on the host controller. Only the FIFO is excluded from this. The FIFO can be accessed by the DSP only.

Both address ranges, local DSP and global PCI bus, are defined by 32-bit addresses. The access from the PCI range into many local ranges is possible through address windows, two dedicated to each controller. These include a 4 MB window (for prefetchable accesses) and a 8 MB window (for non-prefetchable accesses). The segmentation of the PCI address range to the window spaces the controllers is carried out by the BIOS and fixed by defining the content of all PCI base registers.

Every window can be moved through the local address range by modifying the content of the DSP page register (DSPP).

PCI Addresses 4.2.1

The content of the Base 0 register is defined by the BIOS of the host controller.

The content of the DSPP register can be written by the software running on the host controller.This register can be reached through the nonprefetchable window.

Table 4.7. Relations Between PCI and Local Addresses on R-Controllers

	4 MB Prefetchable Range		8 MB Nonprefetchable Range	
	Bit [31..22]	Bit [21..0]	Bit [31..23]	Bit [22..0]
PCI Address	<Base0>	AD [21..0]	<Base1>	AD [22..0]
Local Address	<DSPP>		0000 0001 1	

Local Address Layout 4.2.2

Table 4.8. Memory Map of the DSP 6415

Local Hex Address Range	Block Size (Bytes)	Bus	Data Bus Width (Bytes)	Description	Utilization
000x xxxx	1M	Internal	8	On chip RAM	
0180 0000 – 0183 FFFF	256K	Internal		EMIFA Config. Register	
0184 0000 – 0187 FFFF	256K	Internal		L2 Cache Config. Register	
0194 0000 – 0197 FFFF	256K			Timer 0 Register	
0198 0000 – 019B FFFF	256K			Timer 1 Register	
019C 0000 – 019F FFFF	256K			Interrupt Select Register	
01A0 0000 – 01A3 FFFF	256K			Enhanced DMA Register	
01A8 0000 – 01AB FFFF	256K	Internal		EMIFB Config Register	
01AC 0000 – 01AF FFFF	256K	Internal		Timer 2 Register	
01B0 0000 – 01B3 FFFF	256K	Internal		GPIO Register	
01C0 0000 – 01C3FFFF	256K			PCI Register	
6000 0000 – 63FF FFFF	64M	EMIFB CE0	2	External RAM	Register

Table 4.8. Memory Map of the DSP 6415

Local Hex Address Range	Block Size (Bytes)	Bus	Data Bus Width (Bytes)	Description	Utilization
6400 0000 – 67FF FFFF	64M	EMIFB CE1	2	External RAM	
6800 0000 – 6BFF FFFF	64M	EMIFB CE2	2	External RAM	
6C00 0000 – 6FFF FFFF	64M	EMIFA CE3	2	External RAM	FIFO 16K x 64
8xxx xxxx	256M	EMIFA CE0	8	External RAM	RAM
9xxx xxxx	256M	EMIFA CE1	8	External RAM	
Axxx xxxx	256M	EMIFA CE2	8	External RAM	
Bxxx xxxx	256M	EMIFB CE3	8	External RAM	FIFO 16K x 64

Content of the DSP Configuration Registers *4.2.3*

Table 4.9. EMIFA Configuration Register

Local Hex Address	Acronym	Value	Description
1800048	CE0SEC	00000042	EMIFA CE0 Space Secondary Control
1800044	CE1SEC	unmodified	EMIFA CE1 Space Secondary Control
1800050	CE2SEC	unmodified	EMIFA CE2 Space Secondary Control
1800054	CE3SEC	00000040	EMIFA CE3 Space Secondary Control
1800000	GBLCTL	00012724	EMIFA Global Control Rx-Controller with 2 MB SRAM
1800008	CE0CTL	FFFFFFE3	EMIFA CE0 Space Control Rx-Controller with 2 MB SRAM
1800004	CE1CTL	unmodified	EMIFA CE1 Space Control, not used
1800010	CE2CTL	unmodified	EMIFA CE2 Space Control, not used
1800014	CE3CTL	FFFFFFE3	EMIFA CE3 Space Control, FIFO
1800018	SDCTL	0248f000	EMIFA SDRAM Control Rx-Controller with 2 MB SRAM
180001C	SDTIM	003F05DC	EMIFA SDRAM Refresh Control Rx-Controller with 2 MB SRAM
1800020	SDEXT	00175F3F	EMIFA SDRAM Extension Rx-Controller with 2 MB SRAM

Table 4.10. EMIFB Configuration Register

Local Hex Address	Acronym	Value	Description
1A80000	GLBCTL	00012324	EMIFB Global Control
1A80008	CE0CTL	5055C11D	EMIFB CE0 Space Control, Register
1A80004	CE1CTL	FFFFFFBF	EMIFB CE1 Space Control, not used
1A80010	CE2CTL	2A22E80A	EMIFB CE2 Space Control, BIS Flash Prom
1A80014	CE3CTL	FFFFFFBF	EMIFB CE3 Space Control, not used

Table 4.11. GPIO Configuration Register

Local Hex Address	Acronym	Value	Used As	Description
01B00000	GPEN	0x1FF		GPIO Bit Enable; Use of the GPIO Pins GP0, ..., GP8 as IO Pins
01B00004	GPDIR	0xE		Direction of GPIO pins adjusted as:
		-	not applied	GP0 Input
		-	not applied	GP1 Output
		-	not applied	GP2 Output
		-	MCBSP2 enable of serial PCI Config Prom	GP3 Output
		-	not applied	GP4 Input
		-	not applied	GP5 Input
		1	FIFO full	GP6 Input, EXT_INT6 of the DSP
		0	FIFO not full	GP6 Input, EXT_INT6 of the DSP
		-	not applied	GP7 Input
		-	not applied	GP8 Input
01B00008	GPVAL	0xBE		GPIO Value Register, Output Value of GPIO

Memory at EMIFA, Space CE0 *4.2.4*

The external RAM of the DSP has a word width of 64-bit. It is connected to the DSP via the EMIFA bus with a band width of 106 MWords per second.

Table 4.12. Type of External Memory used on the RX-Controllers

Local Hex Address	Size (MB)	Word (Byte)	Type	Bandwidth (MB/s)	Type of Controller	Identification
8000 0000 – 801F FFFF	2	8	SRAM	1280	RCTRL H12532 RCTRL embedded in AQS Host H12547	imbf=FFFF or 0000 and slot_brdv=XFXX or X0XX imbf=0001

FIFO at EMIFA, Space CE3 *4.2.5*

The FIFO (IDT72V3670) can store 8K Words of 64-bits each. The multiplex logic LVDC fills the FIFO and the DSP reads the words out via EMIFA with a bandwidth of 106 MWords per second.

Every FIFO word includes the received data of 48-bits and a time stamp of 16-bits.

Table 4.13. Type of FIFOs used on the RX-Controllers

Local Hex Address	Size (KByte)	Word (Byte)	Type	Bandwidth (MB/s)	Type of Controller	Identification
B000 0000 – B00F FFF8	128	8	IDT72V 3670	1280	Rx CTRL H12532 Rx CTRL embedded in AQS Host H12547	imbf=FFFF or 0000 and slot_brdv=XFXX or X0XX imbf=0001

Flash Prom at the EMIFB Bus, Space CE2 *4.2.6*

Access features to the BIS Flash Prom:

Bus Width: 2 byte, data bit 7, ..., 0 implemented, data bit 15, ..., 8 not implemented; therefore this doubles the occupied address room.

Control of access: Number of clock cycles.

Duration of Access: 85 ns for write and 270 ns for read access.

Table 4.14. Type of FIFOs used on the RX-Controllers

Local Hex Address	Size (KB)	Word (Byte)	Type	Type of Controller	Identification
6800 0000 – 6801 FFFF	64	1		RCTRL H12532	imbf=FFFF or 0000 and slot_brdv=XFXX or X0XX
Flash Prom is part of AQS Host H12547 and not connected to the DSP of the RCTRL		1		RCTRL embedded in AQS Host H12547	imbf=0001

Registers at the EMIFB Bus, Space CE0 *4.2.7*

All registers are accessed via the EMIFB bus.

Access features to the registers:

Bus Width: 2 byte, data bit 15, ..., 0 implemented.

Control of access: Ready controlled.

Duration of Access: Ca. 144 ns. for write and 120 nest. for read access.

Address Layout

Table 4.15. Device Codes on EMIFB (CE0 space), Existent on RCTRL

Register	Local Address	Function	Mode R/W	Bits
ctrl	60000000	Control Register	W	1, 0
fifores	60000004	FIFO Reset	W	---
sts	60000008	Status Register	R	15-0
channel	6000000A	Channel Register	R/W	3-0
chanconf	60000030	Channel Configu-ration	R	15-0
slot_brdv	60000038	Slot and Board Version	R	15-0

Every read access to other addresses of the EMIFB bus than presented in this table delivers the content of the Status Register (sts).

Register Description *4.2.7.1*

Control Register (ctrl)

Register	Local Address	Function	Mode R/W	Bits
ctrl	60000000	Control Register	W	0

The receiving mode can be set by modifying these two bits.

A read of the status register (sts) delivers the current selection.

Bits	15		2	1	0
Field	Not implemented			mod1	mod0
Reset State				0	1

Table 4.16. Control Register

Field	Value	Description
mod (1..0		Modus of Operation
	X1	RCTRL connected to a F-Controller
	00	RCTRL connected to a G-Controller
	10	RCTRL connected to a DRU

FIFO Reset (fifores)

Register	Local Address	Function	Mode R/W	Bits
fifores	60000004	FIFO Reset	W	-

Writing to this register without data resets counters and flags of the FIFO and resulting in a clear of the content. A pending parity error bit is also cleared.

The FIFO is also cleared with a power-up and a PCI reset.

Control Register (ctrl)

Register	Local Address	Function	Mode R/W	Bits
channel	6000000A	Channel Register	R/W	3-0

The channel number of the Fx-Controller to which the software wants the RCtrl to be connected to is written (by the software) into this register.

The content of this register is shown at the front display. This is advantageous in test applications with multiple Rx-Controllers.

The register is implemented in version = 2 and so on (seen in chanconf).

Bits	15		4	3	2	1	0
Field	Not implemented			chan			
Reset State				0	0	0	0

Table 4.17. Channel Register

Field	Value	Description
chan (3..0	0000	Reset State
	0001...1001	Connect Rx-Controller to a Fx-Controller out of nine.

Channel Control Register (chanconf)

Register	Local Address	Function	Mode R/W	Bits
chanconf	60000030	Channel Configuration	R	15-0

The bits of the Channel Configuration Register provide information about versions, functions and options.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	Board Function			Version						FCtrl Channel			External Config. Bit			

Table 4.18. Channel Configuration Register

Field	Value	Description
External Config. Bit (3..0		„Board Function” specific meaning:
		On Rx-Controller:
	1111	IPSO Rx-Controller, H12532
	1110	PCI Rx-Controller, H12565
FCTRL Channel (6..5)		The FCTRL channels are labeled 1 to 8. By TCTRL, GCTRL and RCTRL is FCTRL channel = 0.
	111	F-Controller 1
	110	F-Controller 2
	101	F-Controller 3

Table 4.18. Channel Configuration Register

Field	Value	Description
	100	F-Controller 4
	011	F-Controller 5
	010	F-Controller 6
	001	F-Controller 7
	000	F-Controller 8 or TCTRL, GCTRL, RCTRL
Version (12..7)		„Board Function" specific meaning:
		On Rx-Controller: Version of the ‚LVDC' FPGA
	000001	LVDC Version 1 on IPSO Rx–Controller (H12532), without BIS Flash Prom and without Channel Register
	000010	LVDC Version 2 on the Rx–Controllers with Flash and Channel Register and existent as IPSO– (H12532F1) and PCI Rx–Controller (H12565)
Board Function (15..13)		Labels the function of the channels.
	000	TCTRL
	001	FCTRL
	010	GCTRL
	100	RCTRL

Slot Board Version Register (slot_brdv)

Register	Local Address	Function	Mode R/W	Bits
slot_brdv	60000038	PCI Slot and Board Version of a Tx-Controller	R	15-0

This register contains the slot address in the IPSO 19" Unit and the hardware version.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	Slot Address				Board Revision				Board Sub-revision							

Table 4.19. Slot Board Version Register

Field	Value	Description
Board Revision (11..8)		4-Bit labeling of the board version to differentiate the boards with the various hardware.
	0000	IPSO Rx-Controller with 2 MB external RAM.
	0001	IPSO Rx-Controller with 2 MB external RAM and Flash.
	0010	IPSO Rx-Controller with 16 MB external RAM and Flash.
Board Sub-revision (7..0)	00000000	Labeling of the sub-revision, e.g. new EC due to a software relevant error.
Slot-Add (15..12)		Gives the slot of the controller, relevant in the IPSO 19” Unit.
	0001	Slot 1
	0010	Slot 2
	0011	Slot 3
	0100	Slot 4
	0101	Slot 5
	0110	Slot 6
	0111	Slot 7
	1000	Slot 8
	1001	Slot 9
	1111	Default at the Rx–Controller embedded in IPSO AQS Host, H12547
	1011	Default at the PCI Rx–Controller, H12565

Status Register (sts)

Register	Local Address	Function	Mode R/W	Bits
sts	60000008	Status Register	R	7-0

The status register is read only. It contains the FIFO flags, the mode control bits and the transfer error bits.

The register enters its reset state after power-up, reset and a write to the **fifores** address.

Bit	15	---	9	8	7	6	5	4	3	2	1	0
Fields	Not applied			WERR	IR	PAF	OR	PAE	HFL	mod1	mod0	PERR
Reset State				0	0	1	1	0	1	1	0	0

Table 4.20. Status Register

Field	Value	Description
WERR		Word Error
	1	A sequence or control bit error occurred since last FIFO reset. The cause depends on the selected mode.
IR		FIFO input ready, connected to EXT_INT6 of the DSP.
	0	Input ready, FIFO not full.
	1	FIFO full.
PAF		PAE, Flag of FIFO almost empty; threshold adjusted to 32 words.
	0	FIFO contains less than 33 words.
	1	FIFO contains more than 32 words.
HFL		FIFO Half Full Flag.
	0	FIFO contains more than 4096 words.
	1	FIFO contains less than 4096 words.
mod (1..0)		Mode of operation.
	11	Reserved
	10	F–Controller Mode: Rx CTRL connected to a F–Controller.
	00	G–Controller Mode: Rx CTRL connected to a G–Controller.
	01	DRU Mode: Rx CTRL connected to a DRU.

Table 4.20. Status Register

Field	Value	Description
PERR		Parity error of an input word.
	1	Error since last FIFO reset.

Data Acquisition and Time Measurement *4.3*

Data Acquisition

The receiving speed is 80 MWords per second from the Fx-Controller and 100 MWords per second from the DRU.

Every received data word is checked for:

- being an empty or a valid data word, resulting in acceptance or rejection
- having the correct and expected position in the sequence, result is WERR of sts
- having the correct parity, result is PERR of sts.

Sequence violations or parity errors set the error flags but do not avoid storing the word in the FIFO. This is to provide a complete image of the defective sequence.

The error flags are reset at power-up, PCI reset or a write access to **fifores**.

Time Measurement

Every received word sequence consists of data words and controlling keywords and idle or empty words. The stored sequence image (in the FIFO) includes only the keywords and their affiliated following data words of different number. There are no gaps.

Here, measurement of time means, counting the time distance of each keyword from the previous one as number of receiving clock cycles.

Keywords are:

- A-words of the sequence from the F-Controller.
- NG-words of the sequence from the G-Controller.
- Ctrl-words of the sequence from the DRU.

Setting the receiving mode in the Control Register selects the right keywords.

The time distance is measured by a 32-bit counter. The low part of the 32-bit value will be stored together with the keyword in the empty upper 16-bits of the 64-bit FIFO. Except for stream from the DRU, the upper part of the 32-bit value will be stored together with the next data word.

The word stream from the DRU provides no possibility to store the upper part of the counter. Therefore, the measurable time capacity is reduced to a 16-bit count.

With receiving the keyword, the counter is cleared and starts counting again at zero.

The maximum measurable time distance is:

- 53.687 seconds @ 80 MHz, Fx-Controller
- 655.36 microseconds @ 100 MHz, DRU.

R–Ctrl Operating in F–Controller Mode *4.3.1*

All A-words and the one B-words which follows an A-word in the next clock period will be stored. All A-words get a time stamp.

Identifier	Value	Accepted	WERR	Sequential Situation	Time Measuring
WID	0	Yes	---	A-Word following a B-Word	Low part of timer inserted in this A-Word and timer cleared.
	1	Yes	---	B-Word following an A-Word	High part of timer inserted in this B-Word
	0	Yes	0->1	A-Word following an A-Word	Low part of timer inserted in this A-Word and timer cleared
	1	No	---	B-Word following a B-Word	Counting

R–Ctrl Operating in G–Controller Mode *4.3.2*

All NG words (Next Gradient) and all valid words (gradient data words) will be stored. There are no constraints regarding, succession, number or clock period.

Every NG word gets a time stamp measured from the preceding NG word.

Identifier	Value	Accepted	WERR	Sequential Situation	Time Measuring
!Valid..!NG	00	Yes	0->1	Undefined.	Low part of timer inserted in this NG word and timer cleared.
	01	Yes	---	First valid word following a NG word.	High part of timer inserted in this valid word.
	01	Yes	---	Valid word after first valid word following a NG word.	Counting.
	10	Yes		NG word following an NG word.	Low part of timer inserted in this NG word and timer cleared.
	10	Yes		NG word following a Valid word.	Low part of timer inserted in this NG word and timer cleared.
	01	No	---	Idle.	Counting.

R-CTRL Operating in DRU Mode *4.3.3*

All control words (!Ctrl=0) and all data words (!Data=0) will be stored.

There are streams of control words and, separated by idle words, back-to-back streams of data words. Every control word gets a time stamp measured from the preceding control word. Every data word gets a time stamp measured from the last preceding control word.

Identifier	Value	Accepted	WERR	Sequential Situation	Time Measuring
!Data..!Ctrl	00	Yes	0->1	Undefined.	Low part of timer inserted in this word and timer cleared.
	01	Yes	---	Data word.	Low part of timer inserted in this data word, not cleared.
	10	Yes	---	CTRL word.	Low part of timer inserted in this CTRL word and timer cleared.
	11	No	---	Idle.	Counting.

Engineering Design *4.4*

Dimensions

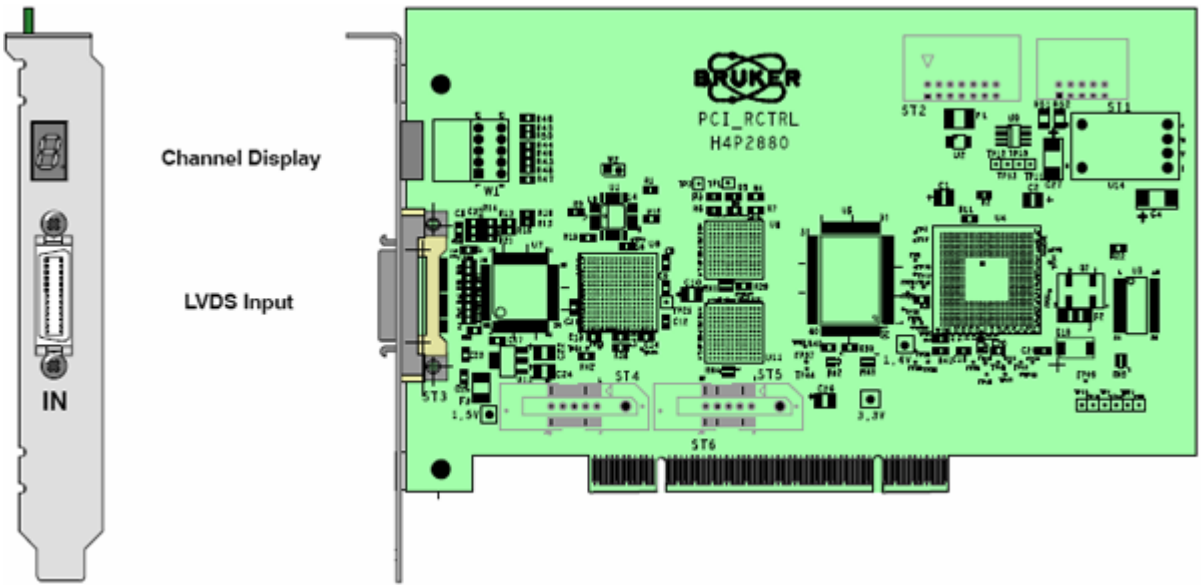


Figure 4.2. PCI Rx-Controller

Ports

Data Input

- Low voltage, low noise LVDS input via 8 balanced data lines and one clock line.
- Transfer rate 80 to 100 million words per second.
- Word width 48-bit.

JTAG Structure

The implemented JTAG interface has 3 chains. JTAG is used to program the logic, read the BIS Prom and debug the DSP operation.

Table 4.21. JTAG Structure on Rx-Controller of the IPSO 19“ Unit

Connector	Stxxx		
JTAG Bridge	Uxx, Adr=yy		
Connector		ST??	ST??
JTAG Chains	**Chain 1**	**Chain 2**	**Chain 3**
Devices		Uxx:DSP	Uxx:FIFO1
			Uxx:FIFO2
			Uxx:FPGA
			Uxx:EEPROM (FPGA)

Power Requirements

Part No.	**Assembly**	**+5V**	**Σ +5 V**	**+3.3V**	**+12V**	**+5VSB**	**-12V**
H1256xx	Rx-Controller	0	0	0.6A	0	0	0

Addendum 5

Pin Allocation of Connectors 5.1

LVDS Connector

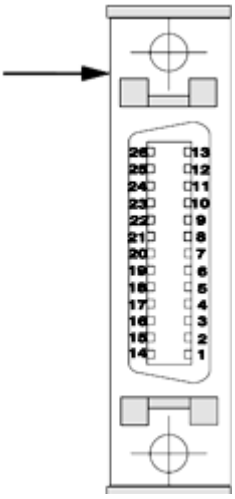


Figure 5.1. Pin location of the 48Bit LVDS Connector at PCB

Table 5.1. Cable and Pin Assignment

Function	Type of Wire	Transmitter Signal	Receiver Signal	Pin Nr.
Signal: Differential pair of the received serial transmit clock connected to the corresponding inputs of the transmitter.	Twisted and shielded	TxCLK_P	RxCLK_P	6
		TXCLK_M	RXCK_M	18
Shield: Common drain wire of all separate shields, connected to CHASSIS.		LVDS Gnd		26
Signal: Differential pair of the received serial data stream connected to the corresponding inputs of the transmitter.	Twisted and shielded	TxIN_P0	RxIN_P0	3
		TxIN_M0	RxIN_M0	15
Shield		LVDS Gnd		26

Table 5.1. Cable and Pin Assignment

Signal	Twisted and shielded	TxIN_P1	RxIN_P1	4
		TxIN_M1	RxIN_M1	16
Shield		LVDS Gnd		26
Signal	Twisted and shielded	TxIN_P2	RxIN_P2	5
		TxIN_M2	RxIN_M2	17
Shield		LVDS Gnd		26
Signal	Twisted and shielded	TxIN_P3	RxIN_P3	9
		TxIN_M3	RxIN_M3	21
Shield		LVDS Gnd		26
Signal	Twisted and shielded	TxIN_P4	RxIN_P4	10
		TxIN_M4	RxIN_M4	22
Shield		LVDS Gnd		26
Signal	Twisted and shielded	TxIN_P5	RxIN_P5	11
		TxIN_M5	RxIN_M5	23
Shield		LVDS Gnd		26
Signal	Twisted and shielded	TxIN_P6	RxIN_P6	12
		TxIN_M6	RxIN_M6	24
Shield		LVDS Gnd		26
Signal	Twisted and shielded	TxIN_P7	RxIN_P7	13
		TxIN_M7	RxIN_M7	25
Shield		LVDS Gnd		26
USB signal pair, left open	Twisted and shielded	USB+		1
		USB-		14
Shield of the USB signal pair, connected to CHASSIS		USB Gnd		2
Signal: connected to bit1 of register “chanconf” on F and G Controller	Individual	CHANNEL_DETECT0		7
Signal: connected to bit1 of register “chanconf” on F and G Controller	Individual	CHANNEL_DETECT1		20
VCC of USB power, left open	Individual	USB Pwr		19
GND of USB power, connected to GND	Individual	USB Gnd		8
Common shield of the entire bundle	Shield	CHASSIS		Body

Chassis

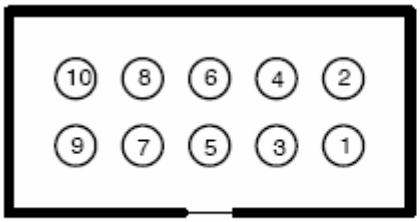
Chassis is a separate plane in the PCB layer stack. This plane stacks directly next to the ground plane, giving a very tight capacitive (only capacitive) and low inductance coupling to GND. The chassis plane screws to the external chassis along the front edge near the connectors and the line drivers.

This solution reduces the digital noise at that point and the noise which is picked up by the driver and carried to the outside. In addition it avoids parasitic current through the GND plane which could be caused by potential differences of the remote device.

DS_OPT, Deskew optimization:

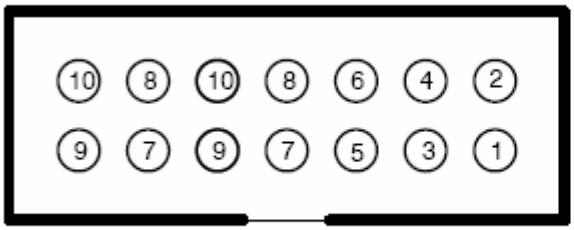
DS_OPT of the transmitter is triggered after power up and under software intervention. At the receiver this pin should be configurable to high or low which would enable or disable the receiver to optimize the skews.

JTAG Connectors



Pin	Signal	Pin	Signal
1	TRSTB	2	GND
3	TDOB	4	GND
5	TDIB	6	GND
7	TMSB	8	GND
9	TCKB	10	GND

Figure 5.2. JTAG Programming Connector



Pin	Signal	Pin	Signal
1	TMSL1	2	TRSTL1
3	TDIL1	4	ENABLE_T
5	3,3V	6	GND
7	TDOL1	8	GND
9	TCKL1	10	GND
11	TCKL1	12	GND
13	EMU0	14	EMU1

Figure 5.3. JTAG Emulation Connector for DSP

PCI Connector

Table 5.2. PCI Board Connector Revision 2.3

Pin	Side B	Side A		Pin	Side B	Side A
1	- 12 V	TRST#		32	AD[17]	AD[16]
2	TCK	+12V		33	C/BE[2]#	+3.3V
3	GND	TMS		34	GND	FRAME#
4	TDO	TDI		35	IRDY#	GND
5	+5V	+5V		36	+3.3V	TRDY#
6	+5V	INTA#		37	DEVSEL#	GND
7	INTB#	INTC#		38	GND	STOP#
8	INTD#	+5V		39	LOCK#	+3.3V
9	PRSNT1#	Reserved		40	PERR#	SMBCLK
10	Reserved	+3.3V(I/O)		41	+3.3V	SMBDAT
11	PRSNT2#	Reserved		42	SERR#	GND
12	3.3V Key			43	+3.3V	PAR
13	3.3V Key			44	C/BE[1]#	AD[15]
14	Reserved	3.3V aux.		45	AD[14]	+3.3V
15	GND	RST#		46	GND	AD[13]
16	CLK	+3.3V(I/O)		47	AD[12]	AD[11]
17	GND	GNT#		48	AD[10]	GND
18	REQ#	GND		49	M66EN	AD[09]
19	+3.3V(I/O)	PME#		50	5V Key	
20	AD[31]	AD[30]		51	5V Key	

Table 5.2. PCI Board Connector Revision 2.3

21	AD[29]	+3.3V		52	AD[08]	C/BE[0]#
22	GND	AD[28]		53	AD[07]	+3.3V
23	AD[27]	AD[26]		54	+3.3V	AD[06]
24	AD[25]	GND		55	AD[05]	AD[04]
25	+3.3V	AD[24]		56	AD[03]	GND
26	C/BE[3]#	IDSEL		57	GND	AD[02]
27	AD[23]	+3.3V		58	AD[01]	AD[00]
28	GND	AD[22]		59	+3.3V$^{(I/O)}$	+3.3V$^{(I/O)}$
29	AD[21]	AD[20]		60	ACK64#	REQ64#
30	AD[19]	GND		61	+5V	+5V
31	+3.3V	AD[18]		62	+5V	+5V

Addendum

Figures

Figures

Tables

Tables

End of Document

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