Bruker BioSpin

LVDS Gradient Interface

48-Bit LVDS Gradient Interface
Technical Manual

Version 001

think forward

NMR Spectroscopy

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Contents

Contents

Introduction 1

Introduction 1.1

This document describes the Low Voltage Differential Serial (LVDS) interface between the sources of the gradient sequence (GCU/GCntrl or DPP output respectively) and their destinations (Gradient Amplifiers DPP Input respectively).

These devices are connected in the following manner:

- GCU or G-Cntrl Output -> Gradient Amplifier or BGU Input
- GCU or GCntrl-Output -> DPP Input/DPP-Output -> Grad.Amp. or BGU-Input.

GCU/G-Cntrl-Output and Gradient Amplifier/BGU-Input can be connected directly. Inserting the DPP as a third device is optional.

This document is based on the description of the 28-bit interface “LVDS GCU3/ BGU3 Interface” supplemented with the following advancements:

- Size of words is now 48 bit; bandwidth up to 80 M words; transmitted on8 data pairs with a bit rate of 480 MHz.
- Possibility to safeguard the transmission by a parity bit.
- Extended data size from 20 to 32 bits for future use.
- Extended address range from 64 to 1024 addresses.

Serving the extended data size and address range needs devices with a local data bus wider than 32 bits. Therefore GCU, DPP and BGU so far can’t make use of these two features. But the requirements to connect them each other and to 64-bit devices by this interface are taken into account and fulfilled by the specifications of this document. Of course to do this would require in advance to replace their interface devices by 48-bit ones.

Version Declaration 1.2

Modifications will be marked with a vertical bold line at the right side. Modifications marked in this version are made since 2005_11_17.

Acronyms 1.3

LVDS	Low Voltage Differential Serial interface.
GCU	Gradient Control Unit of the AV System.
G-Controller (GCntrl)	Gradient Controller of the IPSO System.
F-Controller (FCntrl)	Frequency Controller of the IPSO System.
BGU	Gradient Amplifier of the AV System for medical applications.
Grad.Amp.	Generic Gradient Amplifier.
DPP	Digital Pre-emphasis Processor.

Disclaimer 1.4

The unit should only be used for its intended purpose as described in this manual. Use of the unit for any purpose other than that for which it is intended is taken only at the users own risk and invalidates any and all manufacturer warranties.

Service or maintenance work on the unit must be carried out by qualified personnel.

Only those persons schooled in the operation of the 48-Bit LVDS Interface should operate the unit.

Read this manual before operating the unit. Pay particular attention to any safety related information.

Warnings and Notes 1.5

There are two types of information notices used in this manual. These notices highlight important information or warn the user of a potentially dangerous situation. The following notices will have the same level of importance throughout this manual.

Note: Indicates important information or helpful hints

WARNING: Indicates the possibility of severe personal injury, loss of life or equipment damage if the instructions are not followed.

Contact for Additional Technical Assistance *1.6*

For further technical assistance on the BPSU36-2 unit, please do not hesitate to contact your nearest BRUKER dealer or contact us directly at:

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Specifications 2

Involved Devices 2.1

Device	Applica-tion	Part #	Environmental Conditions	
			Hardw.	Softw.
Gradient–Controller (G–Cntrl0)	HR/TOMO	H12530	IPSO	topspin Version x.x
Gradient Control Unit (GCU3)	HR/TOMO	H5817	AQS	**XWIN–NMR Version 3.5**
DPP1: Digital–Preemphasis–Processor, 28–Bit LVDS	HR/TOMO	H12513	IPSO	topspin Version x.x
DPP1: Digital–Preemphasis–Processor, 48–Bit LVDS	HR/TOMO	H12513F1	IPSO	topspin Version x.x
DPP2: Digital–Preemphasis–Processor with PPC	HR/TOMO	H12560	IPSO	topspin Version x.x
Gradient–Amplifier/BGU3 DIA Converter LVDS RAMPD Board	TOMO	T9227	IPSO/AQS	XWIN–NMR Version 3.5
Gradient–Amplifier/BGU3 DIA Converter LVDS Board	HR	T9226	IPSO/AQS	XWIN–NMR Version 3.5

Accessories *2.2*

Part	Type	Manufacturer	Part Nr.
48–Bit LVDS Receiver, (33–112) MHz	DS90CR484	NS	85539
48–Bit LVDS Transmitter, (33–112) MHz	DS90CR483	NS	85529
48–Bit LVDS Receiver, (65–112) MHz	DS90CR482	NS	86853
48–Bit LVDS Transmitter, (65–112) MHz	DS90CR481	NS	86112
48–Bit LVDS PCB Connector, 26 pin female	10226–1210VE	3m	85843
48–Bit LVDS Cable 1m	14526–EZHB–100–0QC	3m	86868
48–Bit LVDS Cable 2m	14526–EZHB–200–0QC	3m	
48–Bit LVDS Cable 5m	14526–EZHB–500–0QC	3m	
48–Bit LVDS Cable 10m	14526–EZHB–A00–0QC	3m	not recommended

Pin Assignment and Connections

3

This chapter contains the pin assignment and description of connectors and cables (for the serial side of the LVDS).

Cables 3.1

The cable consists of 10 separately shielded pairs and 4 individual wires. The 10 shields are connected to a common drain wire (LVDS Gnd).

The shield of the entire bundle is connected to the plated body of the connector called “Chassis”.

The characteristic Impedance is 100+/- 10 Ohms.

The Propagation Velocity 4.1 ns/m.

Pins Assignment

Type of Wire	Function	Transmitter Signal	Receiver Signal	Pin Nr.	Usage
Twisted + Shielded	Signal	TxCLK_P	RxCLK_P	6	used
	Signal	TxCLK_M	RxCLK_M	18	used
	Shield	LVDS Gnd		26	used
Twisted + Shielded	Signal	TxOUT_P0	RxIN_P0	3	used
	Signal	TxOUT_M0	RxIN_M0	15	used
	Shield	LVDS Gnd		26	used
Twisted + Shielded	Signal	TxOUT_P1	RxIN_P1	4	used
	Signal	TxOUT_M1	RxIN_M1	16	used
	Shield	LVDS Gnd		26	used
Twisted + Shielded	Signal	TxOUT_P2	RxIN_P2	5	used
	Signal	TxOUT_M2	RxIN_M2	17	used
	Shield	LVDS Gnd		26	used

Twisted + Shielded	Signal	TxOUT_P3	RxIN_P3	9	used
	Signal	TxOUT_M3	RxIN_M3	21	used
	Shield	LVDS Gnd		26	used
Twisted + Shielded	Signal	TxOUT_P4	RxIN_P4	10	used
	Signal	TxOUT_M4	RxIN_M4	22	used
	Shield	LVDS Gnd		26	used
Twisted + Shielded	Signal	TxOUT_P5	RxIN_P5	11	used
	Signal	TxOUT_M5	RxIN_M5	23	used
	Shield	LVDS Gnd		26	used
Twisted + Shielded	Signal	TxOUT_P6	RxIN_P6	12	used
	Signal	TxOUT_M6	RxIN_M6	24	used
	Shield	LVDS Gnd		26	used
Twisted + Shielded	Signal	TxOUT_P7	RxIN_P7	13	used
	Signal	TxOUT_M7	RxIN_M7	25	used
	Shield	LVDS Gnd		26	used
Twisted + Shielded	Signal	USB+		1	used
	Signal	USB-		14	used
	Shield	LVDS Gnd		26	used
Individual	Signal	CHANNEL_DETECT0		7	used
Individual	Signal	CHANNEL_DETECT1		20	used
Individual	Signal	USB pwr		19	reserved
Individual	Signal	USB gnd		8	used
Shield	Common Shield Of The Entire Bundle	CHASSIS		Metal surface of the connector	used

The PCB Connector *3.2*

The PCB is av10226-1210VE, 26-pin female connector.

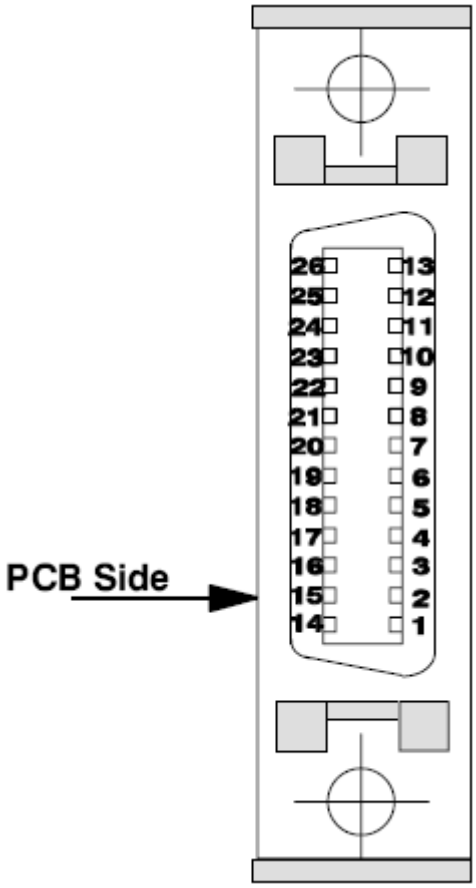

Figure 3.1. Front View at 48-bit LVDS Connector

Signal Description *3.3*

TxCLK	Differential pair of the serial transmit clock connected to the corresponding outputs of the transmitter.
RxCLK	Differential pair of the received serial transmit clock connected to the corresponding inputs of the receiver.
TxOUT	Differential pair of the serial transmitted data connected to the corresponding outputs of the transmitter.
RxIN	Differential pair of the received serial data stream connected to the corresponding inputs of the receiver.
LVDS Gnd	Common drain wire of all separate shields, connected to CHASSIS.
USB Gnd	Shield of the USB signal pair, connected to CHASSIS.
USB +/-	USB signal pair, connected to CHASSIS if not used.
USB pwr	VCC of USB power, connected to CHASSIS if USB is not used.
USB gnd	GND of USB power, connected to GND at GCU and GCntrl, tied top in 20 at DPP input, left open at DPP output and BGU input if USB is not used.
CHANNEL_DETECT 0/1	By reading the logical state of CHANNEL_DETECT the GCU, GCntrl and FCntrl can recognize the connection of the DPP, the Gradient Amplifier, the SGU or the open line.
CHASSIS	Chassis is a separate plane in the PCB layer stack. This plane stacks directly next to the ground plane, giving a very tight capacitive (only capacitive) and low inductance coupling to GND. The chassis plane screws to the external chassis along the front edge near the connectors and the line drivers. This solution reduces the digital noise at that point and the noise which is picked up by the driver and carried to the outside. In addition it avoids parasitic current through the GND plane which could be caused by potential differences of the remote device.
DS_OPT	Deskew optimization: DS_OPT of the transmitter is triggered after power up and under software intervention. At the receiver this pin should be configuerable to High or Low which would enable or disable the receiver to optimize the skews.

Pin Connections

Signal	Pin Nr.	Signal at					
		GCU	**G-Cntrl**	**DPP2_Out**	**DPP2_In**	**BGU/ Grad. Amp.**	**SGU**
		connected to					
DS_OPT/ DESKEW	---	DS_OPT of the LVDS transmitter is activated after power-up and by command.			DESKEW of LVDS receiver has to be configurable (High or Low).		
CHANNEL_ DETECT_0	7	Status register + pull_up		pull_up	Pin 8 (GND)	open	Pin 8 (GND)
CHANNEL_ DETECT_1	20	Status register + pull_up		pull_up	Pin 8 (GND)	Pin 8 (GND)	open
USB gnd	8	GND	GND	Pin 8 + 20 of DPP_In to pin 8 of DPP_Out		USB device (if any)	
USB pwer	19	open	5 V	Pin 19 of DPP_In	Pin 19 of DPP_Out		
USB +/-	1/14	open	USB Hub	Pin 1 + 14 of DPP_In	Pin 1 + 14of DPP_Out		
USB Gnd	2	CHASSIS					
LVDS Gnd	26						

Local Bus Bit Assignment

4

This chapter contains information on the local bus bit assignment of the involved devices on the parallel side of the LVDS.

NXGO and BSTR are the “Next Gradient” signal and the “Gradient Data Valid” signal sent from GCU.

NG and VALID are the “Next Gradient” signal and the “Gradient Data Valid” signal sent from GCntrl.

Table 4.1. Bit Assignment of 48-bit LVDS

LVDS Parallel Interface																							
Bit Pos.	48	47	-	44	43	-	38	37	-	22	21	-	18	17	-	6	5	4	3	2	1
Bit#	1	4			6			16			4			12			1	1	1	1	1
Meaning	P	MSB Address						MSB Data						Data (res)			(res)		L	V	N
Device																							
BGU	PAR	open			ADD<5..0>			DATA<15..0>			gnd			gnd			gnd		-	!BSTR	!NXGO
GCU	PAR	gnd			ADD<5..0>			DATA<19..0>						gnd			gnd		!LAST	!BSTR	!NXGO
DPP2	PAR	ADD<9..0>						DATA<19..0>						gnd			gnd		!LAST	!BSTR	!NXGO

Table 4.1. Bit Assignment of 48-bit LVDS

IPSO/G-Cntrl	PAR	ADD<9..0>	DATA<19..0>	gnd	gnd	!LAST	!VALID	!NG
Grad. Amp.	PAR	ADD<9..0>	DATA<19..0>	gnd	gnd	!LAST	!VALID	!NG

The 32-Bit Local Bus Connection on the GCU, BGU and DPP *4.1*

GCU and DPP are equipped with a 32-bit processor and a 32-bit local data bus. Therefore they can't access all 48-bit at once.

On DPP the processor is able to accept 20 gradient data bits, 10 address bits, !LAST and !NXGO. The data word of the GCU contains several control bits and can handle 26 bits of the LVDS word only.

The Gradient structure is a 32-bit wide word list in Data Memory. This list is created by the i960 on GCU and written into the Sequencer Data RAM. Bit 31 is a StopBit for the Sequencer and bit 26 marks a word for the external DAC or its internal Timer. Bits 26 to31 are not transferred to external destinations.

Bit 0 to 25 of the GCU Gradient Memory form together with the validity bit (BSTR) and the next gradient strobe (NXGO) the 28-bit gradient data word of the so far used 28-bit LVDS. Introducing the parity bit (PAR) and wider address and data parts made the wider 48-bit LVDS necessary. In such case the !LASTBit can not be retrieved from any bit position of the local bus. It has to be generated by the sequencer.

Transferring the 48-bit word to DPP or Grad.Amp. is released at the parallel side of the LVDS by the 80 MHz rising edge.

Table 4.2. Connection of the 32-Bit Local Bus to 48-Bit LVDS

Bit Pos. at LVDS	48	47	-	44	43	-	38	37	-	22	21	-	18	17	-	6	5	4	3	2	1
Bit#	1	4			6			16			4			12			1	1	1	1	1
Meaning	P	MSB Address						MSB Data						Data (res)			(res)		N	V	N
	PAR	ADD<9..6>			ADD<5..0>			DATA<15..0>			gnd			gnd			gnd		!LAST	!BSTR	!NXGO
								DATA<19..0>													
Local Bus Pos. at:																					
GCU	-	n.a.			25	-	20	19	-	4	3	-	0	n.a.			n.a.				
DPP	-	29	-	26	25	-	20	19	-	4	3	-	0	n.a.			n.a.				
BGU	-	n.a.			25	-	20	19	-	4	n.a.			n.a.			n.a.				

!BSTR, !NXGO, !LAST and PAR are not generated or handled by the processor on GCU and BGU and !BSTR and PAR also not on DPP. Therefore they have at that locations no representation on the Local Bus.

The !BSTR signal active low indicates the validity of the gradient address and data lines at the LVDS output of the receiver.

The next gradient signal (!NXGO = active low) is always valid also without the BSTR validity bit.

The 64-Bit Local Bus Connection on G-Cntrl *4.2*

Table 4.3. Connection of the 64-Bit Local Bus to 48-Bit LVDS

Bit Pos. at LVDS	48	47	-	44	43	-	38	37	-	22	21	-	18	17	-	6	5	4	3	2	1	-	-
Bit#	1	4			6			16			4			12			1	1	1	1	1	1	1
Meaning	P	MSB	Address					MSB	Data					Data (res)			(res)		L	V	N	OUT	A/B
	PAR	ADD<9..6>			ADD<5..0>			DATA<19..0>						gnd			gnd		!LAST	!BSTR	!NXGO		
Local Bus Pos. at:																							
G-Cntrl	-	47b	-	44b	43b	-	38b	37b	-	22b	21b	-	18b	17b		6b	5b	4b	3b	2b	34a	33a	0

PAR is not generated by the processor. Therefore it has no representation on the Local Bus.

Transferring the gradient data is carried out by the sequencer. The LVDS interface is clocked with the 80 MHz rising edge.

The VALID signal (VALID = active low) indicates the validity of the gradient address and data lines of the BWord at the LVDS output of the receiver.

The next gradient signal of word A (NG = active low) is always valid without any VALID bit.

Gradient Address and Data Layout

5

Table 5.1. Gradient Address Layout (all further addresses are reserved).

Name	Gradient Address ADD<9::0>	Gradient Data DAT<19::0>	Effect	
			on DPP	on Grad.Amp.
X Gradient	0x000	<amplitude value>	X Gradient	
Y Gradient	0x001		Y Gradient	
Z Gradient	0x002		Z Gradient	
B0 Gradient	0x003		B0 Gradient	
Control word	0x03F	0x10	X,Y,Z,B0 → 0	BGU–HR: X,Y,Z,B0 → 0 BGU–TOMO: Count X,Y,Z,B0 down
		0x20	Count X,Y,Z,B0 down	
		0x01	forwarded to Grad. Amp.	Blank of X Grad.
		0x02		Blank of Y Grad.
		0x04		Blank of Z Grad.
		0x08		Blank of B0 Grad.

The data bits of the Control Word are not analyzed on the existent BGU! Only the address 0x03F activates setting or counting the gradient values to zero. If the DPP is inserted between GCU and Grad.Amp., the Control Word will be processed on the DPP and dependent on its data content forwarded or not forwarded to the Grad.Amp.

A future Grad.Amp. can get this control word, analyze its data bits and carry out an action controlled out of the pulse program, if this would be reasonable.

Table 5.2. Gradient Data Layout

DATA<19..0>	19	---	4	3	---	0
Bit Value, 20 bit DAC	MSB					LSB
Bit Value, 16 bit DAC	MSB	---	LSB			
LVDS Value Coding, 16 bit, hexadecimal	7 F F F Pos. . . . 0 0 0 0 . . . 8 0 0 0 Neg.					
DAC Value Coding, 16 bit, hexadecimal	F F F F Pos. . . . 8 0 0 0 . . . 0 0 0 0 Neg.					

Functional Requirements

6

Parity 6.1

- The Parity is created to be “Even” by including the following number of bits:

  bit1...bit47 on GCntrl and DPP2

  bit1...bit46 on FCntrl

- DPP1 (H12513 with 28-bit LVDS and H12513F1 with 48-bit LVDS) is not able to generate the parity bit.
- Switching off the parity check by software intervention should be possible at any input!

Control 6.2

- The LVDS Receiver Interface at the Gradient Amplifier must have a pre-load register for the Gradient Data of each channel located between the LVDS Receiver and the DAC Register.
- The rising edge of the received 80 MHz clock of the phase with NXGO/NG = low loads the contents of all preload registers into the DAC Registers.
- Each NXGO/NG is followed by the new gradient data packet which must be loaded into the preload registers and activated with the next NXGO/NG.
- The rising edge of the received 80 MHz clock of each clock phase with BSTR/VALID = low loads the value at the Gradient Data lines into the preload register indicated by the value at the Gradient Address lines of that clock phase.
- NXGO/NG are valid independent of BSTR/VALID respectively. That means, they need not the validity declaration of BSTR/VALID.
- Each single clock phase with NXGO/NG = low is followed by 1, 2, 3 or n (X, Y, Z, B0) clock phases with BSTR/VALID = low.
- Clock phases with BSTR/VALID = low could be separated by idle phases.
- There are no clock phases with NXGO/NG = low AND BSTR/VA-LID = low.

Configuration Recommendations for the Transmitter and Receiver *6.3*

As described above the pin DS_OPT of the transmitter is triggered after the Power-On reset to send the optimization sequence.

Experience shows that, if the DESKEW process is enabled at the receiver and the cable is plugged out and in again without powering the system down and up would lead to malfunctioning up to the next power down. Therefore, there should also be additional means at the transmitter to carry out the DESKEW sequence on the running system, preferably software. Otherwise the cable must not be changed after power up.

The DESKEW sequence lasts at least 4 clock cycles (50 nsec) but can also be longer. The outputs of the receiver device are held low during DESKEW except for the clock. The evaluating logic has to make sure that a 48-bit word with all bits at low will not be sampled as valid data.

The transmitter and receiver devices (DS90CR481/482) provide several features to avoid the sampling of invalid data and to optimize the signal quality (Power down, Deskew, DC balancing, Pre-emphasis). To work properly they require a consistent configuration on both sides of the cable:

Deskew	Activated at the transmitter after status change of CHANNELDE-TECT by a software command and after Powerup.Configurable at the receiver by jumper or software.Disabled at the receiver if the length of the cable is below 5 meters. Disabled at the receiver if no means are provided to start Deskew by a software command on the powered system.Disabled at the transmitter and the receiver at a transfer clock over 80 MHz.
Pre-emphasis	Configurable at the transmitter by jumper or software. Disabled at the transmitter if the cable length is below 2 meters. There must not be any over or undershoot at the receivers end.
DC Balancing	Enabled at the transmitter.
Power Down	Disabled at transmitter and receiver.

Device	Function	Config.	Configurable
Receiver DS90CR482	Deskew	Disabled pin4=GND	YES by jumper or software
	Power down	Disabled	NO

Device	Function	Config.	Configurable
Transmitter DS90CR481	Deskew	Activated after Power–On reset	Activateable by software
	DC balancing	Enabled pin24=VCC	NO
	Preemphasis	Disabled pin14=open (NC)	YES by jumper or software
	Power down	Disabled	NO

It should be pointed out that all these features can not avoid the sampling of corrupted data as valid in case of plugging out and in the cable under power.

Timing 7

Details of Clock Data Timing should be extracted from National Semiconductors Website (http://www.national.com/pf/DS/) for following data sheets:

48-Bit LVDS: DS90CR481/482

Figures

Figures

Tables

Tables

End of Document

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