IPSO 19" & IPSO AQS

AVANCE III
User Manual

Version   001

Bruker BioSpin

The information in this manual may be altered without notice.

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Intelligent Pulse Sequenz Organizer (IPSO)

This Manual covers the spectrometer control unit called IPSO as version

- IPSO 19"
- IPSO AQS

which are used in the *AVANCE ^{III}* spectrometers

Chapter "1." summarizes the most essential informations for users to get started quickly and to avoid beginner's mistakes without reading plenty of pages.

Chapter "2." lists the part/order numbers of the main assemblies, subassemblies and devices.

Chapter "3." et seqq. provide the more detailed descriptions of assemblies and devices.

1. Condensed Introduction

Do's and Don'ts

- Do not connect a receiver to the LVDS connector of the controller in Slot2 of the IPSO 19" Unit. There will never be valid data.
- A LVDS cable should never be removed from or connected to a powered controller. Corrupted data could be sampled as valid.
- Do not connect more than one Gradient Amplifiers to the same system.

1. 1. Structure and Features

Features

- IPSO is a digital spectrometer control unit with a variable number of output channels (Tx–Controllers)
- Each Tx–Controller outputs a stream of 48–bit words at a clock rate of 80 MHz per word
- Transferral of a complete set of frequency parameters requires two words.
- The time resolution of parameter switching in any combination of Frequency, Phase, Amplitude is 12.5 nsec.
- The minimal duration of any combination of parameters is 25 nsec.
- Gradient channels require one word per gradient.
- The maximal number of addresses for different gradients (the max. number of gradient channels) is 1k.
- A constant time delay between the outputs of the different Tx–Controllers may be adjusted to any number of 80MHz clock cycles up to 2^{29}x12.5nsec

Structure

The distinctive Parts of the system are the Host Controller charged with administrative tasks, the number of Tx–Controllers generating and transferring the parameter sequences and the Sequencer providing for a means of communication between the Tx–Controllers.

The Controllers

The system contains the 3 types of controllers, Host Controller, Rx–Controller and the Tx–Controller.

Host Controller: There is only one Host Controller in the system. The Host Controller is an IBM compatible PC with all standard interfaces thus making access possible to the whole pool of standard hardware and software.

The Host Controller boots its operating system software (diskless LINUX) from and communicates with the TOPSPIN–PC over Ethernet. It also communicates over its standard interfaces with the Rx– and the Tx–Controllers and with peripheral devices.

Rx–Controller: The Rx–Controller is able to receive 48–bit words at its LVDS interface at a rate of up to 100–Mega words. Therefore it can be used as a fast data link from the receiver channel to the transmit channel, bypassing the ethernet and the TOPSPIN–PC. Furthermore all Tx–Controllers and their LVDS interfaces can be tested with the IPSOTEST if their interfaces are connected to a Rx–Controller.

Realtime processing of that data can be done by an onboard DSP. The processed data can be transferred by the DMA channels of the DSP over the system bus to any other controller or may be fetched by any other controller.

Usually there is one Rx–Controller in the system. Without additional software (that means transparent to the software) it is possible to include additional Rx–Controllers using extension boxes.

The Rx–Controller has no connections to the Sequencer and communicates and exchanges data with other controllers via the system bus. It will function in any slot of the IPSO but should be inserted in slot 1.

Tx–Controller: Depending on its configuration, the Tx–Controller can be used for any of the 3 output functions in the system. These functions are the T–Controller servicing the RCP outputs at T0 with timing signals, the F–Controller generating the frequency parameters for the SGUs and the G–Controller generating the gradient packets for the amplifiers.

The Tx–Controllers and their common Sequencer are the most decisive parts of the IPSO system. The Sequencer is a single device, just one piece of silicon. It contains the communication and decision making logic of all Tx–Controllers and the communication bus between them known from former systems as the AQ–Bus. The AQ–Bus allows for real time communication on a 1–clock base of 12.5 nsec.

The controller itself consists of a DSP with memory, FIFO, output logic and interfaces to the system bus and the Sequencer. The DSP gets its code from the Host Controller, generates the parameter sequences and writes them into the FIFO. Its most important task is to keep the FIFO full. The Sequencer (once started) reads the words out of the FIFOs of all controllers, realizes the defined timing in each channel and controls the outputs.

The global functions of the Sequencer (e.g. START, STOP, SUSPEND, RESUME and so on) are part of the Sequencer logic of the T–Controller. Therefore a T–Controller has to be in the system to carry out any type of acquisition.

LVDS

The LVDS cable is the transport media for digital data words between the Tx– and the Rx–Controllers respectively and the peripheral devices like SGU, Gradient Amplifier, DRU and DPP (Digital Preemphasis Processor). The abbreviation LVDS means "low voltage digital signal". The voltage switching range of the data lines is between 1.0V and 1.4V.

The used devices take 48–bit data words at a clock rate of 80MHz (and 100MHz between DRU and Rx–Controller respectively) and serialize and transport them over 8 balanced data line pairs accompanied by one clock pair. At the receiver side the data stream is deserialized and the 48–bit data word and its 80MHz clock are reconstructed.

Because there are 8 data lines, the cable has to transport 6 data bit plus one balance bit per 12,5nsec. That means a bit frequency of 560MHz on each data line. Since a good signal quality needs a good transmission behavior up to the fifth harmonic wave this cable has to transport the signals up to about 3–GHz without frequency dependent distortions.

The LVDS cable driver is always active even if the Tx–Controller is transmitting no valid data.

There are 2 options called "Deskew" and "Preemphasis" which are intended to compensate the negative influence of cables longer than about 3 meters to the signal quality. The usual cable length below 2 meters requires neither Deskew nor Preemphasis.

Deskew: This feature minimizes the effective skew of the different data line pairs in the cable. To be effective it has to be enabled at the receiver and carried out at the transmitter. The default state at introduction is "NOT ENABLED" at the receiver and is activated at the transmitter by a software command only.

                    If enabled at the receiver Deskew has to be carried out after power–up and again each time after the cable has been plugged out and in under power. This can be done by software using the command "`Deskew`" of the "`ipsotest`" program.
                    Software activated Deskew needs TOPSPIN 2.0b6 and a Tx–Controller with Part# "H12538F2". Otherwise with "Deskew enabled at the receiver" the system has to be powered up again after reconnecting.

Preemphasis: This feature compensates for the greater need of charge on cables longer than 2 meters. To be effective it needs one cable–length–dependent resistor at the transmitter. If ever necessary such Tx_Controllers will be given a special part number.

                    The state of the Tx–Controllers with part number "H15538" and "H15538F1" and H12538F2 is "NO PREEMPHASIS"

Besides the data and clock lines the LVDS cable includes 4 lines of an USB channel (unused so far) and 2 state lines. The state lines tell the Tx–Controller the kind of the connected device like "unconnected, SGU connected, Gradient Amplifier connected, DPP connected".

Figure 1: Block diagram of the IPSO 19" Unit
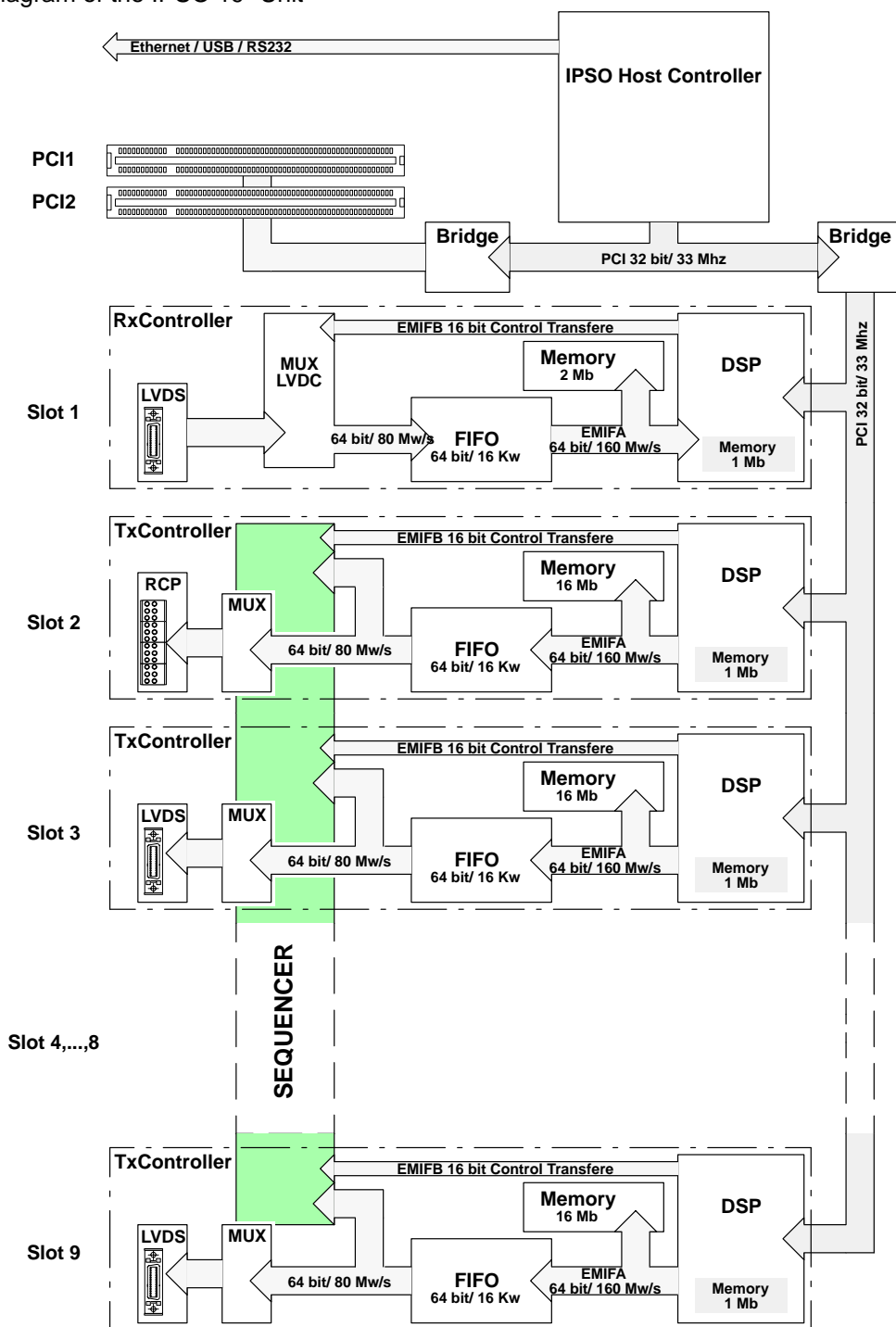
1. 2. Handling

ESD

Handling under ESD safety conditions is necessary.
Don't touch uncovered metal of PCB and connectors before discharging yourself!

Boot procedure

The IPSO needs to boot its diskless LINUX from the TOPSPIN–PC via the Ethernet. This connection with or without an hub included requires the following cable:

Connection	Type	Color	Part#	Length
point–to–point	UTP/CAT5, crossed	red	84338	5m
			83980	10m
point–to–hub	UTP/CAT5, straight	white	83025	5m
			83026	10m

If connected, the IPSO needs only to be switched on or to be resetted to begin booting.

Power ON/OFF Button
To be effective this button needs to be pressed for about 2 seconds to switch the system on and 6 seconds to switch it off.

Reset Button
This button resets the Host Controller, the PCI logic and restarts the boot process. So it leads to the same result as ON/OFF without Power OFF.

Board Installation

Opening the IPSO AQS
Installation of PCI Cards may require removal the right PCB (next figure) together with the upper part of the front panel. This is possible after removing the screws which are highlighted in the next figure.

Figure 2: Removable screws of the IPSO AQS
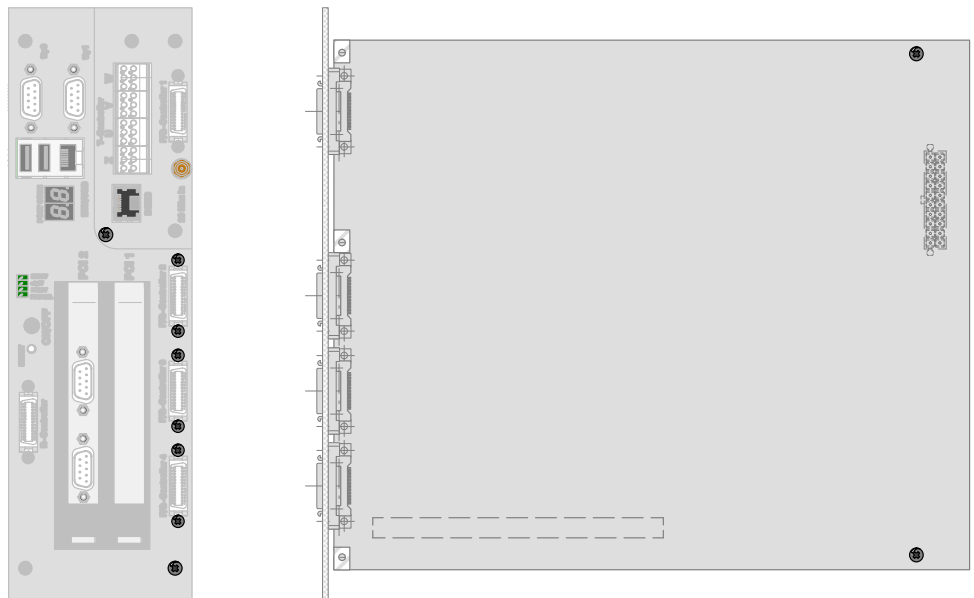
Opening the IPSO 19" Unit
The case of the IPSO has to be opened to facilitate controller/PCI card installation. To do that it is only necessary to remove the two screws (right and left) of the top cover next to the front side.

Rules of Modularity on the IPSO 19" Unit
There are two kind of controllers (Rx–Controller and Tx–Controller) which can be plugged into the 9 slots. Some of the slots are dedicated to a unique controller and some stamp a special function on the generic Tx–Controller:

Rx–Controller: Slot1 is intended to be used by the Rx–Controller only. But it would work as receiving controller in any other slot.

Tx–Controller: Slot2 to Slot9 are designed to be Tx–Controller's places. Plugged into Slot1 the Tx–Controller would be recognized as "unknown" (U–Controller) but it will not be able to communicate with the sequencer and to transmit data.

Slot2:   Only this slot provides access to the acquisition global functions like START, STOP and so on and to the RCP outputs. Therefore the Tx–Controller in this slot gets the task of the T–Controller. It controls the RCP outputs instead of its LVDS output. Do not connect a cable to this LVDS connector. The LED below this connector is always off.

Slot3 to Slot9:   Tx–Controllers in these slots can work as F–Controller (default) or G–Controller.

                               The LED below the LVDS connector lights green at the F–Controller and yellow at the G–Controller.

                               The channel numbering of the F–Controller begins at the leftmost one and counts up to the right. There must not be any gap between the F–Controllers.

Which F–Controller will become the G–Controller?

Only the F–Controller which is connected to a Gradient Amplifier will be configured as G–Controller and its LED below the LVDS connector will change from green to yellow.

Connecting more than one Controller to a Gradient Amplifier is not supported by TOPSPIN.

Previous to Rel.2.0, TOPSPIN will only allow the last F–Controller of a system to become the G–Controller. This would be the last one at the right side on "IPSO 19" Unit" and F/G–Controller–4 on "IPSO AQS".

A later release might advantageously allow the G–Controller to be freely selected by connecting the Gradient Amplifier.

Until then an arbitrary F–Controller can be selected as G–Controller if all higher numbered F–Controllers will be logically disabled.

For Example:
You use 3 F–Controllers and 1 G–Controller which is in the slot of FxController–4.
If you want to disable the present G–Controller and use FxController–3 instead, you have to

1. unplug the LVDS–Cable from previous G–Controller

2. plug the LVDS–Cable to FxController–3

3. login to IPSO as root

4. and run
```
root@IPSO:/opt/test>sh aqmod.sh –disable fctrl4 ↵
```

1. 3. Ports

The IPSO services the following Input– and Output Ports

Figure 3: Front View of IPSO 19" Unit
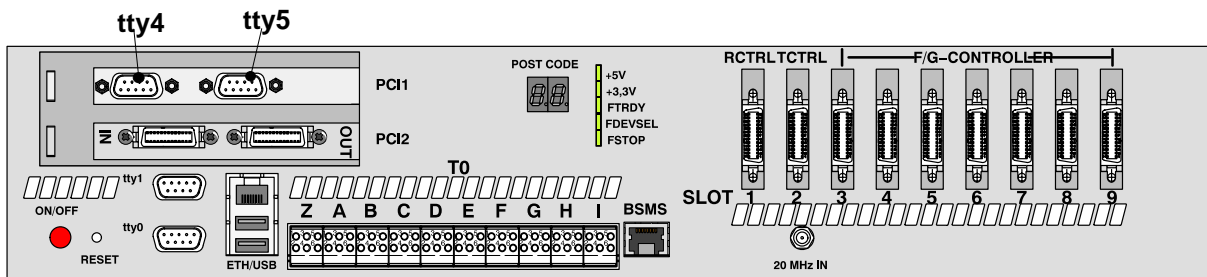
Figure 4: Front View of IPSO AQS
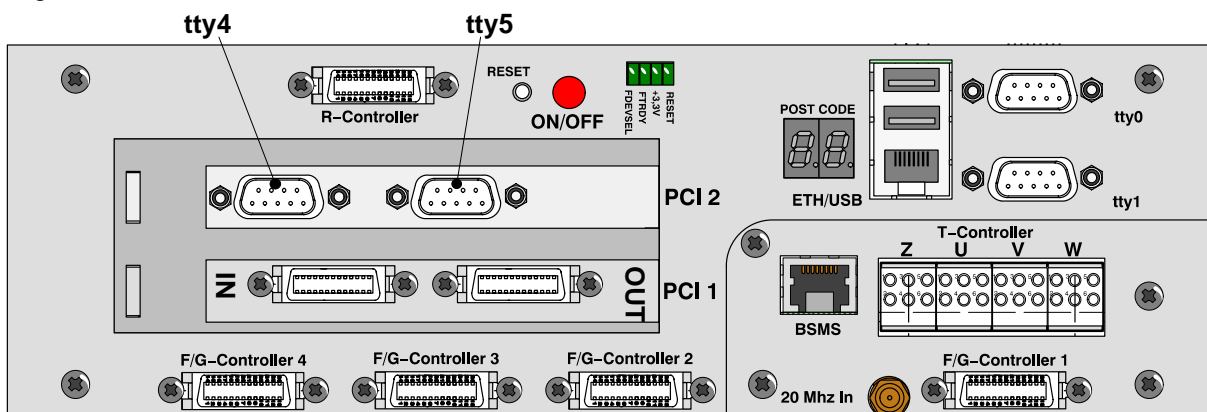
PCI Slots

The two standard PCI slots meet the "PCI Local Bus Specification, Rev.2.1". Both slots are intended for 5–Volt signaling cards (IPSO AQS can accept short cards only).

The total power consumption, summarized for both slots, must not exceed the following values:

IPSO 19" Unit: 10A from +5V and 3.5A from 3.3V

IPSO AQS: 10A from +5V and 5A from 3.3V

Connectors

tty0, tty1:   RS232C on ETX module, max. baud rate 115.2Kbaud
                   The configuration of the tty–interfaces (parity, number of stop bits,
                   kind of handshake, baud rate) is defined and set by the application
                   program.

                   Type of connector is D–Sub, 9 pin, female

Pin #	Signal	Pin #	Signal	Pin #	Signal
1	RI	4	DTR	7	RTS
2	RxD	5	GND	8	CTS
3	TxD	6	DSR	9	not con.
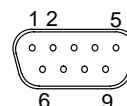
tty4, tty5:   RS232C on auxiliary PCI adapter EX–41052,
                   max. baud rate 115.2Kbaud
                   The configuration of the tty–interfaces (parity, number of stop bits,
                   kind of handshake, baud rate) is defined and set by the application
                   program.

Type of connector is D–Sub, 9 pin, female

Pin #	Signal	Pin #	Signal	Pin #	Signal
1	CDC	4	DTR	7	RTS
2	RxD	5	GND	8	CTS
3	TxD	6	DSR	9	RI
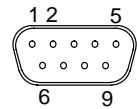
ETH   10/100 BaseT, Intel 82551ER

USB   USB 1.1 OHCI

The Real Time Pulses (RCP) on Connector T0

Electrical Properties and Constraints of the RCP outputs and receiver inputs
The high and low switching levels (U_2) and the associated current (I_c) of the RCP signals depend on the circuitry and driving capacity of the driver and the circuitry of the connected receiver.

Figure 5: RCP Circuit
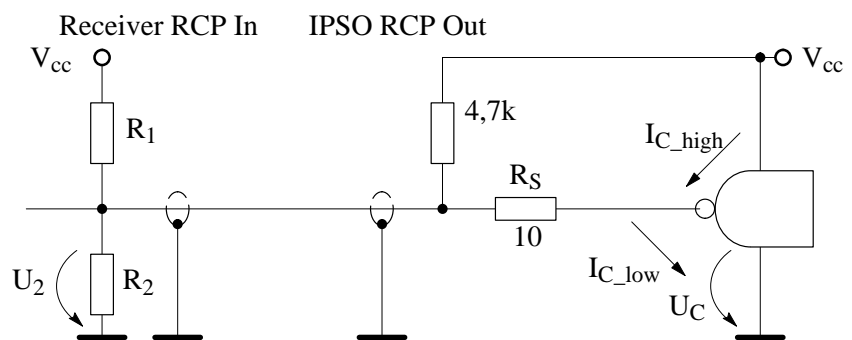
$$V_{CC} = 5V$$

$$U_{C\_low} = 0,3V$$

$$U_{C\_high} = (3,0...3,3)V \qquad U_{2\_low/high} = \frac{\left\{ V_{CC} + U_{C\_low/high} \times \frac{R_1}{R_S} \right\}}{\left\{ 1 + \frac{R_1}{R_2} + \frac{R_1}{R_S} \right\}} \qquad I_{C\_low/high} = \frac{\left\{ U_{2\_low/high} - U_{C\_low/high} \right\}}{R_S}$$

The table shows the resulting voltage levels and currents for some combinations of R_1/R_2. Other combinations are possible and can be checked by the formulas above.

Table 1: RCP voltage levels and currents

Parameter	Combinations of Input Circuit				Units
R_1	100	100	100	200	Ohm
R_2	68	∞	100	200	Ohm
U_2 if I_C=0	2,0	5,0	2,5	2,5	V
U_{2_low}	0,64	0,73	0,66	0,5	V
U_{2_high}	2,8	3,18	2,91	2,95	V

Parameter	Combinations of Input Circuit				Units
I_{c_low}	34	43	36	20	mA
I_{c_high}	−20	−12	−30	−25	mA

Signals and Location

IPSO 19" Unit

The signals which are available at the front side connector T0 are:

Type of Signal	Direct.	Name	Count
RCP Output	out	TCU_xy	51
Trigger Input	in	Trig 1,...,4	4
Extern Suspend	in	EXT_MAN_SUSP	1
Extern Stop	in	EXT_MAN_STOP	1
Emergency Stop	in/out	EX_SGU_RES	1
Peripheral Status	in	SGU_ST	1
Next Value Clock for Preemphasis	out	EXT_GCLK	1

Another 19 RCP signals (shown in red in column "T0") are available at connector ST47 inside of the IPSO case.

Figure 6: RCP pin location of IPSO 19" Unit
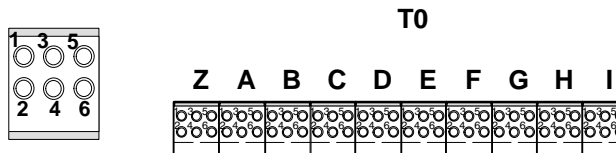
Table 2: Pin assignment of the RCP signals on IPSO 19" Unit

Source/ Destina- tion	RCP and Control Signals of the T–Controller on IPSO 19" Unit								NMR		
	FIFO Word+ Bit Position (64,...,1)		tctrl output reg. tout0, ..., tout4	set nmr 0(#)	set nmr 3(#)	set nmr 4(#)	Layout Name	Di- rec- tion			
	A	B							Meaning	T0	BS MS
BSMS/ LCB		2	T0(0)		0		TCU62	out	!LOCK_HOLD	B1	2
BSMS/ SCBR		3	T0(1)		1		TCU0	out	!HOMOSPOIL	B2	6
1H Transm.		4	T0(2)		2		TCU1	out	SELH_!H/F	B4	
1H Transm.		5	T0(3)		3		TCU2	out	SELX_!X/F	B5	
BSMS/ LCB		6	T0(4)		4		TCU3	out	!INT_A_(Z0)	B3	4
BP		7	T0(5)		5		TCU4	out	MIXCC	B6	

Source/ Destina- tion	FIFO Word+ Bit Position (64,...,1)		tctrl output reg. tout0, ..., tout4	set nmr 0(#)	set nmr 3(#)	set nmr 4(#)	Layout Name	Di- rec- tion	NMR		
	A	B							Meaning	T0	BS MS
		8	T0(6)		6		TCU5	out	res	C1	
HPPR		9	T0(7)		7		TCU6	out	RCP_PA_SWI TCH	C2	
QNP		10	T0(8)		8		TCU7	out	FXA	C3	
QNP		11	T0(9)		9		TCU8	out	FXB	C4	
		12	T0(10)		10		TCU9	out	res	D1	
		13	T0(11)		11		TCU10	out	res	D2	
		14	T0(12)		12		TCU11	out	res	D3	
		15	T0(13)		13		TCU12	out	res	D4	
		16	T0(14)		14		TCU13	out	res	D5	
		17	T0(15)		15		TCU14	out	res	D6	
		18	T1(0)		16		TCU15	out	res	G1	
		19	T1(1)		17		TCU16	out	res	G2	
		20	T1(2)		18		TCU17	out	res	G3	
		21	T1(3)		19		TCU18	out	res	G4	
		22	T1(4)		20		TCU19	out	res	G5	
		23	T1(5)		21		TCU20	out	res	G6	
		24	T1(6)		22		TCU21	out	res	H1	
		25	T1(7)		23		TCU22	out	res	H2	
MED		26	T1(8)		24		TCU23	out	ECG_START_ TRIG	H3	
MED		27	T1(9)		25		TCU24	out	AUT_TUNG_I N	H4	
MED		28	T1(10)		26		TCU25	out	AK- TIV_DEC_RE S	H5	
MED		29	T1(11)		27		TCU26	out	AK- TIV_DEC_RE S	H6	
MED		30	T1(12)		28		TCU27	out	Customer specified	I1	
MED		31	T1(13)		29		TCU28	out	Customer specified	I2	
MED		32	T1(14)		30		TCU29	out	Customer specified	I3	
MED		33	T1(15)		31		TCU30	out	Customer specified	I4	
		34	T2(0)			0	TCU31	out	GAIN_0_TR 1		
		35	T2(1)			1	TCU32	out	GAIN_1_TR 1		

Table title: RCP and Control Signals of the T–Controller on IPSO 19" Unit

Source/Destination	FIFO Word+ Bit Position (64,...,1)		tctrl output reg. tout0, ..., tout4	set nmr 0(#)	set nmr 3(#)	set nmr 4(#)	Layout Name	Di-rec-tion	NMR		
	A	B							Meaning	T0	BS MS
		36	T2(2)			2	TCU33	out	C/AB_TR1	🟥	⬜
		37	T2(3)			3	TCU34	out	GAIN_0_TR 2	🟥	⬜
		38	T2(4)			4	TCU35	out	GAIN_1_TR 2	🟥	⬜
		39	T2(5)			5	TCU36	out	GAIN_2_TR 2	🟥	⬜
		40	T2(6)			6	TCU37	out	GAIN_2_TR 1	🟥	⬜
1H1 KW AMPL		41	T2(7)			7	TCU38	out	RELAY_H	E3	⬜
X1 KW AMPL		42	T2(8)			8	TCU39	out	RELAY_X	E4	⬜
X1 KW AMPL		43	T2(9)			9	TCU40	out	RELAY_Y	E5	⬜
		44	T2(10)			10	TCU41	out	res RACK_ON/ OFF	E6	⬜
		45	T2(11)			11	TCU42	out	RCP	F1	⬜
X1 KW AMPL		46	T2(12)			12	TCU43	out	RELAY Z	F2	⬜
		47	T2(13)			13	TCU44	out	RCP_Scope	F3	⬜
		48	T2(14)			14	TCU45	out	RCP_EXT_D EV	F4	⬜
		49	T2(15)			15	TCU46	out	RCP	F5	⬜
HIGH POWER		50	T3(0)			16	TCU47	out	STP1_DIR	🟥	⬜
HIGH POWER		51	T3(1)			17	TCU48	out	LB_SEL	🟥	⬜
HIGH POWER		52	T3(2)			18	TCU49	out	DCM_STRT	🟥	⬜
HIGH POWER		53	T3(3)			19	TCU50	out	STP1_CLK	🟥	⬜
HIGH POWER		54	T3(4)			20	TCU51	out	STP2_CLK	🟥	⬜

Table title: **RCP and Control Signals of the T–Controller on IPSO 19” Unit**

RCP and Control Signals of the T–Controller on IPSO 19” Unit										
Source/ Destina- tion	FIFO Word+ Bit Position (64,...,1)		tctrl output reg. tout0, ..., tout4	set nmr 0(#)	set nmr 3(#)	set nmr 4(#)	Layout Name	Di- rec- tion	NMR		
	A	B							Meaning	T0	BS MS
HIGH POWER		55	T3(5)			21	TCU52	out	RES_STP1	🟥	⬜
HIGH POWER		56	T3(6)			22	TCU53	out	DCM_RES	🟥	⬜
HIGH POWER		57	T3(7)			23	TCU54	out	GO_POS	🟥	⬜
2H Lock Switch		58	T3(8)			24	TCU55	out	SEL_2H AMP	A1	⬜
		59	T3(9)			25	TCU66	out	res	🟥	⬜
		60	T3(10)			26	TCU57	out	res	Z2	⬜
		61	T3(11)			27	TCU58	out	Q_SWITCH	A3	⬜
2H Lock Switch		62	T3(12)			28	TCU59	out	SEL_!X/2H	A2	⬜
		63	T3(13)			29	TCU60	out	res	F6	⬜
		64	T3(14)			30	TCU61	out	res	I5	⬜
	58		T3(15)			31	TCU56	out	res	I6	⬜
GRASP	59		T4(0)	32			TCU63	out	BLK_GRAD_ X	A4	⬜
GRASP	60		T4(1)	33			TCU65	out	BLK_GRAD_ Y	A5	⬜
GRASP	61		T4(2)	34			TCU64	out	BLK_GRAD_ Z	A6	⬜
	62		T4(3)				TCU67	out		🟥	⬜
	63		T4(4)				TCU68	out		🟥	⬜
	64		T4(5)				TCU69	out		🟥	⬜
BP HR MAS							TRIG1	in	Trigger 0	C5	⬜
BSMS SLCB							TRIG2	in	Trigger 1	C6	⬜
TRIG STRAFI							TRIG3	in	Trigger 2	E1	⬜
TRIG Solid MAS							TRIG4	in	Trigger 3	E2	⬜
Ext. But- ton							EXT_MA N_SUSP	in	Manual Sus- pend	Z5	⬜
Ext. But- ton							EXT_MA N_STOP	in	Manual Stop	Z6	⬜
							EX_SGU _RES	in/out	Emergency Stop	Z3	⬜

RCP and Control Signals of the T–Controller on IPSO 19" Unit										
Source/ Destina- tion	**FIFO Word+ Bit Position (64,...,1)**		**tctrl output reg. tout0, ..., tout4**	**set nmr 0(#)**	**set nmr 3(#)**	**set nmr 4(#)**	**Layout Name**	**Di- rec- tion**	**NMR**		
	A	**B**							**Meaning**	**T0**	**BS MS**
SGU							SGU_ST	in	STATUS	Z4	
DPP							EXT_GC LK	out	NEXT VALUE	Z1	
							GND				1,3, 5

IPSO AQS

The signals which are available at the front side connector T0 are:

Type of Signal	Direct.	Name	Count
RCP Output	out	TCU_xy	14
Trigger Input	in	Trig 1,...,4	4
Extern Suspend	in	EXT_MAN_SUSP	1
Extern Stop	in	EXT_MAN_STOP	1
Emergency Stop	in/out	EX_SGU_RES	1
Peripheral Status	in	SGU_ST	1
Next Value Clock for Preemphasis	out	EXT_GCLK	1

Another 3 RCP signals are available at the RJ–45 connector, labeled "BSMS"

Figure 7: RCP Connector and pin location of IPSO AQS, versions FTMS and NMR
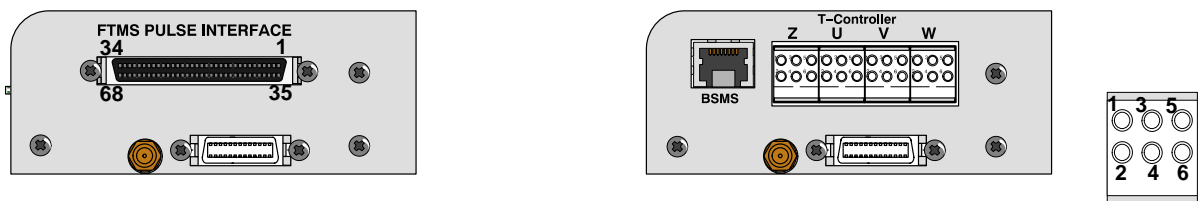
Table 3: Pin assignment of the RCP signals on IPSO AQS

RCP and Control Signals of the T–Controller on IPSO AQS												
Sourc e/Des- tina- tion	**FIFO Word+ Bit Posi- tion (64,...,1)**		**tctrl outp reg. tout0, ..., tout4**	**set nmr 0(#)**	**set nmr 3(#)**	**set nmr 4(#)**	**Layout Name**	**Di- rec- tion**	**NMR**			**FTMS**	
	A	**B**							**Meaning**	**T0**	**B S M S**	**Meaning**	**amp 68**
BSMS/ LCB		2	T0(0)		0		TCU62	out	!LOCK_HO LD		2	User Pulse	5
BSMS/ SCBR		3	T0(1)		1		TCU0	out	!HOMOS- POIL		6	User Pulse	6

	FIFO Word+ Bit Position (64,...,1)		tctrl outp reg. tout0, ..., tout4	set nmr 0(#)	set nmr 3(#)	set nmr 4(#)	Layout Name	Di-rec-tion	NMR			FTMS	
Source/Des-tina-tion	A	B							Meaning	T0	B S M S	Meaning	amp 68
1H Transm.		4	T0(2)		2		TCU1	out	SELH_!H/F	U2		User Pulse	7
1H Transm.		5	T0(3)		3		TCU2	out	SELX_!X/F	U3		User Pulse	8
BSMS/ LCB		6	T0(4)		4		TCU3	out	!INT_A_(Z0)		4	User Pulse	9
HPPR		9	T0(7)		7		TCU6	out	RCP_PA_S WITCH	U4			
		12	T0(10)		10		TCU9	out	res	U5			
		13	T0(11)		11		TCU10	out	res	U6		Combi Laser Pulse	10
		14	T0(12)		12		TCU11	out	res	W2		IRMPD Laser Pulse	11
		15	T0(13)		13		TCU12	out	res	W4		Q Source Shutter	12
		16	T0(14)		14		TCU13	out	res	W6		Q Hexa-pol Deflection	13
1H1 KW AMPL		41	T2(7)			7	TCU38	out	RELAY_H	W1		AMPL BLANK	27
X1 KW AMPL		42	T2(8)			8	TCU39	out	RELAY_X	W3		User Pulse	28
X1 KW AMPL		43	T2(9)			9	TCU40	out	RELAY_Y	W5		User Pulse	29
		47	T2(1 3)			13	TCU44	out	RCP_Scop e	V5			
		48	T2(1 4)			14	TCU45	out	RCP_EXT_ DEV	V6			
2H Lock Switch		58	T3(8)			24	TCU55	out	SEL_2H AMP	U1		User Pulse	31
BP HR MAS							TRIG1	in	Trigger 1	V1		Trigger 1	1
BSMS SLCB							TRIG2	in	Trigger 2	V2		Trigger 2	2
TRIG STRAFI							TRIG3	in	Trigger 3	V3		Trigger 3	3

RCP and Control Signals of the T–Controller on IPSO AQS

RCP and Control Signals of the T–Controller on IPSO AQS												
Source/Destina-tion	**FIFO Word+ Bit Posi-tion (64,...,1)**		**tctrl outp reg. tout0, ..., tout4**	**set nmr 0(#)**	**set nmr 3(#)**	**set nmr 4(#)**	**Layout Name**	**Di-rec-tion**	**NMR**			**FTMS**	
	A	**B**							**Meaning**	**T0**	**B S M S**	**Meaning**	**amp 68**
TRIG Solid MAS							TRIG4	in	Trigger 4	V4		Trigger 4	4
									res	Z2			
Ext. Button							EXT_ MAN_ SUSP	in	Manual Suspend	Z5			
Ext. Button							EXT_ MAN_ STOP	in	Manual Stop	Z6			
							EX_S GU_R ES	in/ out	Emergency Stop	Z3			
SGU							SGU_ ST	in	STATUS	Z4			
DPP							EXT_G CLK	out	NEXT VALUE	Z1			
							GND				1,3 ,5		

1. 4. Boot Operation

A successful boot operation requires the ethernet connection to the powered TOPSPIN–PC which services a valid "diskless", the correct BIOS adjustments on the "IPSO Host Controller" and pushing the Power–On button for about 2 seconds.

The successful completion of the boot process can be checked in TOPSPIN by typing

        ha

or in a LINUX shell by typing

        /opt/topspin/prog/bin/scripts/GetSpectDev –i

Both methods return the IP–Address of the connected IPSO.

The boot process is automatically controlled by the DHCP process. Normally there is nothing to configure and thus nothing to set incorrectly. The causes of an unsuccessful boot process can only be:

- LAN Boot in BIOS not enabled. To enable the LAN Boot feature would require the connection of a monitor and a keyboard to the IPSO

- A corrupted "diskless" on the TOPSPIN–PC, which should be installed again

- A hardware error, which would necessitate further investigation of the boot process to get some more information.

Investigating the Boot Process

Additional information about the boot process can be obtained from 3 sources and from different phases of the boot sequence

1. By monitoring the POST code display and beep codes
   (requires no additional resources)

2. By configuring the Hyper Terminal application (Windows) or the "cu" application (LINUX) on the TOPSPIN–PC.
   (Shows messages of bootloader and LINUX)

3. By connecting a monitor and a keyboard to the IPSO
   (Shows all messages during the boot process and provides access to the BIOS adjustments)

POST Code Display

The Power–on–self–test and configuration routines (POST) start just after Power–on. The POST code points to the individual parts which are currently just running or have stopped in case of an error. This sequence normally ends after about 20 seconds with "C0 = Trying to boot OS"

The list of references between POST codes and routines may be found in the addendum or can be loaded from the webside of "PHOENIX Technologies Ltd" (PhoenixBIOS 4.0, Rev.6).

The POST code display is undefined after start of Linux.

So far occasionally occurred BIOS errors:

POST Code	POST Routine	Possible Causes	Recommended Actions
28	Auto size DRAM	DRAM error	1.Check insertion of the DRAM in the socket 2.Exchange DRAM or PC–Module
49	Unsuccessful PCI configuration	Faultily inserted PC–Module (Host Controller) Any defective Tx– or Rx– Controller in the system Defective RESET sequence	1.Check insertion of the PC–Module 2.Remove the controllers one after the other and try again 3.Check voltages of the Power Supply 4.Exchange the PC–Module
60	Check extended memory	Normal BIOS routine which takes about 10 seconds; the duration is dependend on the volume of memory	If the test doesn't finish, check the correct fit of the memory.
98	Search for any extention ROM	Normal BIOS routine which takes only a few seconds	If the test doesn't finish, check the correct fit of the PC–Module and any PCI–Connection.
B0	Check for errors, stops at B0 with 2 beeps in case of error	The timer contains corrupted time and date information.	To recover the content of the timer: 1. Press the RESET button or 2. Connect an USB–keyboard and press F1 to resume and correct time and date with LINUX or 3. Connect a monitor too, press F2 to enter the BIOS setup and correct the time and date or set "Hold on errors" to "NO"
C0	Try to boot	Successful BIOS process but "No Operating System found"	1.Check Ethernet connection. Yellow LINK LED on? Green Rx/Tx LED active? 2.Check in BIOS if Netboot=yes? (see below) or Netboot is at the top of the list in the submenu "Boot Device Priority" and set the item "Onboard LAN RPL ROM" to "Enabled"

Note:	The PC–Module can be pulled off after removing the 4 screws on top of the Module.	
	To check or exchange the DRAM, the module has to be opened after removing the 2 screws at its bottom side.	

Acoustic Beep Codes

Additional to the POST code display some POST routines sound a beep code on error. This beep code is derived from the hexadecimal POST code of the failing test as follows:

1. The 8–bit error code is broken down to four 2–bit groups.

2. Each group is made one–based (1 through 4) by adding 1.

3. Short beeps are generated for the number in each group.

Example: POST code 16h = 00 01 01 10 = 1–2–2–3 beeps

The "Hyper Terminal" or "cu" window

The boot messages of the IPSO–OS (LINUX) can be printed in a window of the TOPSPIN–PC. This needs a RS232 connection from tty0 of IPSO to a COM port of the TOPSPIN–PC. For details see the TOPSPIN Installation Guide.

Monitor and Keyboard at IPSO

The most detailed information about the boot process can only be obtained by connecting an additional monitor and a keyboard to the connectors inside of the case. It is then possible to watch the BIOS and Linux Messages during the boot sequence and to enter the BIOS setup utility.

Boot Sequence

	Phase of Boot Sequence	Post Code	POST Beeps	Operation
1.	Power On			
		16h	1–2–2–3	Check BIOS ROM checksum
		20h	1–3–1–1	Test DRAM refresh
		22h	1–3–1–3	Test 8742 Keyboard Controller
		2Ch	1–3–4–1	RAM failure on address line xxxx*
		2Eh	1–3–4–3	RAM failure on data bits xxxx* of low byte of memory
		30h	1–4–1–1	RAM failure on data bits xxxx* of high byte of memory
2.	Running POST Code	46h	2–1–2–3	Check ROM copyright notice
		4Ah		
		58h	2–2–3–1	Test for unexpected interrupts
		59h		
		6Eh		
		87h		
		98h	1–2	Search for option ROMs
		B0h	1–1	Halt on error
		C0h		Try to boot

	Phase of Boot Sequence	Post Code	POST Beeps	Operation
3.	DHCP Process			IPSO applies for an IP address at the DHCP server
4.	Running Boot Loader			Load and Start of Bootloader **First message sent to the Hyper Terminal window from Boot Loader**
5.	Loading the OS			Boot messages of Linux in Hyper Terminal

Checking the BIOS Setup

This requires a monitor and a keyboard at IPSO.

The majority of BIOS items should retain their default values. The complete list of items and its values can be found in the "Addendum".

To show the BIOS version press the Pause key after start of booting.

To investigate and modify the BIOS adjustments start the BIOS setup utility by pressing F2 when the following string appears during bootup.

```
Press <F2> to enter Setup
```

Note: Selecting incorrect values may cause boot failures. Load setup–default values to recover by pressing <F9>

Table 4: BIOS adjustments

Entry	Meaning	Phönix BIOS 4.0, Rel. 6.0
Kontron–Version		MOD9R111
Network boot support?		yes
Display Control → Flat Panel Type		Auto Detect
PNP OS Installed	PCI Bridge Support	no
Onboard LPT	Used for JTAG	enable
Legacy USB Support	Global, Interface 0+1, extern	enable
On Chip USB 2 Device	Interface 2+3, intern to Slot A+B	disable
PCI Configuration → PCI IRQ Line1	IRQ select for Line "w"	Auto Select
PCI Configuration → PCI IRQ Line2	IRQ select for Line "x"	Auto Select
PCI Configuration → PCI IRQ Line3	IRQ select for Line "y"	Auto Select
PCI Configuration → PCI IRQ Line4	IRQ select for Line "z"	Auto Select

1. 5. System Configuration

System configurations of this context means:

1. During boot the BIOS checks for available hardware on the PCI bus, e.g. inserted controller or PCI cards. It recognizes the bus layout, scans all possible slots (sites) for devices, reads the type of the devices and their required amount of address space, defines and sets the base address of each device, lists all devices found and determines which interrupt line they are connected to.

2. After boot, the AQ–Driver uses the list of the BIOS, reads some additional registers of some devices and gains the necessary information to decide on which IPSO host model (IPSO 19" Unit or IPSO AQS) the software is coming up.

There is no active role for the user to influence this process other than changing the arrangement of inserted controllers and PCI cards. And normally this should not be necessary.

Modifying the arrangement changes the device number of each device and could alter the following situations:

- Which controllers can communicate with each other without having to go over a bridge. This is normally irrelevant.

- Which of the controllers share the same interrupt line with each other and with other devices, e.g. the Ethernet or the tty ports.

- To which priority level of the interrupt controller (there are 15) the interrupt of a device has been routed

The PCI bus contains 4 interrupt lines (INTw, INTx, INTy, INTz named in BIOS as Line1, Line2, Line3, Line4). The distribution of each controller slot interrupt to one of these lines is hard wired.

Table 5: Interrupt distribution of the IPSO 19" Unit

	Controller Slot										
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**PCI 1**	**PCI 2**
	rctrl	**tctrl**	**fctrl 1**	**fctrl 2**	**fctrl 3**	**fctrl 4**	**fctrl 5**	**fctrl 6**	**fctrl 7**		
Line 1	x					x					
Line 2				x	x				x		
Line 3			x					x		x	
Line 4		x					x				x

Table 6: Interrupt distribution of the IPSO AQS

	Controller Slot							
	rctrl	**tctrl**	**fctrl 1**	**fctrl 2**	**fctrl 3**	**gctrl**	**PCI 1**	**PCI 2**
Line 1			x					x
Line 2		x				x		
Line 3					x			
Line 4	x			x			x	

The decision about routing of Line1/2/3/4 to any of the interrupt priority levels (IRQ) and sharing it with further interrupt sources is made by the BIOS, provided the BIOS parameter "PCI IRQ Line" is set to "Auto Select". These routings can be checked in a LINUX shell with:

```
cat /proc/interrupts
```

We do not recommend replacing "Auto Select" by a special IRQ level.

	highest					Interrupt Priority Order										lowest
IRQ	0	1	8	9	10	11	12	13	14	15	3	4	5	6	7

Recognition of the host model

Recognition of the host model and the version of the installed controller will be performed by the AQ–Driver of LINUX in following steps:

1. Search for a PLX device with Subdevice–ID = 0x0200 and the IMBF version register implemented.

2. Read the content of the IMBF version register

3. If IMBF=0xFFFF or 0x0000, → IPSO 19" Unit

    1. Read the version register SLOT_BRDV on each Controller

    2. SLOT_BRDV=0xXFXX or 0xX0XX → 2MB external RAM on this Controller and DSP TMS320C6415
    SLOT_BRDV=0xX1XX → 16MB external RAM on this Controller and DSP TMS320C6415
    SLOT_BRDV=0xX2XX → 128MB external RAM on this Controller and DSP TMS320C6455

4. If IMBF= 0x0001, → IPSO AQS → IPSO AQS HOST including RxController with 2MB external RAM and DSP TMS320C6415

    1. Read the board version of IPSO AQS ACQ out of the T_BRDV register

    2. T_BRDV=0x0000 → TxController with 16MB external RAM and DSP TMS320C6415 on IPSO AQS ACQ

    3. T_BRDV=0x0200 → TxController with 128MB external RAM and DSP TMS320C6455 on IPSO AQS ACQ

Table 7: IPSO Versions

IMBF				T_BRDV		SLOT_BRDV				
variations			model	rev.	subrev.	slot	ver sn.	subv.		
F	F	F	F							IPSO 19" Unit
0	0	0	0							
						X	F	X	X	TxController of IPSO 19" Unit ext RAM 2MB, DSP TMS320C6415
				not used		X	0	X	X	
						X	1	X	X	TxController of IPSO 19" Unit ext RAM 16MB, DSP TMS320C6415
						X	2	X	X	TxController of IPSO 19" Unit ext RAM 128MB, DSP TMS320C6455

IMBF		T_BRDV		SLOT_BRDV			
variations	mo del	rev.	subrev.	slot	ver sn.	subv.	
							IPSO AQS HOST, RxController with ext. RAM of 2MB, DSP TMS320C6415
0 0 0	1	0 0	0 0		not used		IPSO AQS ACQ, 5 TxController, ext. RAM 16MB, DSP TMS320C6415
		0 2	0 0				IPSO AQS ACQ, 5 TxController, ext. RAM 128MB, DSP TMS320C6455

Figure 8: Host bus of the IPSO 19" Unit
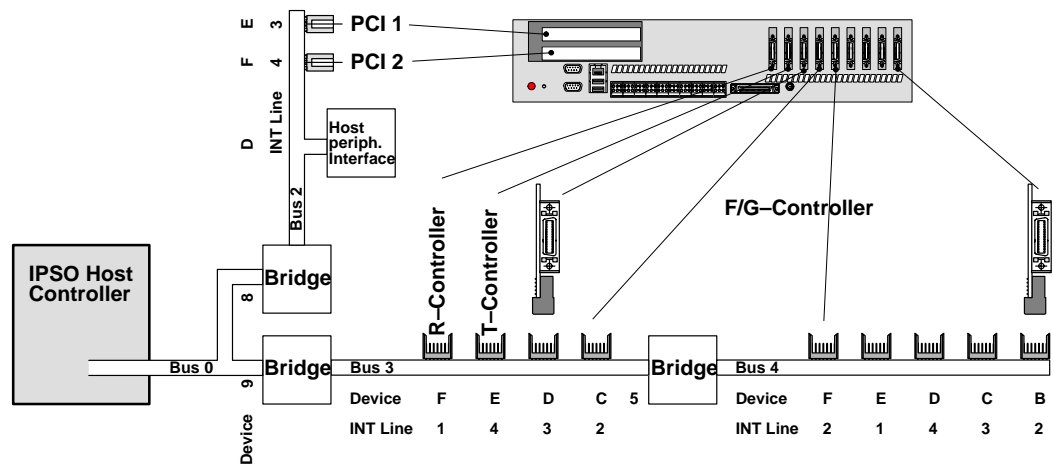
Note: Inserting PCI cards with on–board bridges implies adding further bus segments which can in turn change the bus numbers!

Figure 9: Host bus of the IPSO AQS
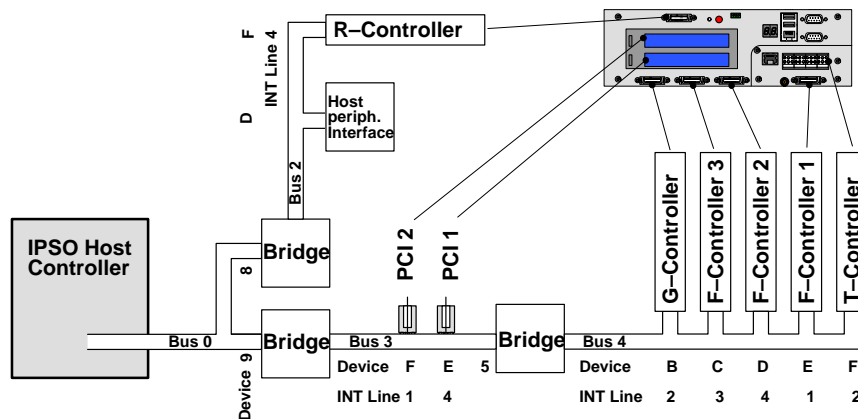
Note: Inserting PCI cards with on–board bridges implies adding further bus segments which can in turn change the bus numbers!

Checking the Configuration

Modification of the system (by inserting or removing controllers or PCI cards) should always be followed by checking the system–recognized structure against the expected one. For instance, "has the system accurately recognized the number and the type of all inserted controllers?".

Starting the ipsotest when logged in at the IPSO

```
root@IPSO:/opt/test>ipsotest ↵
```

returns a list of all recognized controllers, their bus and device numbers and their application specific utilization. Bus bridges, general PCI devices and interrupt routings are not shown.

A complete list of all PCI devices and interrupt routings is shown by typing

```
root@IPSO:/opt/test>cat /proc/pci ↵
```

> **Note:** Devices on bus0 and bus1 are not application relevant!

1. 6. Power Supply

Checking Temperature and Voltages

Typing "mbmon –A" when logged in at the IPSO

```
root@IPSO:/opt/test>mbmon -A↵
```

returns something like the following values provided by voltage and temperature sensors:

On IPSO 19" Unit

Temp.=	82.0	80.5	80.5			(so far, June 2006, these values are not correct)
			next to the Voltage Regulators			
		next to the Sequencer				Sensor location on the IPSO Base Board
	below the Host Controller (PC–Module)					
Rot.=	0	0	0			Fan speed; not implemented
Vcore=	1.30	3.41				Core voltage of the Host Controller
Volt.=	3.41	5.03	12.46	−11.87	−5.25	Voltages of the Power Supply

> **Note:** The –5Volt from Power Supply is not used!

On IPSO AQS

Temp.=	82.0	80.5	80.5			(so far, these values are not correct)
			next to the RxController			Sensor location on IPSO AQS HOST
		next to the PCI connector				Sensor location on IPSO AQS ACQ
	below the Host Controller (PC–Module)					Sensor location on IPSO AQS HOST
Rot.=	0	0	0			Fan speed; not implemented
Vcore=	1.30	3.41				Core voltage of the Host Controller
Volt.=	3.41	5.03	12.46	−11.87	−5.25	Voltages of the Power Supply

Power Conditions on the IPSO 19” Unit

Currents and Voltages

Part–No.	Assembly		+5V	Σ +5 V	+3,3V	+12V	+5VSB	−12V
H12519	IMB	ETX 400Mhz + IMB		2,5 A	2,5 A	0,1	(1,8A)	0,1
		2 PCI Slot (25W)		10 A				
		70 RCP/30 mA		2,1A				
H12538xx	TxController	1x(0,3+0,3)	0,6 A		0	0		0
		8x		4,8 A	0	0		0
H12532xx	RxController	1x	0,6 A	0,6 A	0	0		0
Current required from ATX Power Supply				20,0 A	2,5 A	0,1 A	(1,8A)	0,1 A
Power				108,25 W				
				109,45 W				
				118,15W				

Used Power Supply

Any ATX Power Supply with the same Formfactor can be used. The installed one is ATX Version 2.03 compliant with 20–Pin Power Connector. Since –5Volt are not required, Power Supplies with 24–Pin Connectors (ATX12V Version 2.2) also meet the requirements but need an adapter.

The Nipron Power Supplies are said to run 24 hours a day during 10 years.

The Reliability Grade is "Factory Automation" instead of "Office Automation".

The Fan can be replaced without disassembling either the Power Supply or the IPSO.

General Specifications			Continuous Output Specifications				
			+5V	+3.3V	+12V	+5VSB	−12V
Part–No.	87451		21 A	14 A	10A	1,5 A	0,8 A
Manufacturer	Nipron		125 W				
Type	eNSP–300P–S20–00S		185 W				
Continuous Power	200W		203 W				
Peak Power	300W						
Input	AC85~264V						
MTBF	100,000 hours						
Safety Standard	UL, CSA(c–UL), EN, CE						

Power Conditions on the IPSO AQS

Currents and Voltages

Part–No.	Assembly			+5 VSB	Σ +5 V	+3,3 V	+12 V	−12 V	analog +5V
H12549	IPSO AQS ACQ	5x TxCon-troller				5x0,6 A			
		28 RCP			0,9 A				
		Generation of 2,5 V				1,5 A			
Sum of ACQ					0,9 A	4,5 A			
H12547	IPSO AQS Host	ETX 400Mhz		1,5A	2,5 A	1,6 A	0,1 A	0,1 A	
		RxController				0,6 A			
		2 PCI Slot (25W)			10 A				
Sum of IPSO AQS					13,4 A	6,7 A	0,1 A	0,1 A	
Supplied to AQS/3					8,2A		6,7A	0,01A	6,9A sepa-rated GND
Required from Power Supply				1,5 A	21,6 A	6,7 A	6,8 A	0,11 A	6,9 A

Used Power Supply

The Power Supply of the IPSO AQS is a VME–Bus power module with a Formfactor of 12TE/6HE. This module is a special design of GERMAN POWER and can not be replaced by any commercially available device.

This Power Supply meets "ATX Power Supply Design Guide, Version 2.2" except for necessary variations like form, currents, voltages and connectors.
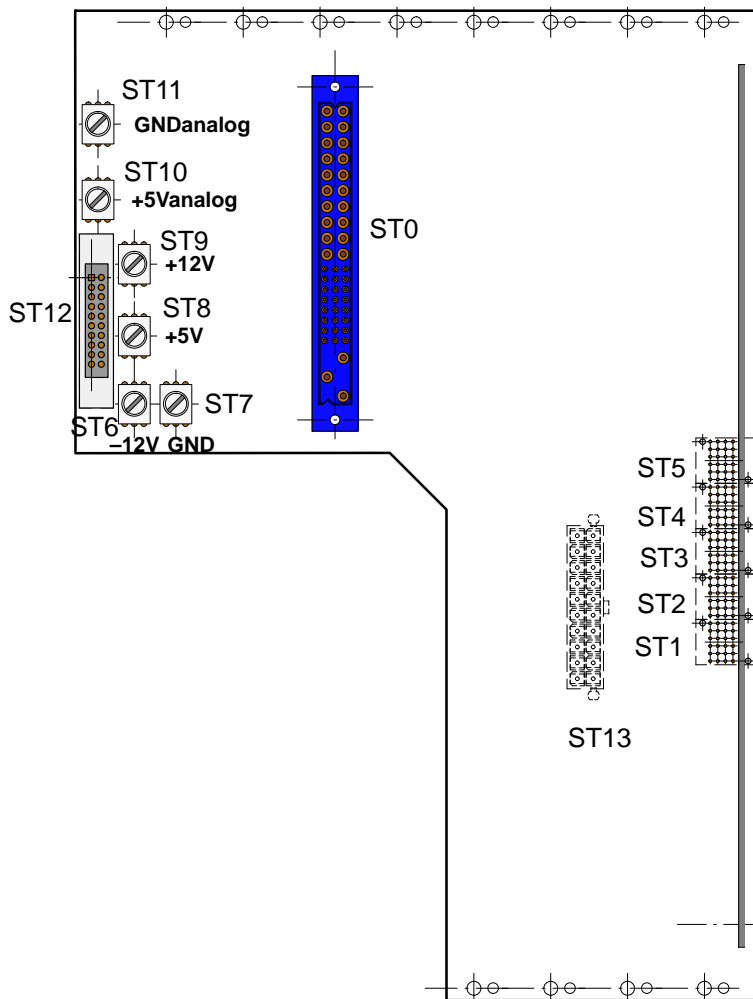
The Power Supply has to be cooled from outside (no fan inside).

General Specifications			Continuous Output Specifications					
			+5VSB	+5V	+3.3V	+12V	−12V	analog +5V
Part–No.			2,0 A	25,7 A	12,1 A	10A	0,2 A	10 A
Manufacturer	German Power							
Type	BSAA350–230W–6							
Continuous Power	350W		350W					
Peak Power								
Input	AC100~240V							
Safety Standard	EN, IEC, UL, CSA(c–UL), CE							

IPSO AQS Power Backplane

Table 8: IPSO AQS Power Backplanes

IPSO AQS (microbay)
Back View

IPSO AQS (nanobay)
Back View

ST11
GNDanalog

ST10
+5Vanalog

ST9
+12V

ST8
+5V

ST12

ST0

ST6   ST7
−12V GND

ST5
ST4
ST3
ST2
ST1

ST13

ST0

ST11
GNDanalog

ST10
+5Vanalog

ST9
+12V

ST8
+5V

ST7
GND

ST12

ST6
−12V

ST13

ST5
ST4
ST3
ST2
ST1