BRUKER

Bruker BioSpin

AQS with IPSO Systems

Technical Manual

Version 002

think forward

NMR Spectroscopy

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WARNING: Disregard of this may lead to personal injury.

NOTE: Hint for good operating practice.

Figure 1.1. High voltage!

Indicates dangerous voltage. Do not open cover with this label!

Figure 1.2. Dangerous device!

Instruction manual symbol. It is necessary for the user to refer to the manual prior to the use of marked items.

Figure 1.3. Electrostatic sensitive Device!

Observe precautions for handling.

Figure 1.4. Protective ground (earth) terminal

Used to identify any terminal which is connected to the external protective conductor for protection against electrical shock in case of fault.

Disclaimer 1.2

The following general safety precautions must be observed during all phases of operation and service of the AQS system. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture and intended use of the AQS system.

BRUKER assumes no liability for the customer‘s failure to comply with theses requirements and is therefore not responsible or liable for any injury or damage that occurs as a consequence of non-approved manipulations on the AQS system.

Emergency 1.3

The mains switch on the AQS chassis front serves as an EMERGENCY OFF. It powers down the systems.

Personnel safety *1.4*

Ground connection *1.4.1*

WARNING: To minimize shock hazard the AQS chassis must be connected to an electrical ground.

The electronics cabinet is equipped with a three-conductor ac power cable. Do only use power cables approved by BRUKER or compliant with IEC safety standards.

Technically qualified personnel only *1.4.2*

WARNING: Installation and servicing should only be done by BRUKER qualified personnel. Always disconnect power cable before servicing. Under certain conditions dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

NOTE: Operating personnel must not remove chassis covers except as described in this manual. Do not replace AQS units with mains switch turned on.

User interface, system messages, and manuals require a good understanding of the English language.

Electrical safety *1.4.3*

The AQS systems's degree of protection against electrical hazard complies with IEC IP20, i.e. all electrical parts are protected against touching.

WARNING: All electrical connectors must be used as supplied by BRUKER. Do not substitute them by other types.

Lifting the AQS chassis *1.4.4*

WARNING: At least two people are needed to insert and remove the AQS chassis from the electronics cabinet. A fully equipped AQS system can weight in excess of 50kg.

NOTE: Remove some or all of the AQS units from the chassis prior to handling to reduce weight.

Cleaning *1.4.5*

WARNING: Always switch power off and disconnect the power cable before cleaning. Never power on until all surfaces are completely dry.

Clean the outside of the AQS chassis and units with a soft, lint-free cloth dampened in water. Do not use any detergent or other cleaning solvents.

IPSO Acquisition System

2

Introduction 2.5

The first Acquisition System (named AQS) was introduced into the market in 1999. The main reason was the development of a BRUKERs own synthesizer (SGU) based on a novel channel concept. The architecture of the former AQR and AQX units have been unified, higher integrated and more standardized. During the last years the architecture has been completed with additional and more diversified configurations still based on a unified hardware and software concept. With this it was possible i.e. to enhance Solids configurations (RX-BB instead of SE451), to higher integrate High Resolution spectrometer electronics (AQS integrated LNA preamplifiers instead of HPPR), to generate new MRI solutions (Pharmascan and Biospec with multiple RX) and standardize the FTMS platforms (SGU FTMS).

The next generation (named AVANCE II) was the introduction off a new receiver system. The former RCU, RX-22 and the HADC/2 and SADC were replaced by the new DRU and RXAD (equipped in the also new AQS/2 chassis) which brought a much higher integration and increased performance.

The next step was the replacement of the VME boards, such as CCU, FCU, TCU and GCU by the recently introduced IPSO (intelligent pulse sequence organizer). The new IPSO compatible SGU/2 is the successor of the former SGU with a much faster and wider digital interface for setting all relevant pulse program parameters such as frequency, phase and amplitude. A package of frequency, phase- and amplitude-words together with some relevant real time pulses can be set synchronously every 25ns via the 80MHz and 48bit wide LVDS link. The setting via the synchronous and differential LVDS link guarantees an excellent isolation between digital computer electronics and purest RF signals.

The new SGU/2 incorporates many more features, such as a pre-viewer for all hardware relevant pulses. So on one has to worry about different hardware required delays. All pre- and post-delayed pulses such as transmitter, preamplifier and receiver gating are generated automatically and must be initialized only once. Therefore the users can fully focus on the NMR sequence and only have to deal with “ideal” pulses.

The new AQS/3 chassis is the consecutive development of the well proven AQS/2 chassis and can now with equipped by the new IPSO AQS Unit. The extended IPSO 19“ Unit represents a stand alone unit and doesn’t fit into the AQS/3 chassis.

Features

- Prepared for up to 10 6TE RF and other NMR electronic units
- Support of the recently new developed **IPSO AQS Unit**
- Expandable with additional, integrated power amplifiers (i.e. AQS 2H-TX)
- Support of mixed systems (HR and multiple RX imaging) by a versatile backplane pulse routing under software control

- Increased flexibility by the operative introduction of the „scan control“ mechanism (sample information bus)
- Fan operation supervision and easy serviceable fan tray

Figure 2.5. 2 Channel AQS/3 with RXAD and DRU

Acquisition control

By the elimination of the acquisition control and data transfer via the CCU and VME bus, a powerful synchronization channel is available. The already in the basic channel concept defined „sample information bus“ is being used for the control of the realtime actions in the digital receiver chain. Synchronous scan information (e.g. receiving phase, file handle, wobble control, accumulation and display management) is distributed over this bus from the acquisition main controller (timing control) via the observe SGU/2. This bus replaces and enhances the well working AQ Bus within the receiving concept.

Analog to Digital Conversion

Newest A/D converter technologies allow sampling rates up to 20MHz with very high dynamic ranges. In conjunction of the tremendous progress in digital signal processing (DSP technology) and very fast and highly integrated flexible digital hardware (FPGA based) it allows enormous higher DQD bandwidths and with that less audio artefacts as anyone could expect in earlier times.

Automatic DC compensation, higher frequency digital local oscillators (NCO, numeric controlled oscillators) and last but not least better performance is also achieved by continuos A/D converter operation (non start/stop mode). Inherent thermal settling of the A/D chips by using start/stop mode disappears. The DWELL clock is derived directly from the basic phase noise minimized spectrometer reference increasing the spectral purity. Finally the DWELL clock generation

for such a system is much easier, because the gating is handled in the DSP by managing the data flow using previously mentioned ‚scan control'.

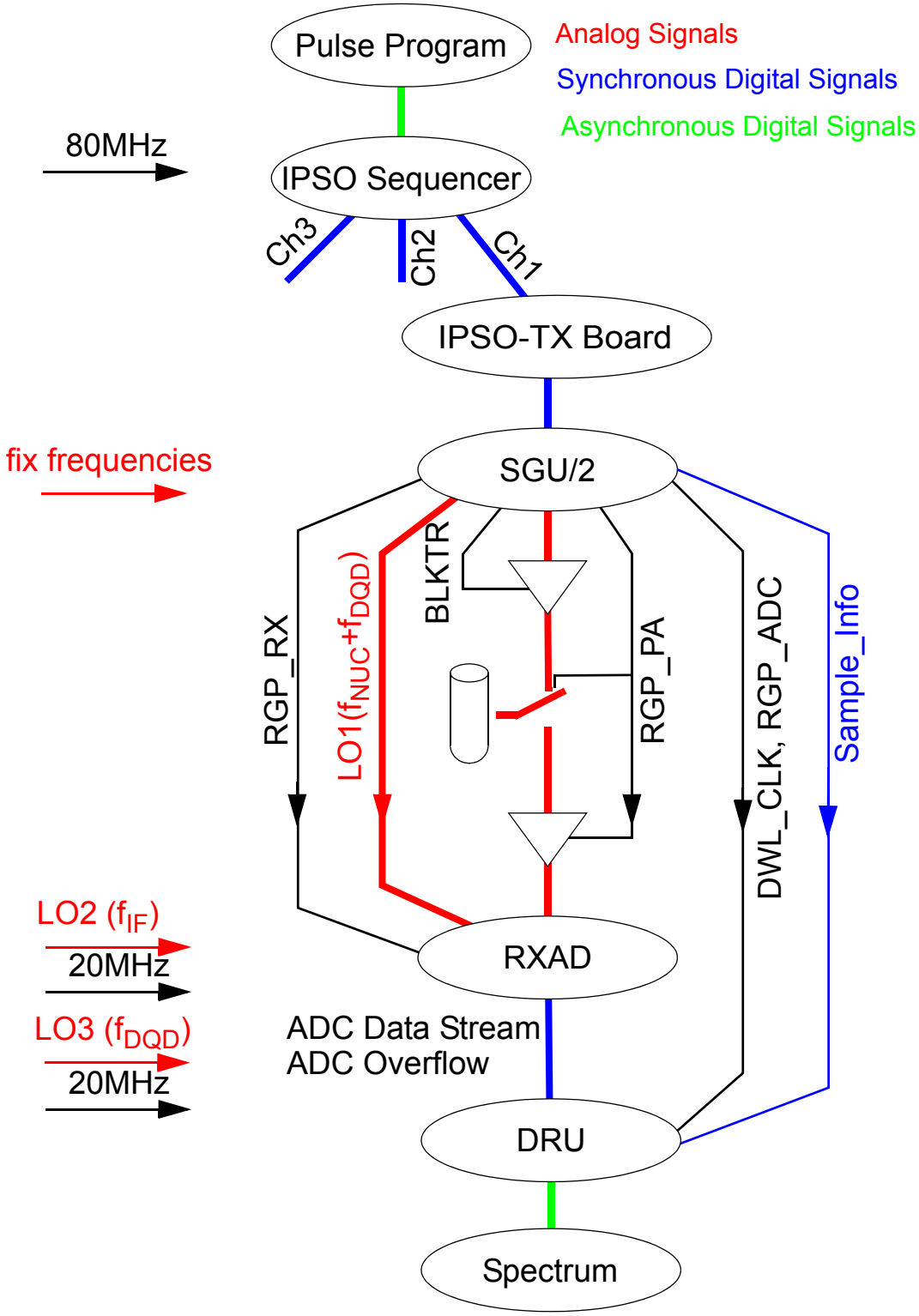
The channel concept *2.6*

With the introduction of the AQS/3 Chassis, the well proven AQS channel concept has been further extended by the replacement of the former TCU/FCU and GCU units with the recently developed **IPSO AQS Unit** and **IPSO 19" Unit**.

It was possible to reduce the control and routing of important channel related real time events and analog signals to only a few dedicated units. All these channel oriented signals (RF signals, shaping, gating and blanking pulses, dwell clocks etc.) are generated in the so called SGU/2 (**S**ignal **G**eneration **U**nit) under full timing control of pulse programs. The SGU/2 is physically controlled by the IPSO via a digital high speed link.

The following diagram shows the consequent implementation of this concept. The number of analog interconnections is reduced to a few dedicated units. All important RF signals, blanking pulses and dwell clock are channel related and follow a straightforward channel philosophy. In this way, extended and independent multi channel operation can be performed in a much more transparent way. Less interfaces and units allow a general guaranteed stability and reliability.

The channel concept



AQS/3 signal and information paths 2.7

Before going into details, it is important to distinguish and understand the three different signal categories used in the AQS/3 Chassis (as already introduced with the former AQS Chassis):

Analog signals: These signals are typically RF signals, which have no time and amplitude discrete values and may be easily checked with a scope. Examples of such signals are the local oscillator signals (i.e. LO1 and LO2).

Synchronous signals: These signals are the basic spectrometer auxiliary, control and timing signals for each transmit but also receive channel. They are all derived from one master oven controlled oscillator (OCXO). Most important are the 10MHz, 20MHz, but also every transmitter blanking and the receiver gating pulse.

Asynchronous signals: Asynchronous signals fall into the category of general information transfer protocol signals. These signals are represented by examples like Ethernet, RS232, RS485 and I^2C.

Basics of the AQS/3 Chassis 2.7.1

The AQS/3 has been designed to support more than one chassis to allow a very flexible extension of NMR transmitting channels, multireceiving capabilities and setting up numerous different NMR application spectrometers configurations. To manage all these configurations, one has to select the required operation by selecting the appropriate rack code only. The rack code can be set with rotary switches on the rear side of the AQS/3 backplane (***"Rackcode Settings" on page 72***).

Viewing the AQS/3 chassis from the front, on the left a proprietary IPSO backplane is incorporated. On the right, the extended AQS/3 user bus is able to supply (as will be shown later on) a lot of different AQS functional units (signal generators, receivers, preamplifiers, amplifiers, etc.).

Every slot on the AQS/3 User Bus backplane is hardware coded, so that every unit can be addressed via its unique slot address. The AQS/3 user bus backplane connector pin assignment is identical for all ten 6TE slots. That means each common signal respectively signalpath is accessible on every slot (exceptions are power supply for BLA2BB, the data transfer to the DRU and signals for the reference board).

RS485 Buses (SBSB[1]), Intra Rack Bus 2.7.2

The AQS/3 incorporates two independent SBSB buses called SBSB_TTL and Intra Rack Bus. The first one represents the system tty10.

The RS485 buses are originating at the DRU, and are under control of other AQS Controller (DRU). They are hard-wired internally in the backplanes. The SBSB_1 is galvanic isolated (SBSB_TTL) on the PSD. This reduces interferences between NMR RF, audio and digital units.

1 SBSB: serial BRUKER SPECTROSPIN bus (historical name)

The DRU serves as the ‘rack master’ or *AQS Controller*. This *AQS Controller* overtakes general control and configuration tasks in the initialization phase which must be setup according to the rack address. The AQS Controller reacts to ‚master‘ commands (e.g. power up, init...) incoming via the tty10 from the spectrometer control software via ethernet. It also reacts to incoming virtual SBSB commands for devices which do not have own SBSB interfaces (refer to I^2C bus).

Internal AQS/3 communication between AQS/3 SBSB devices like SGU‘s and RXAD (e.g. clearing power up errors etc.) is done via the so called Intra-Rack bus (serial asynchronous bus, TTL levels) with the AQS Controller as bus master.

I^2C buses and I^2C adresses *2.7.3*

For functional units without an intelligent and powerful micro controller, because it doesn‘t calculate to have an own costly controller, a multi master capable I^2C connectivity is used. The AQS Controller drives these units via different I^2C buses and plays so the role of a virtual unit controller for each non microprocessor unit. Such units are the AQS BLA2BB, the AQS 1 to 4 Router, AQS REF but more may be coming soon. Incoming spectrometer SBSB commands from tty10 for I^2C devices are converted by the AQS Controller to I^2C commands.

Example: To set the ‚Mini ROUTER‘ located within the BLA2BB, the incoming tty10 command from the acquisition control software is transformed into I^2C compatible commands and then sets up the minirouter inside the BLA2BB.

To exceed the limitation of max. 8 I^2C devices a second I^2C bus is located on the AQS/3 User Bus backplane to allow the control a total of 16 I^2C slaves.

High Speed Link *2.7.4*

The high speed link (LVDS[1]) from IPSO-TX Board to SGU/2 transfers all NMR relevant real time events originating from the pulse program in 25ns time intervals to corresponding SGU/2 (e.g. pulses, shapes, phase jumps, frequency jumps, etc.). Each RF channel is connected by a separate high speed link to the IPSO-TX Board. To allow a flexible extension of NMR channels, the wiring is located on the front side of the corresponding boards. To allow highest speed, a point to point connection architecture has been chosen.

Similarly the A/D converter output of a RXAD is coupled to the DRU via its own and well proven LVDS high speed link. With that it is possible to transfer a complex digital data point (real and imaginary) within 50ns and so allowing DWELL clocks up to 20MHz. Because each receiver channel consists of one RXAD and one DRU this link is physically located on the AQS/3 user bus, allowing to minimize cable connections on the front side.

Sample Info *2.7.5*

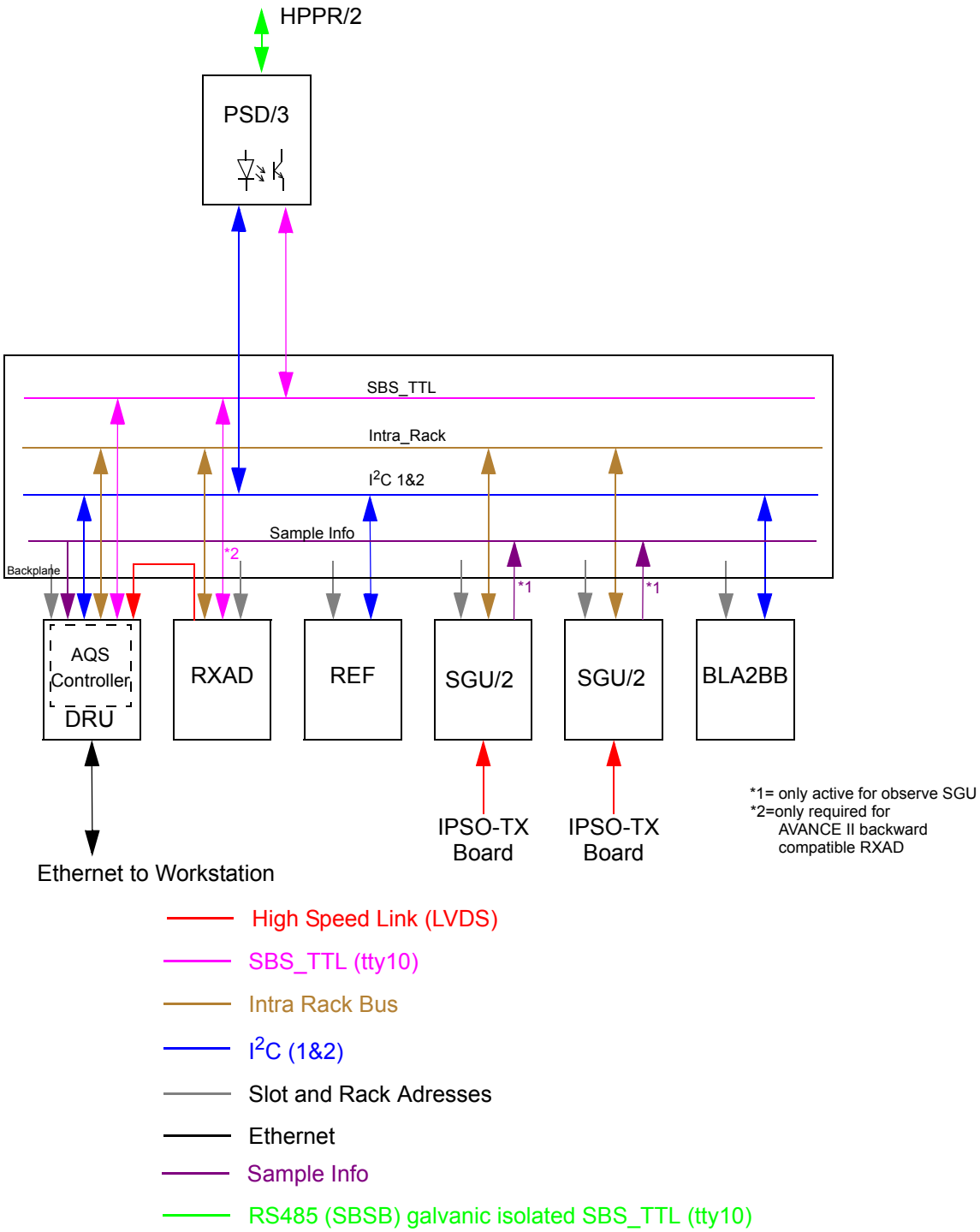
As already prepared on the AQS Chassis backplane a synchronous information mechanism for each acquisition named as „sample info“ has been established to

1 LVDS: Low voltage differential signaling

control the receiver signal and process chain. It is now possible to handle the receiver phase on the DRU by pulse program commands.

The sample information is stored on the workstation disk together with the acquisition data. This provides full synchronicity of the scans. The acquisition data can easily be traced on the disk file by storing the complete set of ‚sample information'.

Figure 2.6. AQS/3 Buses for a two channel system (internal BLA)



Synchronous signals 2.8

Realtime control-pulses (RCP) on the AQS/3 User Bus 2.8.1

BLKTRx~ (Blanking pulses for power amplifiers)

Each BLKTR must be routed to the corresponding power amplifier. A SGU/2 can control up to 8 power amplifiers with the corresponding BLKTR. The SGU/2 must be initialized via Intra Rack bus before starting the experiment. Each SGU/2 will apply under high speed link control the required BLKTR pulse in real time onto the AQS/3 User Bus backplane. The BLKTR has wired nor logic on the backplane so that BLKTRs from different SGU/2 can be combined to one amplifier (easy pulseprogramming, channel concept).

No additional cables are necessary to control the internal power amplifiers (e.g. BLA2BB). The BLKTR are routed directly on the backplane from the SGU/2 to the corresponding BLA channel. BLKTR for external power amplifiers may be accessed on the front of the power supply and distribution board (PSD/3).

RGP_PA~ (Preamplifier receiver gating pulse)

This pulse (also mentioned as RGP_HPPR) is controlled by the SGU/2 which is initialized as observing SGU/2. This signal is routed via the PSD to the observe module in the preamplifier HPPR/2. All other non lock HPPR/2 modules are in transmit or decoupling mode.

Note: In contrast to previous AVANCE systems, the preamplifier RGP will not be connected to the AQR RX22 but to RXAD for multi receiver configurations only.

RGP_LO~ (Local oscillator gating pulse)

This internal pulse enables the local oscillator generation inside the RXAD. The pulse is automatically generated by the observe SGU/2 after switching to receive mode.

RGP_RX~ (Receiver gating pulse)

This pulse controls the gating inside the receiver e.g. the RXAD. The pulse is driven by the observe SGU/2. The signal is directly routed from the observe SGU/2 via AQS/3 User Bus backplane to the receiver RXAD. With this signal the receiver may be ‚opened' later in respect to the preamplifier to prevent saturation.

Dwell_Clk~ (ADC dwell clock)

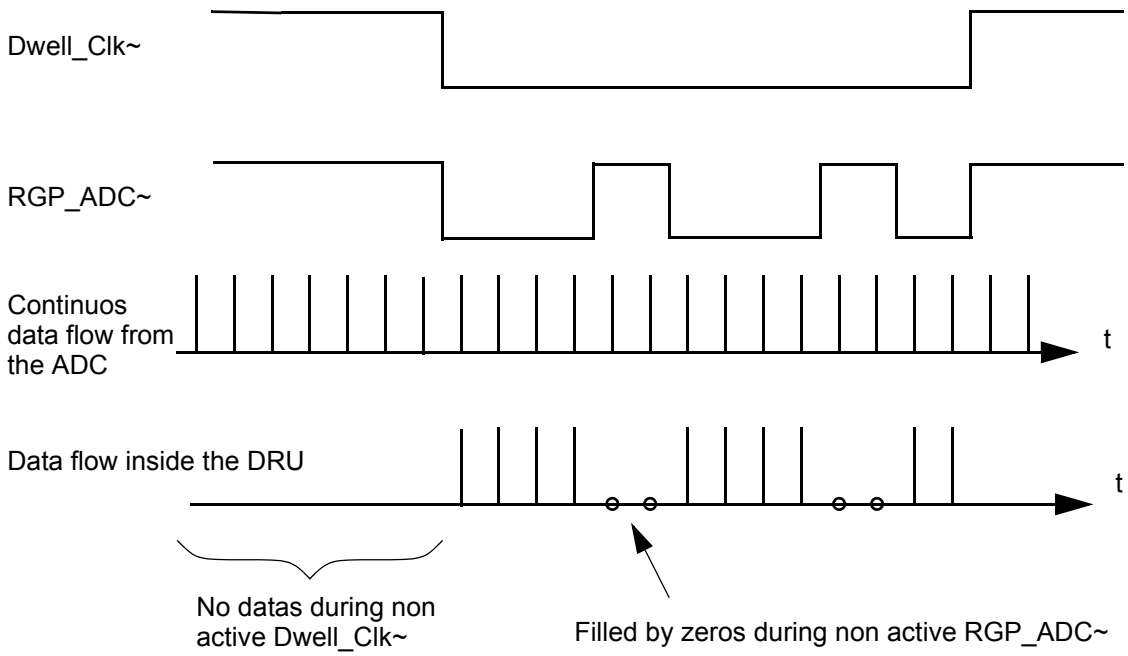
In fact the Dwell_Clk~ changed operational behaviour in respect to previous AVANCE systems. It serves as a dwell enable and with that doesn‘t reflect the physical AD converter rate. The AD converter rate is fixed to an oversampling frequency of 20MHz, is running continuously and the data stream is being enabled (gated) by the Dwell_Clk~ inside the DRU. The signal is also driven by the observe SGU/2.

RGP_ADC~ (ADC gating pulse)

This pulse (also driven by the observe SGU/2) controls the ADC data stream. For a non active RGP_ADC~ the data stream is filled with zeros inside the DRU, during the active pulse, ADC data is passed unchanged.

This signal is specially used for experiments like digital homodecoupling with oversampling.

Figure 2.7. Explanation of Dwell_Clk~ and RGP_ADC~



Sample Info

The Sample Info channel consists of the five lines SAMPLE_INFO(4:0) originating at the corresponding SGU/2. The interface is synchronous to the 20 MHz system clock (20MHZ_CLK) and hence the word rate is 20MW/s

The scan control commands have a fixed length of 6 words. Bit 4 of the first word carries the start bit which is always 1. Bit 4 of the last word must be set to 0. With that, all listeners to these lines are able to synchronize to the information contained within burst sent under pulse program control.

In between two Sample Info bursts, a recovery time of 10us must be granted.

The information is clustered to two groups, each with an individual enable bit:

The first group (enabled by bit „ScanCtrl“) carries information which must be available before a scan (e.g. scan phase, memory buffer, accumulation control). This information is associated to the upcoming scan.

The second group (enabled by bit „WriteCtrl“) carries information on how to proceed with a scan that has been readily accumulated (e.g. file seek, file change). This information is associated to the past scan.

Table 2.1. Data format of the 6 sample info words (5 Bits each)

word	Bit4 Pin E3	Bit3 Pin C2	Bit2 Pin D2	Bit1 Pin E2	Bit0 Pin E1
1	1 (Start)	ScanCtrl	PhaseRun	Phase (0,90,180,270)	
2	reserved=0	st0	st	zd	ze
3	OffsMeas	DruParamIndex			
4	WriteCtrl	FileNumber (0-15)			
5	reserved (set zero)		Write	Seek	
6	0 (Stop)	reserved (set zero)			

ScanCtrl

Enable bit for the first group. This bit must be set to prepare an upcoming scan.

PhaseRun

If this bit is set, the phase accumulator immediately starts running (synchronously to the Sample Info). If this bit is cleared, phase accumulation is delayed until Dwell_Clk~ becomes active for the first time.

Phase

Accumulation phase.

0 = 0 deg
1 = 90 deg
2 = 180 deg
3 = 270 deg

st0 , st

Controls the memory buffer handling.

st0,st	
0,0	accumulate the upcoming scan to the current buffer
0,1	accumulate the upcoming scan to the next buffer
1,0	accumulate the upcoming scan to the first buffer
1,1	reserved

zd, ze

Controls the accumulation.

zd,ze	
0,0	add the upcoming scan to the buffer
0,1	write the upcoming scan to the buffer
1,0	write the upcoming DummyScans+1 scans to the buffer
1,1	reserved

OffsMeas

This bit is partially independent of the groups „ScanCtrl“ and „WriteCtrl“ and triggers the DC offset calibration. The filed „DruParamIndex“ is co-used with „ScanCtrl“ but besides of this it is independent of the other two groups.

Dwell_Clk~ and RGP_ADC~ must be active for at least 1ms. During this time the DC offset is measured by averaging 16384 ADC samples.

DruParamIndex

These four bits select one out of 16 preloaded acquisition parameter sets. This is intended for interleaved acquisition, where all parameters have to change on the fly. (e.g. SWH, TD, DC offset)

WriteCtrl

Enable bit for the second group. This bit must be set to write a scan to disk.

FileNumber

These four bits select one of 16 disk files to write to or to manipulate the file pointer. Data source is always the memory buffer of the last acquisition.

„FileNumber“ can be chosen independently of the preloaded acquisition parameter sets (addressed by „DruParamIndex“) in the range 0-15.
(DataSetList, ifp, dfp, rfp):

0-12: directly access the files 0-12
13: use current file, then decrement file number
14: use current file, no change
15: use current file, then increment file number

Write (wr)

„Write“ = 1: Write TD*NBL samples to the file selected by „FileNumber“.

„Write“ = 0: disk file pointer manipulation only.

Seek (if,df,rf)

Manipulate the disk file pointer of the file „FileNumber“.

All 16 disk file pointers are cleared at experiment setup time.

0=none
1=increment disk file pointer by TD*NBL
2=decrement disk file pointer by TD*NBL
3=reset disk file pointer

SEL_ADCx~ (Select A/D converter)

Obsolete.

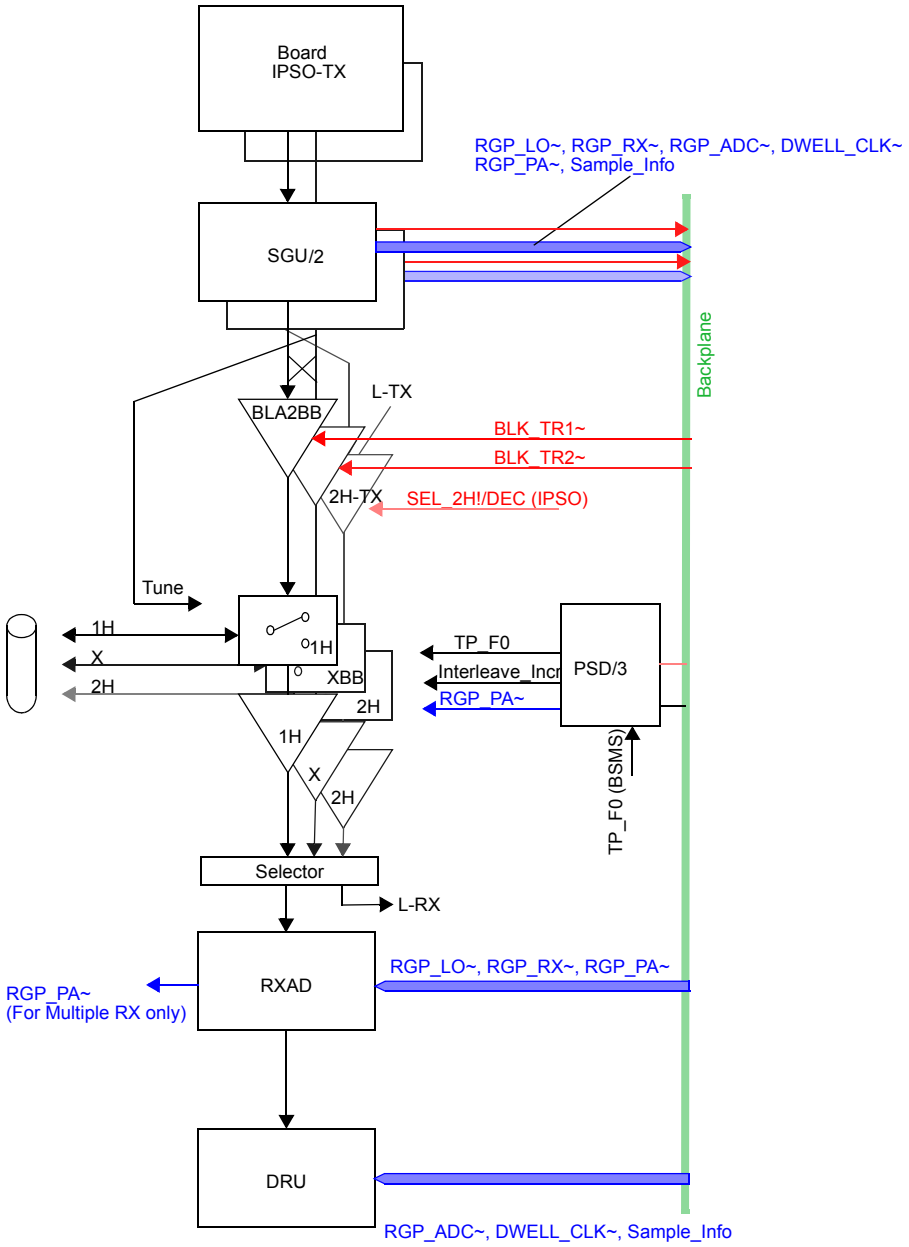
Interleave_Incr~

This pulse allows to switch between different preloaded modes under pulseprogram control. E.g. real time switching between 2H lock mode and 2H decoupling mode of the HPPR/2 can be controlled via this pulse or different receiving parameters can be selected during the experiment for interleaved acquisition.

ADC Overflow

The ADC Overflow signal indicates an overdriven analogue to digital converter. Data are useless in such a situation, a corresponding error message will occur.

Figure 2.8. Pulse distribution on a two channel AVANCE (internal amplifiers)



In this configuration three amplifiers exist but only two SGU/2.
SGU/2 (2) can either be used for the BLA2BB or the 2H-TX (for 2H decoupling or 2H shimming).
There is no blanking pulse required for the 2H-TX.
Controlling Lock mode or 2H-TX mode is done via the signal SEL2H/!DEC) from the IPSO

Receiver pulse separation for multiple-receiver systems *2.9*

All receiver specific pulses must be separated between receivers in multiple receiver systems. These pulses are:

- RGP_PA~, RGP_LO~, RGP_RX~, RGP_ADC~
- DWELL_CLK~
- SEL_ADCx~
- SAMPLE_INFO(0:4), INTERLEAVE_INCR~

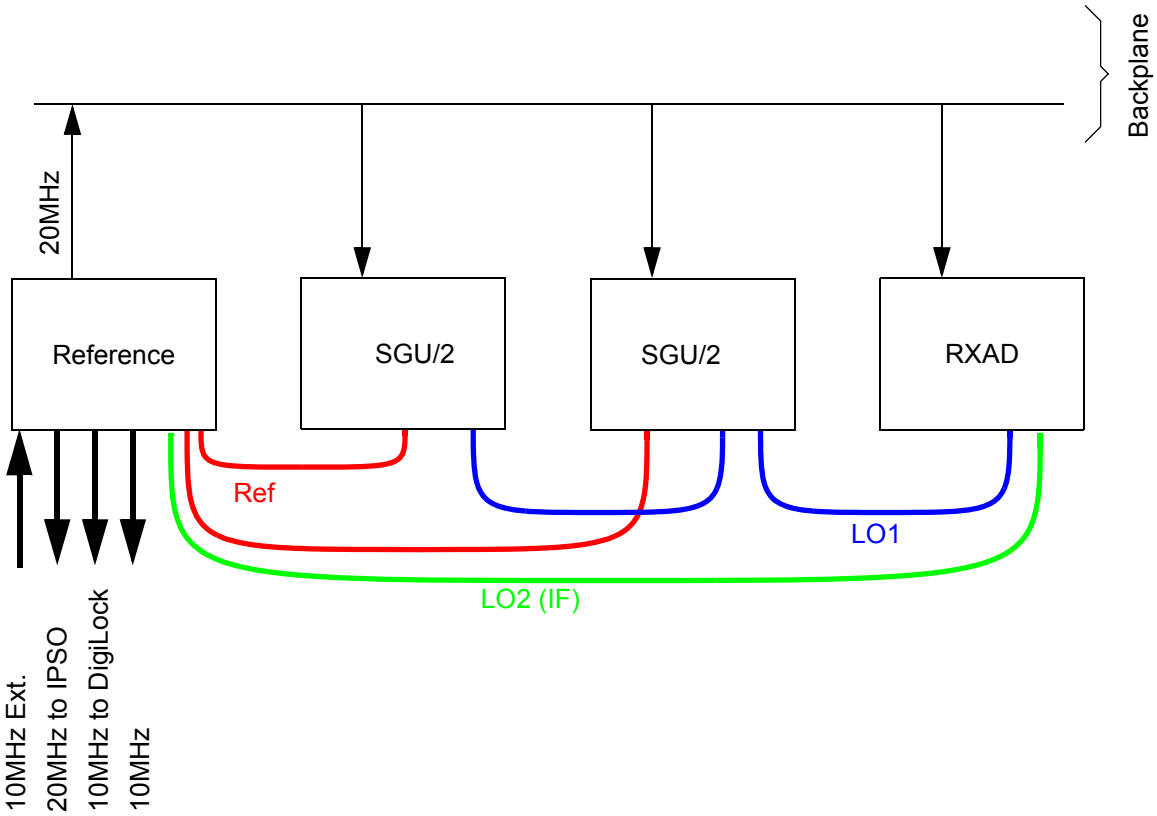
The separation is done with bus switch on the backplane. The bus switch are either controlled by rotary switch SW2 or via I^2C. Details see ***"Pulse switch for receiver pulse separation" on page 71***.

RF signal paths *2.10*

The following RF signals are required in a AQS system:

1. The RF output of every SGU/2 must be connected to a power amplifier or to a router/combiner.
2. Each SGU/2 can be initialized as observe SGU/2 and therefore each SGU/2 must be able to drive the local oscillator signal for the receiver. Every SGU/2 has a local oscillator input and a local oscillator output. The LO is looped through every SGU/2 except the observe SGU/2, which is driving the local oscillator.
3. Several fixed frequencies are generated on the reference board (AQS REFERENCE). These signals are required for the upconversion electronics located in the SGU/2. One reference board can drive up to four SGU/2.
4. The 10MHz output of the reference board is used to synchronize various units like the BSMS Lock. The reference board switches automatically to the external 10MHz input if a signal is applied.
5. The detection reference signal (LO 2) is directly wired from the reference board to the receiver.

Figure 2.9. RF distribution



20MHz Clock Distribution 2.11

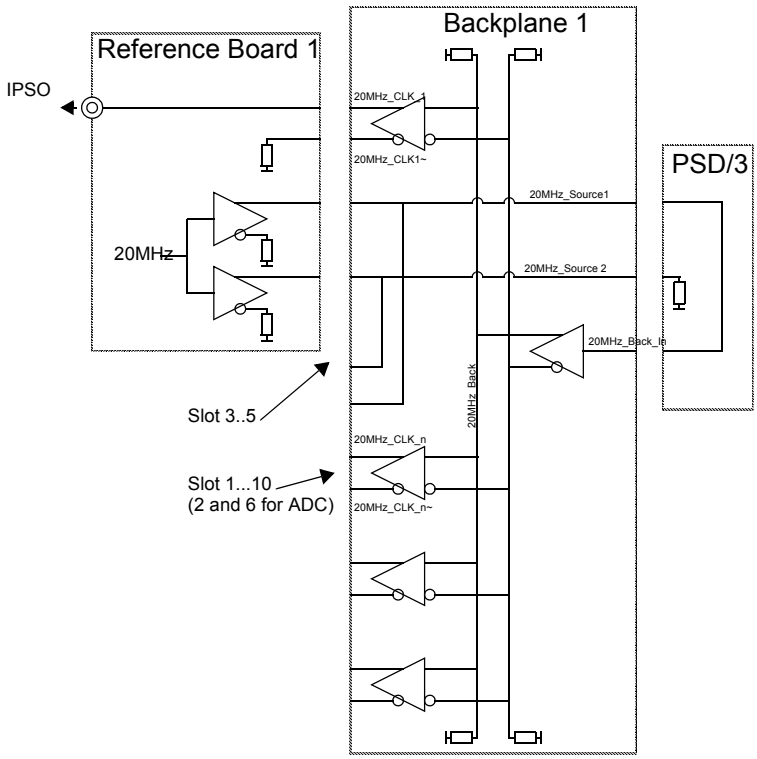
Introduction 2.11.1

This section describes the clock distribution for all AQS units. It's very important for a synchronous system to have a clock distribution with smallest skew between the different units.

Between the clock source and the various boards the same number of drivers and the same length of cable must be used.

Blockdiagram 2.11.2

Figure 2.10. 20MHz Clockdistribution



AQS/3 Configurations 3

IPSO Configurations with AQS/2 Chassis 3.1

The configurations in the following pages are described with the use of an AQS/3 chassis. However some configurations can also be assembled with the AQS/2 chassis. In these cases please observe the following notes:

- Only possible with external IPSO unit
- Use the AQS POWER SUPPLY DIGITAL 350W (H9489) for up to 4 SGU/2 and the AQS POWER SUPPLY DIGITAL 450W (H9520) for more than 4 SGU/2 instead of the IPSO AQS POWER SUPPLY
- AQS SGU, PSD, PSD/2, ACB-S and ACB-Extended are not IPSO compatible
- AQS/2 MEC-PARTS IPSO needed
- Rackcode setting see ***"Rackcode Setting Jumper JU1" on page 73***

A typical 2 to 3 Channel AQS/3 HR (200-400 MHz, internal BLA2BB & BLAX300) 3.2

Bill of Material 3.2.1

Table 3.1. Bill of material

Pos.	Units	Part Number	Description *Units for 3rd channel extension written in italics.*	MP[a]
1	1	Z106171	AQS/3 CHASSIS WIRED ECL ≥ 02 or SIH0303	
2	1	87577	IPSO AQS POWER SUPPLY	
3	1	Z12170 *W1345050*	BSMS FRONTPLATE BLIND 12TE *AQS POWER SUPPLY BLA 28V 20A*	MB
4	1	W1345050	AQS POWER SUPPLY BLA 28V 20A	
5	1	Z003403	AQS PSM2 POWER SUPPLY MODULE	
6	1	Z003402	AQS PSM1 POWER SUPPLY MODULE	
7	1	H14109	AQS PSD/3 BOARD	
8	1	H9984	IPSO AQS HR UNIT	
9	1	Z14118	AQS FRONTPLATE BLIND 8TE	MB

Table 3.1. Bill of material

Pos.	Units	Part Number	Description *Units for 3rd channel extension written in italics.*	MP[a]
10	1	Z100977	AQS DRU ECL ≥ 02	
11	1	Z102116	AQS RECEIVER BOARD RXAD 400	
12	1	Z003265	AQS REFERENCE BOARD 400	
13	2	Z103080	AQS SGU/2 400	
14	1	Z15201 *see pos. 13*	AQS FRONTPLATE 1MM 16TE *AQS SGU*	MB
15	1	Z15202 *W1345052*	AQS COVERPLATE 16TE *AQS BLAX300 6-243MHZ*	MB
16	1	W1345049	AQS BLA2BB150/60 20-400	
17	1	Z14133	AQS FRONTPLATE BLIND 2TE	MB
- [b]	10	25958	SCREW RRCH KR M2,5 x 12,3	MB

a MEC Part: MB = Part contained in AQS/3 MEC-PARTS MB (Z106936)

b use for pos. 3, 9 and 14

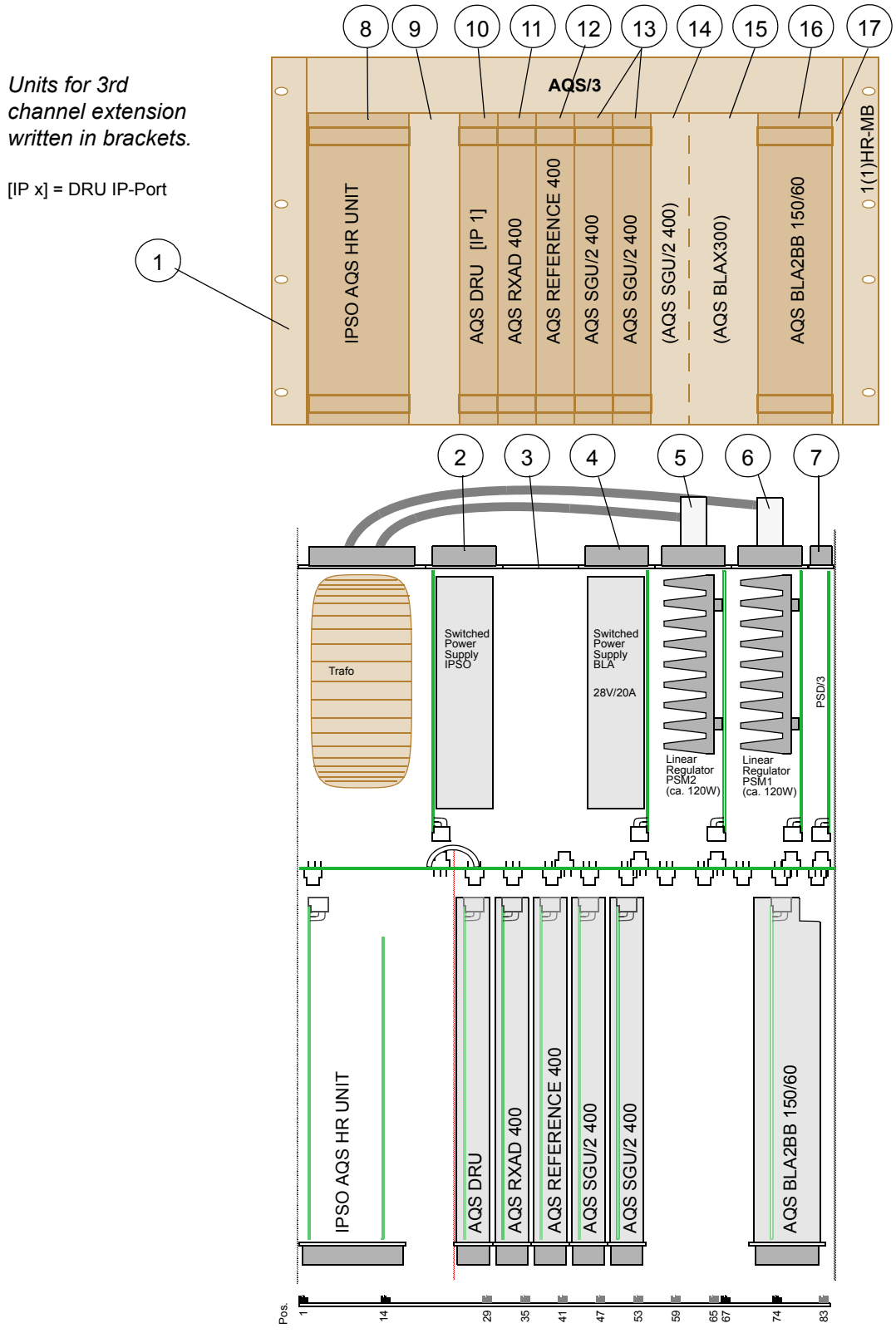
Rackcode Setting *3.2.2*

The rackcode must be set to ‘0x31’ (rotary switches on the AQS/3 user bus rear side: SW2 = 3, SW1 = 1).

For chassis with ECL ≤ 01 see ***"Rackcode Settings" on page 72***

The power-up delay must be set to ‘0’ (rotary switch on chassis rear side).

Figure 3.1. AQS/3 for 2 Channel AVANCE



A typical 2 Channel AQS/3 HR with internal PREAMP and BLA2BB (300 and 400MHz) *3.3*

Bill of Material *3.3.1*

Table 3.2. Bill of material

Pos.	Units	Part Number	Description	MP[a]
1	1	Z106171	AQS/3 CHASSIS WIRED ECL ≥ 02 or SIH0303	
2	1	87577	IPSO AQS POWER SUPPLY	
3	1	Z12170	BSMS FRONTPLATE BLIND 12TE	MB
4	1	W1345050	AQS POWER SUPPLY BLA 28V 20A	
5	1	Z003403	AQS PSM2 POWER SUPPLY MODULE	
6	1	Z003402	AQS PSM1 POWER SUPPLY MODULE	
7	1	H14109	AQS PSD/3 BOARD	
8	1	H9984	IPSO AQS HR UNIT	
9	1	Z14118	AQS FRONTPLATE BLIND 8TE	MB
10	1	Z100977	AQS DRU ECL ≥ 02	
11	1	Z102116	AQS RECEIVER BOARD RXAD 400	
12	1	Z003265	AQS REFERENCE BOARD 400	
13	2	Z103080	AQS SGU/2 400	
14	1	Z003950 Z003951	AQS 1H2H PREAMP 300 AQS 1H2H PREAMP 400	
15	1	Z003954 Z003955	AQS XBB19F 2HS PREAMP 300 AQS XBB19F 2HS PREAMP 400	
16	1	Z2778	BSMS FRONTPLATE BLIND 4TE	MB
17	1	W1345049	AQS BLA2BB150/60 20-400	
18	1	Z14133	AQS FRONTPLATE BLIND 2TE	MB
- [b]	10	25958	SCREW RRCH KR M2,5 x 12,3	MB

a MEC Part: MB = Part contained in AQS/3 MEC-PARTS MB (Z106936)

b use for pos. 3, 9 and 16

Rackcode Setting *3.3.2*

The rackcode must be set to ‘0x31’ (rotary switches on the AQS/3 user bus rear side: SW2 = 3, SW1 = 1).

For chassis with ECL ≤ 01 see ***"Rackcode Settings" on page 72***

The power-up delay must be set to ‘0’ (rotary switch on chassis rear side).

Important Notes *3.3.3*

50 Ohm Terminators on AQS PREAMP’s:

The AQS PREAMP modules are delivered with external 50 Ohm terminators (SMB plug). They must be mounted as follows:

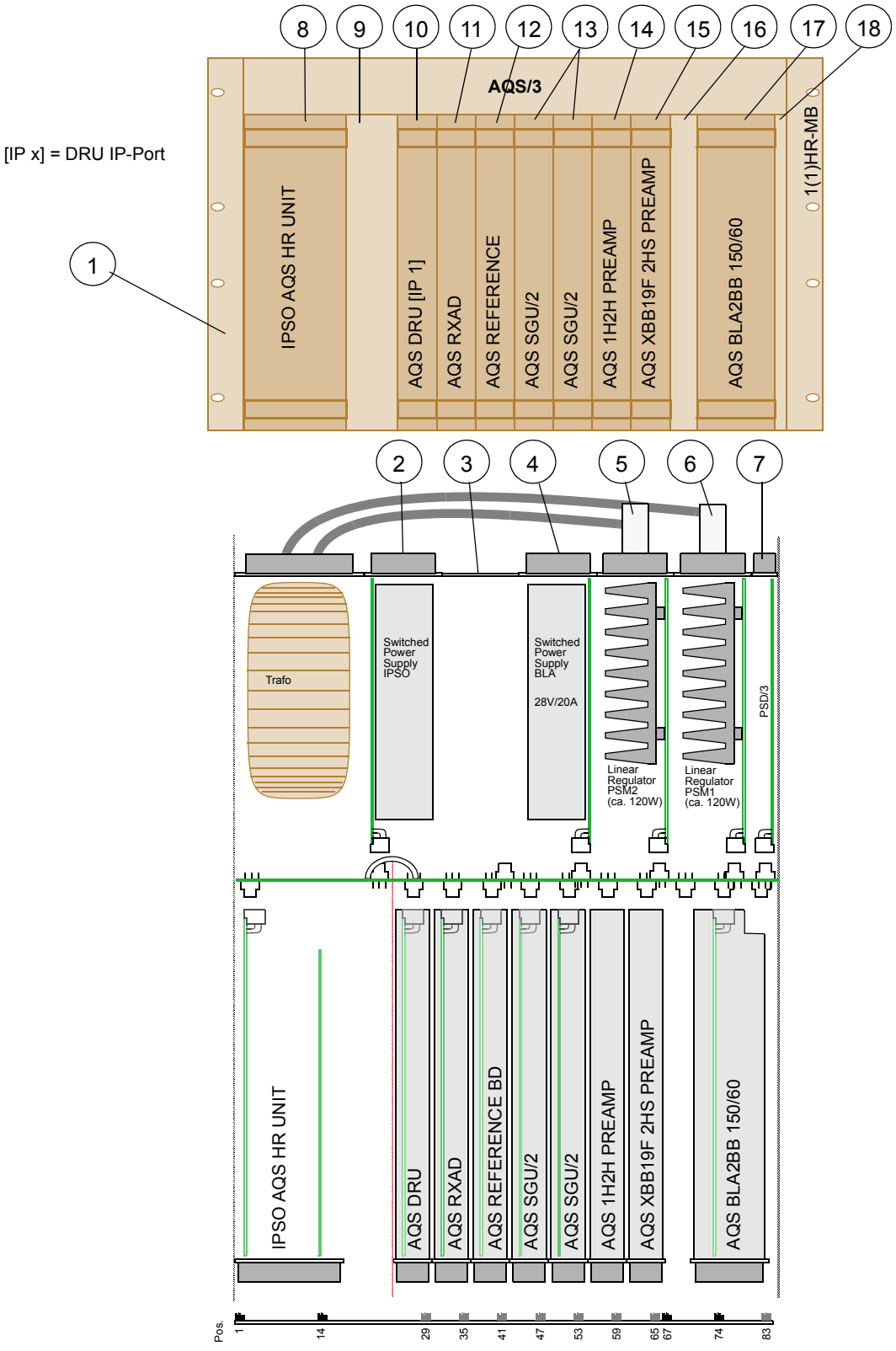
- AQS 1H2H Preamp: LOCK IN
- AQS XBB19F 2HS PREAMP: RF IN and TUNE OUT

Preamp Controller:

The preamplifier controller is integrated in the DRU. A separate AQS PREAMP CONTROL board is not needed.

Board location ***3.3.4***

Figure 3.2. AQS/3 for 2 Channel AVANCE with internal PREAMP and BLA



A typical 2 to 3 Channel AQS/3 HR (internal IPSO, external BLA) 3.4

Bill of Material 3.4.1

Table 3.3. Bill of material

Pos.	Units	Part Number	Description *Units for 3rd channel extension, ROUTER and 2H-TX option written in italics.*	MP[a]
1	1	Z106171	AQS/3 CHASSIS WIRED ECL ≥ 02 or SIH0303	
2	1	87577	IPSO AQS POWER SUPPLY	
3	1	Z12170	BSMS FRONTPLATE BLIND 12TE	MB
4	1	Z12170 *W1345050*	BSMS FRONTPLATE BLIND 12TE *AQS POWER SUPPLY BLA 28V 20A*	MB
5	1	Z102023	AQS PSM5 POWER SUPPLY MODULE	
6	1	Z003402	AQS PSM1 POWER SUPPLY MODULE	
7	1	H14109	AQS PSD/3 BOARD	
8	1	H9984	IPSO AQS HR UNIT	
9	1	Z14118	AQS FRONTPLATE BLIND 8TE	MB
10	1	Z100977 Z102520	AQS DRU (≤ 400MHz) ECL ≥ 02 AQS DRU-E (≥ 500MHz) ECL ≥ 02	
11	1	Z102116 Z102117 Z102118 Z102119	AQS RECEIVER BOARD RXAD 400 AQS RECEIVER BOARD RXAD 600 AQS RECEIVER BOARD RXAD 1000 AQS RECEIVER BOARD RXAD-BB	
12	1	Z003265 Z003936 Z003937	AQS REFERENCE BOARD 400 AQS REFERENCE BOARD 600 AQS REFERENCE BOARD 1000	
13	2	Z103080 Z103081 Z103082	AQS SGU/2 400 AQS SGU/2 600 AQS SGU/2 1000	
14	1	Z13955 *see pos. 12* *Z12489*	AQS FRONTPLATE 1MM 18TE *AQS SGU* *AQS FRONTPLATE BLIND 6TE*	MB
15	1	Z13954	AQS COVERPLATE 18TE	MB
16	1	Z12489 *Z103550* *Z103551*	AQS FRONTPLATE BLIND 6TE *AQS 2H-TX BD 200-400* *AQS 2H-TX BD 500-1000*	MB

Table 3.3. Bill of material

Pos.	Units	Part Number	Description *Units for 3rd channel extension, ROUTER and 2H-TX option written in italics.*	MP[a]
17	1	Z12489 *Z101247*	AQS FRONTPLATE BLIND 6TE *AQS 1 TO 4 ROUTER*	MB
- [b]	16	25958	SCREW RRCH KR M2,5 x 12,3	MB

a MEC Part: MB = Part contained in AQS/3 MEC-PARTS MB (Z106936)

b use for pos. 3, 4, 9, 14, 16 and 17

Rackcode Setting *3.4.2*

The rackcode must be set to ‘0x31’ (rotary switches on the AQS/3 user bus rear side: SW2 = 3, SW1 = 1).

For chassis with ECL ≤ 01 see ***"Rackcode Settings" on page 72***

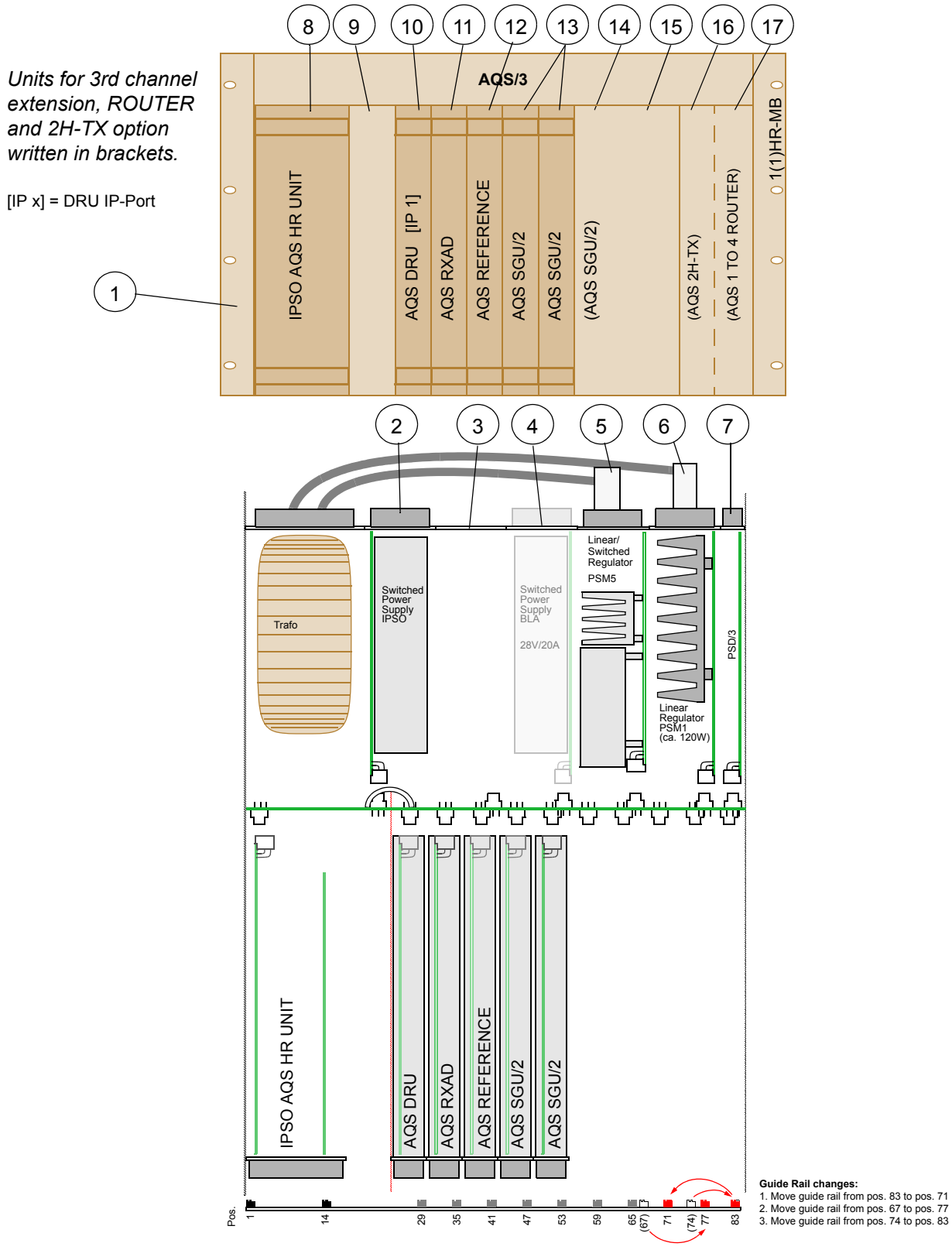
The power-up delay must be set to ‘0’ (rotary switch on chassis rear side).

Guide Rail changes *3.4.3*

To change the guide rails correctly please follow the exact order as described below.

1. Move guide rail from pos. 83 to pos. 71
2. Move guide rail from pos. 67 to pos. 77
3. Move guide rail from pos. 74 to pos. 83

Figure 3.3. AQS/3 for 2 Channel AVANCE



A typical 2 to 6 Channel AQS/3 HR & Solids (external IPSO & BLA) 3.5

Bill of Material 3.5.1

Table 3.4. Bill of material

Pos.	Units	Part Number	Description *Units for 3rd to 6th channel extension, ROUTER and 2H-TX option written in italics.*	MP[a]
1	1	Z106171	AQS/3 CHASSIS WIRED ECL ≥ 02 or SIH0303	
2	1	87577	IPSO AQS POWER SUPPLY	
3	1	Z12170	BSMS FRONTPLATE BLIND 12TE	OB
4	1	Z12170 *W1345050*	BSMS FRONTPLATE BLIND 12TE *AQS POWER SUPPLY BLA 28V 20A*	OB
5	1	Z102023	AQS PSM5 POWER SUPPLY MODULE	
6	1	Z003402	AQS PSM1 POWER SUPPLY MODULE	
7	1	H14109	AQS PSD/3 BOARD	
8	1	Z105564	AQS FRONTPLATE 1MM 24TE	OB
9	1	Z105565	AQS COVERPLATE 24TE	OB
10	1	Z100977 Z102520	AQS DRU (≤ 400MHz) ECL ≥ 02 AQS DRU-E (≥ 500MHz) ECL ≥ 02	
11	1	Z102116 Z102117 Z102118 Z102119	AQS RECEIVER BOARD RXAD 400 AQS RECEIVER BOARD RXAD 600 AQS RECEIVER BOARD RXAD 1000 AQS RECEIVER BOARD RXAD-BB	
12	1	Z003265 Z003936 Z003937 *Z104236* [b]	AQS REFERENCE BOARD 400 AQS REFERENCE BOARD 600 AQS REFERENCE BOARD 1000 *AQS REFERENCE BOARD/2 1000*	
13	2	Z103080 Z103081 Z103082	AQS SGU/2 400 AQS SGU/2 600 AQS SGU/2 1000	
14	1 1 *1-2* *1*	Z14119 Z14120 *see Pos.12* *Z12489*	AQS FRONTPLATE BLIND 1MM 12TE AQS COVERPLATE 8TE *AQS SGU* *AQS FRONTPLATE BLIND 6TE*	OB OB OB

Table 3.4. Bill of material

Pos.	Units	Part Number	Description *Units for 3rd to 6th channel extension, ROUTER and 2H-TX option written in italics.*	MP[a]
15	1 1 *1-2* *1* *1*	Z14119 Z14120 *see Pos.12* *Z12489* *Z103550* *Z103551*	AQS FRONTPLATE BLIND 1MM 12TE AQS COVERPLATE 8TE *AQS SGU* *AQS FRONTPLATE BLIND 6TE* *AQS 2H-TX BD 200-400* *AQS 2H-TX BD 500-1000*	OB OB OB
16	1	Z12489 *Z101247*	AQS FRONTPLATE BLIND 6TE *AQS 1 TO 4 ROUTER*	OB
17	*2*	*Z102000* [b]	*AQS BB SPLITTER 2-WAY*	
18	*2*	*45999* [b]	*ATTENUATOR SMA-SMA 6DB*	
- [c]	18	25958	SCREW RRCH KR M2,5 x 12,3	OB

a MEC Part: OB = Part contained in AQS/3 MEC-PARTS OB (Z106937)

b for 5-6 channel only, see also ***"Reference Board/2 1000" on page 38***

c used for pos. 3, 4, 8, 14, 15 and 16

Rackcode Setting *3.5.2*

The rackcode must be set to ‘0x31’ (rotary switches on the AQS/3 user bus rear side: SW2 = 3, SW1 = 1).

For chassis with ECL ≤ 01 see ***"Rackcode Settings" on page 72***

The power-up delay must be set to ‘0’ (rotary switch on chassis rear side).

Guide Rail changes *3.5.3*

To change the guide rails correctly please follow the exact order as described below.

1. Move guide rail from pos. 83 to pos. 71
2. Move guide rail from pos. 67 to pos. 77
3. Move guide rail from pos. 74 to pos. 83

The REFERENCE BOARD 400..1000 can only support 4 SGU with the necessary reference frequencies. For more than 4 SGU in one chassis a REFERENCE BOARD/2 1000 must be used.

The REFERENCE BOARD/2 has 2 standard and 2 boosted REF outputs.

- Standard Outputs: REF 1 (J6) and REF 2 (J7)
- Boosted Outputs: REF 3+4 (J8) and REF 5+6 (J9)

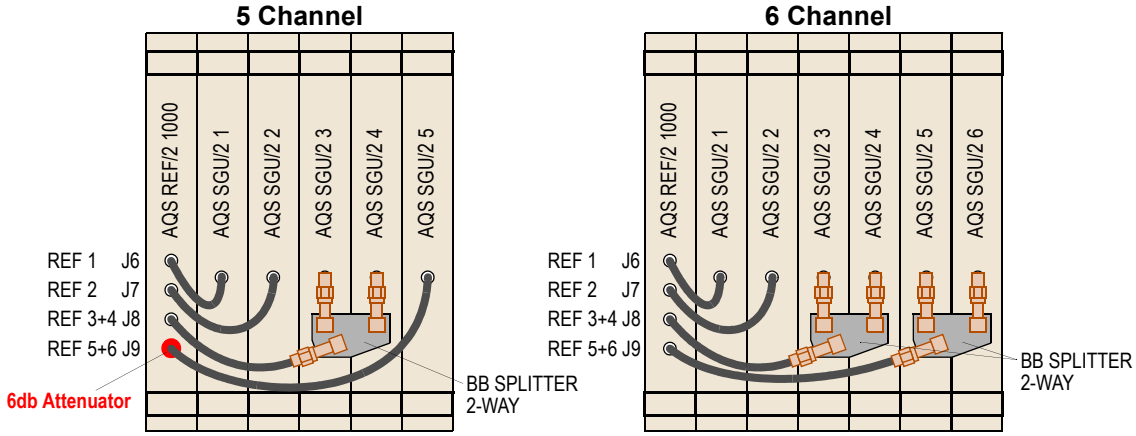
5 Channel Configuration:

The standard outputs REF1 and REF2 supply the first two SGU. SGU3 and SGU4 are connected to output REF3+4 with the AQS BB SPLITTER 2-WAY. SGU5 is connected to output REF5+6 with a 6dB attenuator.

6 Channel Configuration:

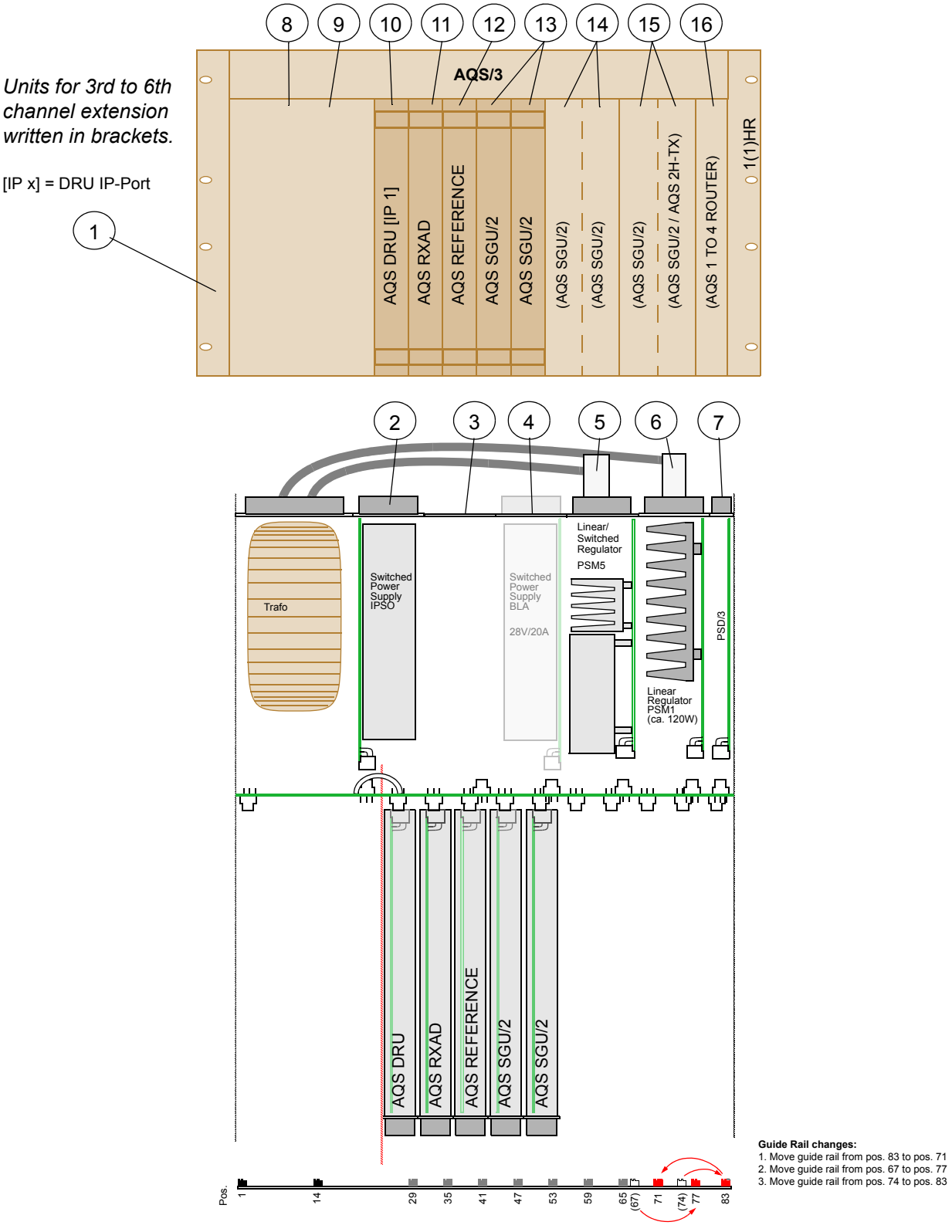
The standard outputs REF1 and REF2 supply the first two SGU. SGU3 and SGU4 are connected to output REF3+4 with the first AQS BB SPLITTER 2-WAY. SGU5 and SGU6 are connected to output REF5+6 with the second AQS BB SPLITTER 2-WAY.

Figure 3.4. REF/2 1000 & BB Splitter Connection



Board location 3.5.5

Figure 3.5. AQS/3 for 2 to 6 Channel AVANCE



A typical 2 to 4 Channel AQS/3 HR with 2 RX (external IPSO & BLA) 3.6

Bill of Material 3.6.1

Table 3.5. Bill of Material

Pos.	Units	Part Number	Description	MP[a]
1	1	Z106171	AQS/3 CHASSIS WIRED ECL ≥ 02 or SIH0303	
2	1	87577	IPSO AQS POWER SUPPLY	
3	2	Z12170	BSMS FRONTPLATE BLIND 12TE	OB
4	1	Z102023	AQS PSM5 POWER SUPPLY MODULE	
5	1	Z003402	AQS PSM1 POWER SUPPLY MODULE	
6	1	H14109	AQS PSD/3 BOARD	
7	1	Z105564	AQS FRONTPLATE 1MM 24TE	OB
8	1	Z105565	AQS COVERPLATE 24TE	OB
9	2	Z100977 Z102520	AQS DRU (≤ 400MHz) ECL ≥ 02 AQS DRU-E (≥ 500MHz) ECL ≥ 02	
10	2	Z102116 Z102117 Z102118 Z102119	AQS RECEIVER BOARD RXAD 400 AQS RECEIVER BOARD RXAD 600 AQS RECEIVER BOARD RXAD 1000 AQS RECEIVER BOARD RXAD-BB	
11	1	Z003265 Z003936 Z003937	AQS REFERENCE BOARD 400 AQS REFERENCE BOARD 600 AQS REFERENCE BOARD 1000	
12	2	Z103080 Z103081 Z103082	AQS SGU/2 400 AQS SGU/2 600 AQS SGU/2 1000	
13	1 *1-2* *1*	Z14119 *see Pos.12* *Z12489*	AQS FRONTPLATE BLIND 1MM 12TE *AQS SGU* *AQS FRONTPLATE BLIND 6TE*	OB OB
14	1	Z12489	AQS FRONTPLATE BLIND 6TE	OB
15	2	20910	HYBRID SPLITTER ZFSC-2-4	
- [b]	16	25958	SCREW RRCH KR M2,5 x 12,3	OB

a MEC Part: OB = Part contained in AQS/3 MEC-PARTS OB (Z106937)

b used for pos. 3, 7, 13 and 14

Rackcode Setting *3.6.2*

The rackcode must be set to ‘0x01’ (rotary switches on the AQS/3 user bus rear side: SW2 = 0, SW1 = 1).

For chassis with ECL ≤ 01 see ***"Rackcode Settings" on page 72***

The power-up delay must be set to ‘0’ (rotary switch on chassis rear side).

! ***Pulse Switch Setting:***

Pulse switch 1 must be opened via AQS controller for multi receive!

Guide Rail changes *3.6.3*

To change the guide rails correctly please follow the exact order as described below.

1. Move guide rail from pos. 83 to pos. 71
2. Move guide rail from pos. 67 to pos. 77
3. Move guide rail from pos. 74 to pos. 83

LO2 Splitter and AUX Combiner *3.6.4*

In a two-receiver system the LO2 signal from the reference board (J5) has to be split for the two receivers by use of a ZFSC-2-4 power splitter. The two outputs of the splitter are connected to the LO2_IN input (J3) of each receiver.

In order to allow the first two SGU/2 to the generate the tune signal, the AUX outputs of SGU/2 1 and SGU/2 2 (J7) are combined with a second ZFSC-2-4. The combined output is connected to the TUNING_IN connector of the HPPR cover module.

Figure 3.6. LO2 Splitter and AUX Combiner

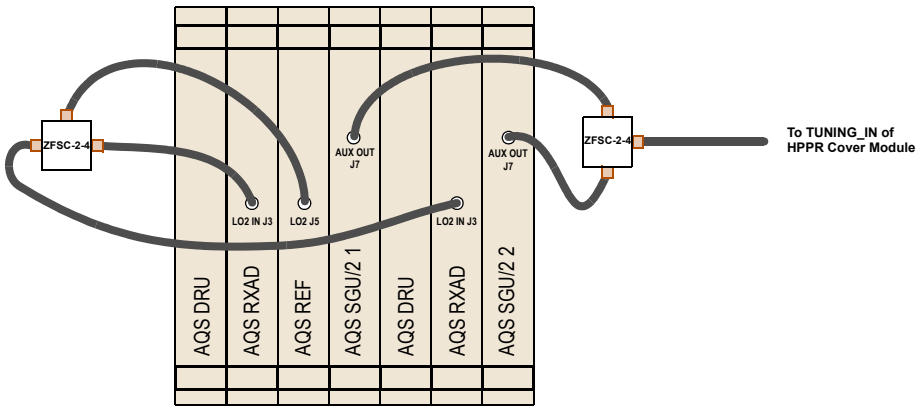
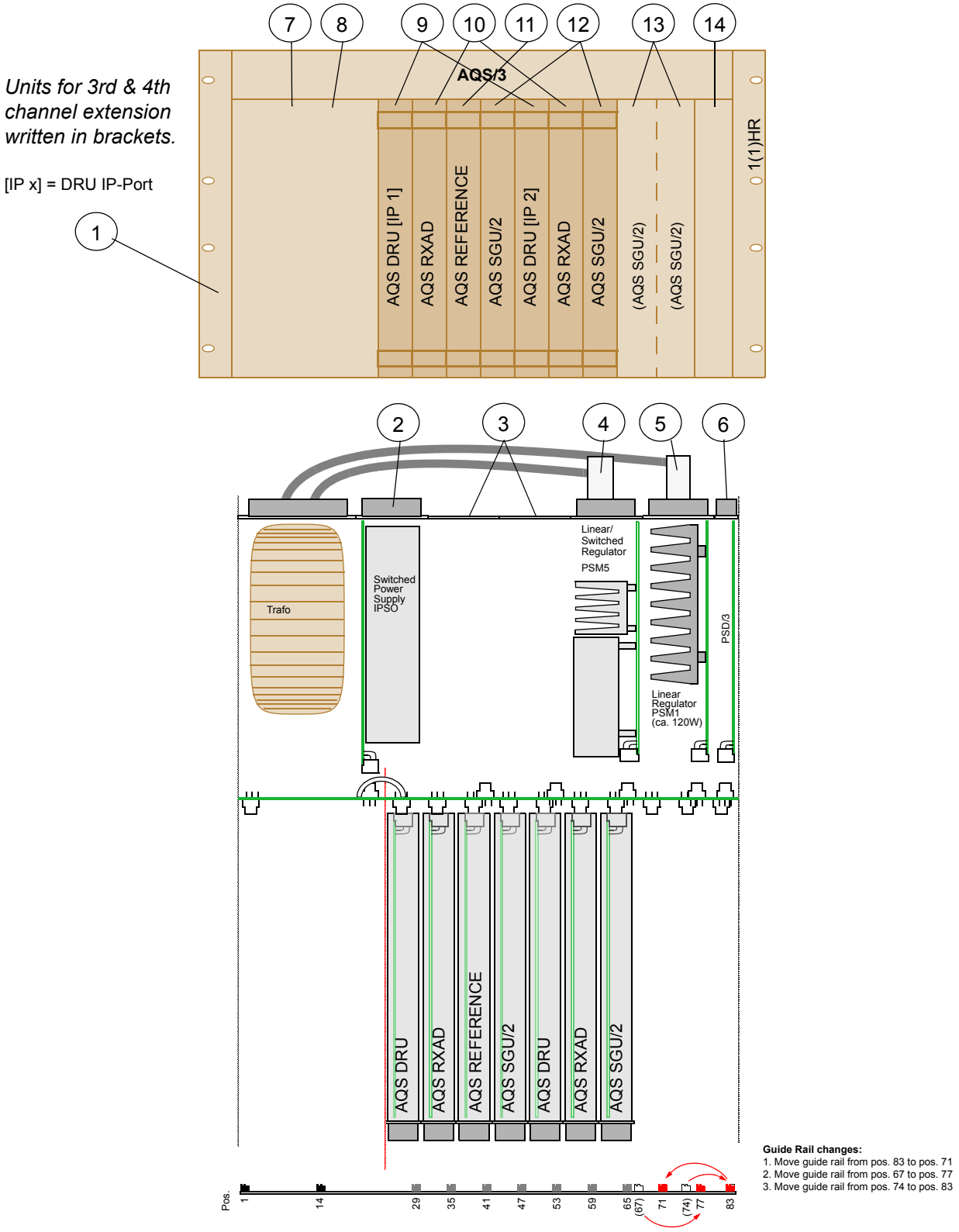


Figure 3.7. AQS/3 for 2 to 4 TX & 2 RX AVANCE



A typical 1 Channel AQS/3 PharmaScan with 1 RX 3.7

Bill of Material 3.7.1

Table 3.6. Bill of material

Pos.	Units	Part Number	Description	MP[a]
1	1	Z106171	AQS/3 CHASSIS WIRED ECL ≥ 02 or SIH0303	
2	1	87577	IPSO AQS POWER SUPPLY	
3	2	Z12170	BSMS FRONTPLATE BLIND 12TE	OB
4	1	Z102023	AQS PSM5 POWER SUPPLY MODULE	
5	1	Z003402	AQS PSM1 POWER SUPPLY MODULE	
6	1	H14109	AQS PSD/3 BOARD	
7	1	Z105564	AQS FRONTPLATE 1MM 24TE	OB
8	1	Z105565	AQS COVERPLATE 24TE	OB
9	1	Z102520	AQS DRU -E	
10	1	Z102116 Z102117	AQS RECEIVER BOARD RXAD 400 ECL ≥ 04[b] AQS RECEIVER BOARD RXAD 600 ECL ≥ 04[b]	
11	1	Z003265 Z003936	AQS REFERENCE BOARD 400 AQS REFERENCE BOARD 600	
12	1	Z103080 Z103081	AQS SGU/2 400 AQS SGU/2 600	
13	1	T10838	MRI AQS TUNE SIGNAL SPLITTER UNIT	
14	1	Z12489	AQR FRONTPLATE BLIND 6TE	OB
15	2	Z14119	AQS FRONTPLATE 1MM 12TE	OB
16	2	Z14120	AQS COVERPLATE 8TE	OB
- [c]	16	25958	SCREW RRCH KR M2,5 x 12,3	OB

a MEC Part: MRI = Part contained in AQS/3 MEC-PARTS OB (Z106937)
b ECL 02 or ECL 03 need additional MRI ARRAY-PREAMP SUPPLY 10V (Z110658)
c used for pos. 3, 7, 14 and 15

Rackcode Setting *3.7.2*

The rackcode must be set to ‘0x01’ (rotary switches on the AQS/3 user bus rear side: SW2 = 0, SW1 = 1).

For chassis with ECL ≤ 01 see ***"Rackcode Settings" on page 72***

The power-up delay must be set to ‘0’ (rotary switch on chassis rear side).

! ***Pulse Switch Setting:***

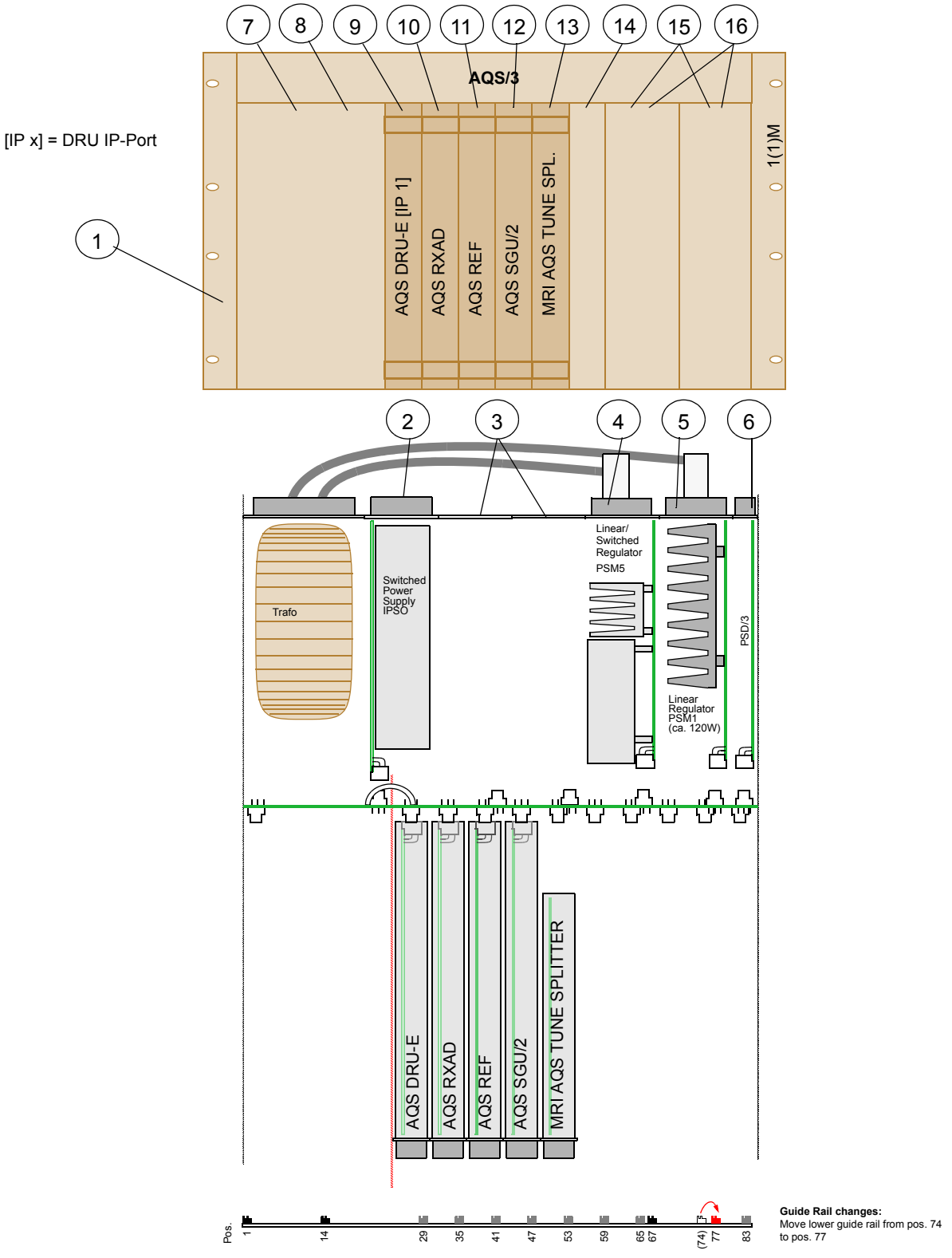
Both pulse switches must be closed via AQS controller.

Guide Rail changes *3.7.3*

To be able to mount the coverplate (pos. 16) in slot 9 & 10 properly, move the lower guide rail from pos. 74 to pos. 77

Board location *3.7.4*

Figure 3.8. AQS/3 for 1 Channel (TX & RX) PharmaScan AVANCE



A typical AQS/3 BioSpec (2-4TX/1RX) 3.8

Bill of Material 3.8.1

Table 3.7. Bill of material

Pos.	Units	Part Number	Description *Units for 3-4 TX channel extension written in italics.*	MP[a]
1	1	Z106171	AQS/3 CHASSIS WIRED ECL ≥ 02 or SIH0303	
2	1	87577	IPSO AQS POWER SUPPLY	
3	1	Z107413	AQS PSM ADM	
4	1	Z104783	AQS PSM HPLNA	
5	1	Z102023	AQS PSM5 POWER SUPPLY MODULE	
6	1	Z003402	AQS PSM1 POWER SUPPLY MODULE	
7	1	H14109	AQS PSD/3 BOARD	
8	1	Z105564	AQS FRONTPLATE 1MM 24TE	OB
9	1	Z105565	AQS COVERPLATE 24TE	OB
10	1	Z102520	AQS DRU -E	
11	1	Z102116 Z102117 Z102118	AQS RECEIVER BOARD RXAD 400 ECL ≥ 04[b] AQS RECEIVER BOARD RXAD 600 ECL ≥ 04[b] AQS RECEIVER BOARD RXAD 1000 ECL ≥ 04[b]	
12	1	Z003265 Z003936 Z003937	AQS REFERENCE BOARD 400 AQS REFERENCE BOARD 600 AQS REFERENCE BOARD 1000	
13	2	Z103080 Z103081 Z103082	AQS SGU/2 400 AQS SGU/2 600 AQS SGU/2 1000	
14	1 *1*	Z12489 *see Pos.13*	AQR FRONTPLATE BLIND 6TE *AQS SGU*	OB
15	2 *1* *1*	Z14119 *see Pos.13* *Z12489*	AQS FRONTPLATE BLIND 1MM 12TE *AQS SGU* *AQS FRONTPLATE BLIND 6TE*	OB OB
16	2	Z14120	AQS COVERPLATE 8TE	OB
- [c]	8	25958	SCREW RRCH KR M2,5 x 12,3	OB

a MEC Part: MRI = Part contained in AQS/3 MEC-PARTS OB (Z106937)

b ECL 02 or ECL 03 need additional MRI ARRAY-PREAMP SUPPLY 10V (Z110658)

c used for pos. 3, 8, 14 and 15

Rackcode Setting *3.8.2*

The rackcode must be set to ‘0x01’ (rotary switches on the AQS/3 user bus rear side: SW2 = 0, SW1 = 1).

For chassis with ECL ≤ 01 see ***"Rackcode Settings" on page 72***

The power-up delay must be set to ‘0’ (rotary switch on chassis rear side).

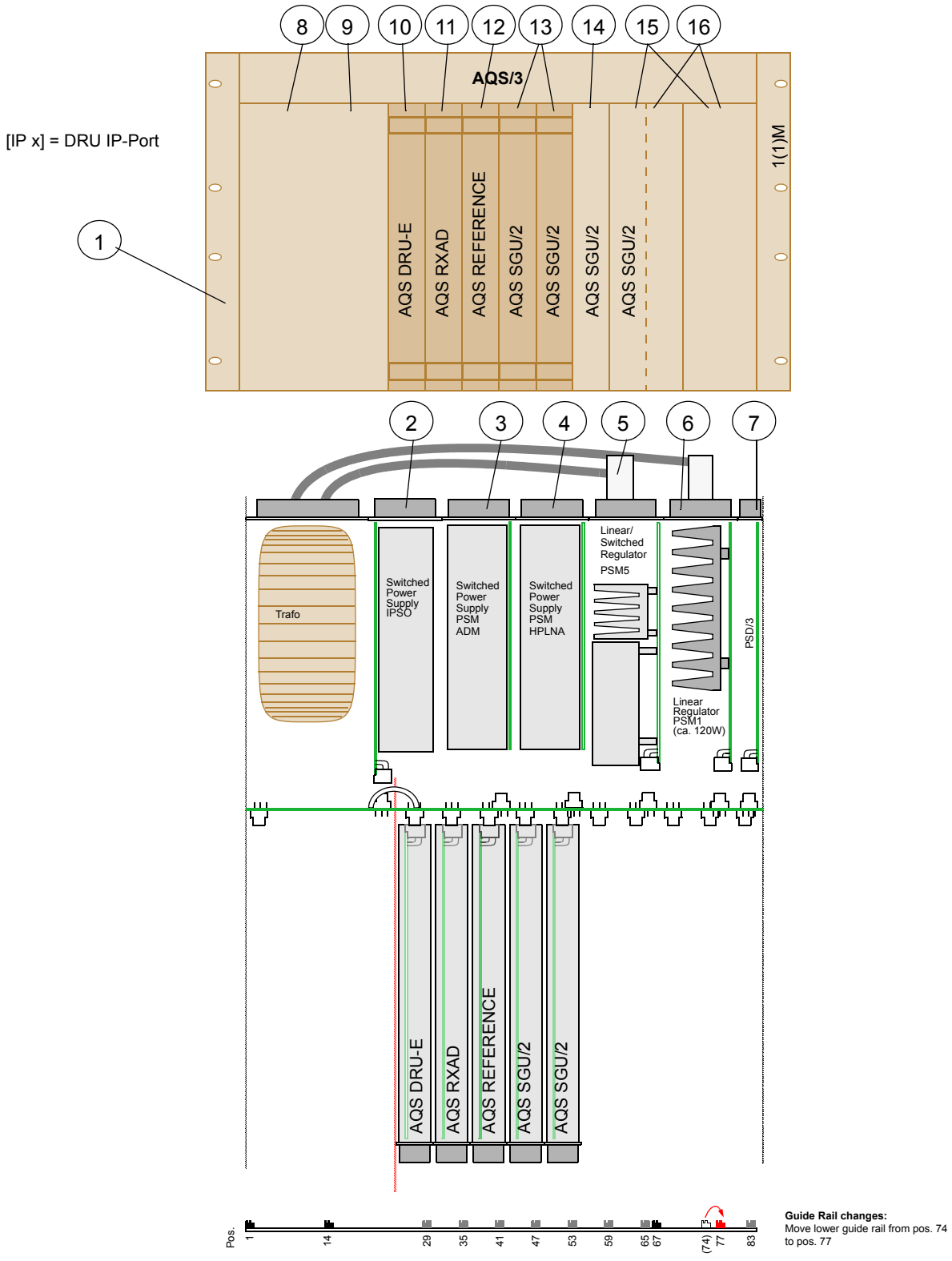
! ***Pulse Switch Setting:***

Both pulse switches must be closed via AQS controller.

Guide Rail changes *3.8.3*

To be able to mount the coverplate (pos. 16) in slot 9 & 10 properly, move the lower guide rail from pos. 74 to pos. 77

Figure 3.9. AQS/3 for 2 Channel (2-4TX/1RX) BioSpec AVANCE



A typical 4 to 8 RX Channel AQS/3 BioSpec (2-4TX/4-8RX) 3.9

Bill of Material 3.9.1

Table 3.8. Bill of material: Rack 1

Pos.	Units	Part Number	Description *Units for 3-4 TX channel extension written in italics.*	MP[a]
1	1	Z106171	AQS/3 CHASSIS WIRED ECL ≥ 02 or SIH0303	
2	1	87577	IPSO AQS POWER SUPPLY	
3	1	Z107413	AQS PSM ADM	
4	1	Z104783	AQS PSM HPLNA	
5	1	Z102023	AQS PSM5 POWER SUPPLY MODULE	
6	1	Z003402	AQS PSM1 POWER SUPPLY MODULE	
7	1	H14109	AQS PSD/3 BOARD	
8	1	Z105564	AQS FRONTPLATE 1MM 24TE	OB
9	1	Z105565	AQS COVERPLATE 24TE	OB
10	2	Z102520	AQS DRU -E	
11	2	Z102116 Z102117 Z102118	AQS RECEIVER BOARD RXAD 400 ECL ≥ 04[b] AQS RECEIVER BOARD RXAD 600 ECL ≥ 04[b] AQS RECEIVER BOARD RXAD 1000 ECL ≥ 04[b]	
12	1	Z003265 Z003936 Z003937	AQS REFERENCE BOARD 400 AQS REFERENCE BOARD 600 AQS REFERENCE BOARD 1000	
13	2	Z103080 Z103081 Z103082	AQS SGU/2 400 AQS SGU/2 600 AQS SGU/2 1000	
14	*2* *1-2*	Z12489 *see Pos.13*	AQR FRONTPLATE BLIND 6TE *AQS SGU*	OB
15	1	Z104431	AQS PULSE SPLITTER	
- [c]	6	25958	SCREW RRCH KR M2,5 x 12,3	OB

a MEC Part: OB = Part contained in AQS/3 MEC-PARTS OB (Z106937)
b ECL 02 or ECL 03 need additional MRI ARRAY-PREAMP SUPPLY 10V (Z110658)
c used for pos. 8 and 14

Table 3.9. Bill of material: Rack 2

Pos.	Units	Part Number	Description *Units for 8 RX channel extension written in italics.*	MP[a]
20	1	Z103493	AQS/2-M CHASSIS WIRED ECL ≥ 01	
21	1	H9489	AQS POWER SUPPLY DIGITAL 350W ECL ≥ 11	
22	1	Z104432	AQS RF-SPLITTER	
23	1	Z12170	BSMS FRONTPLATE BLIND 12TE	IP-M
24	1	Z102023	AQS PSM5 POWER SUPPLY MODULE	
25	1	Z003402	AQS PSM1 POWER SUPPLY MODULE	
26	1	Z2778	BSMS FRONTPLATE BLIND 4TE	IP-M
27	2 *(6)*	Z102520	AQS DRU -E	
28	2 *(6)*	Z102116 Z102117 Z102118	AQS RECEIVER BOARD RXAD 400 ECL ≥ 04[b] AQS RECEIVER BOARD RXAD 600 ECL ≥ 04[b] AQS RECEIVER BOARD RXAD 1000 ECL ≥ 04[b]	
29	5 *(1)*	Z14119	AQS FRONTPLATE 1MM 12TE	IP-M
30	5 *(1)*	Z14120	AQS COVERPLATE 8TE	IP-M
- [c]	18	25958	SCREW RRCH KR M2,5 x 12,3	IP-M

a MEC Part: IP-M = Part contained in AQS/2-M MEC-PARTS IPSO MRI (Z105994)
b ECL 02 or ECL 03 need additional MRI ARRAY-PREAMP SUPPLY 10V (Z110658)
c used for pos. 23, 26 and 29

Rackcode Setting *3.9.2*

Rack 1:

The rackcode must be set to ‘0x01’ (rotary switches on the AQS/3 user bus rear side: SW2 = 0, SW1 = 1).

For chassis with ECL ≤ 01 see ***"Rackcode Settings" on page 72***

The power-up delay must be set to ‘0’ (rotary switch on chassis rear side).

! ***Pulse Switch Setting:***

All pulse switches must be opened via AQS controller.

Rack 2:

The rack code must be set to ‘0x102’ (rotary switches SW3..1 on the AQS/2-M user bus rear side).

The power-up delay must be set to ‘1’ (rotary switch on chassis rear side).

! ***Pulse Switch Setting:***

All pulse switches must be closed via AQS controller.

Guide Rail changes *3.9.3*

Rack 1:

To change the guide rails correctly please follow the exact order as described below.

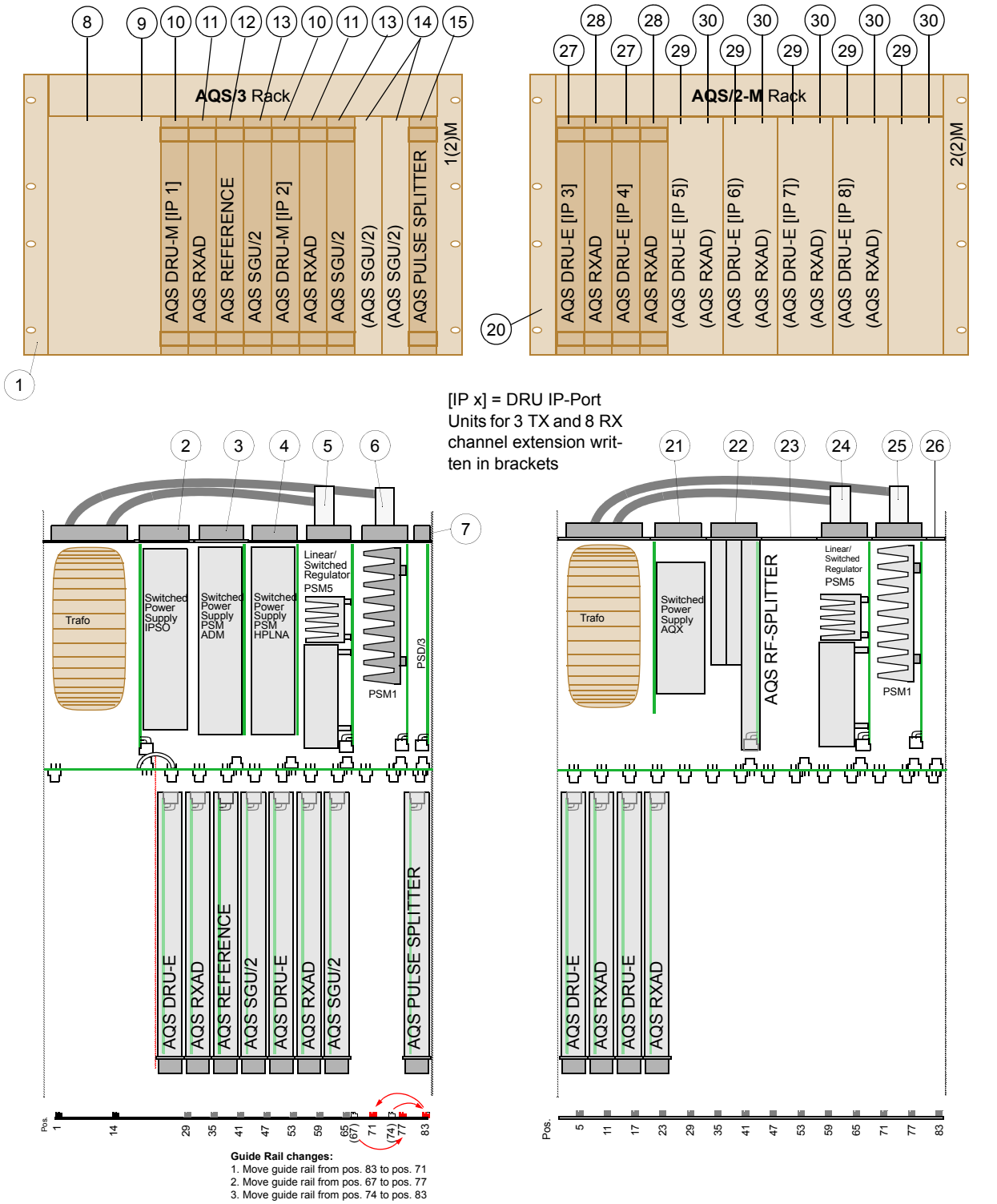
1. Move guide rail from pos. 83 to pos. 71
2. Move guide rail from pos. 67 to pos. 77
3. Move guide rail from pos. 74 to pos. 83

Rack 2:

No changes

Board location ***3.9.4***

Figure 3.10. AQS/3 for 4 to 8 RX Channel AQS BioSpec (2-4TX/4-8RX) AVANCE



A typical 16 RX Channel AQS/3 BioSpec (2-4TX/16RX) 3.10

Bill of Material 3.10.1

Table 3.10. Bill of material: Rack 1

Pos.	Units	Part Number	Description *Units for 3-4 TX channel extension written in italics.*	MP[a]
1	1	Z106171	AQS/3 CHASSIS WIRED ECL ≥ 02 or SIH0303	
2	1	87577	IPSO AQS POWER SUPPLY	
3	1	Z107413	AQS PSM ADM	
4	1	Z104783	AQS PSM HPLNA	
5	1	Z102023	AQS PSM5 POWER SUPPLY MODULE	
6	1	Z003402	AQS PSM1 POWER SUPPLY MODULE	
7	1	H14109	AQS PSD/3 BOARD	
8	1	Z105564	AQS FRONTPLATE 1MM 24TE	OB
9	1	Z105565	AQS COVERPLATE 24TE	OB
10	2	Z102520	AQS DRU -E	
11	2	Z102116 Z102117 Z102118	AQS RECEIVER BOARD RXAD 400 ECL ≥ 04[b] AQS RECEIVER BOARD RXAD 600 ECL ≥ 04[b] AQS RECEIVER BOARD RXAD 1000 ECL ≥ 04[b]	
12	1	Z003265 Z003936 Z003937	AQS REFERENCE BOARD 400 AQS REFERENCE BOARD 600 AQS REFERENCE BOARD 1000	
13	2	Z103080 Z103081 Z103082	AQS SGU/2 400 AQS SGU/2 600 AQS SGU/2 1000	
14	*2* *1-2*	Z12489 *see Pos.13*	AQR FRONTPLATE BLIND 6TE *AQS SGU*	OB
15	1	Z104431	AQS PULSE SPLITTER	
- [c]	6	25958	SCREW RRCH KR M2,5 x 12,3	OB

a MEC Part: OB = Part contained in AQS/3 MEC-PARTS OB (Z106937)
b ECL 02 or ECL 03 need additional MRI ARRAY-PREAMP SUPPLY 10V (Z110658)
c used for pos. 8 and 14

Table 3.11. Bill of material: Rack 2

Pos.	Units	Part Number	Description	MP[a]
20	1	Z103493	AQS/2-M CHASSIS WIRED ECL ≥ 01	
21	1	H9489	AQS POWER SUPPLY DIGITAL 350W ECL ≥ 11	
22	1	Z104432	AQS RF-SPLITTER	
23	1	Z12170	BSMS FRONTPLATE BLIND 12TE	IP-M
24	1	Z102023	AQS PSM5 POWER SUPPLY MODULE	
25	1	Z003402	AQS PSM1 POWER SUPPLY MODULE	
26	1	Z2778	BSMS FRONTPLATE BLIND 4TE	IP-M
27	7	Z102520	AQS DRU -E	
28	7	Z102116 Z102117 Z102118	AQS RECEIVER BOARD RXAD 400 ECL ≥ 04[b] AQS RECEIVER BOARD RXAD 600 ECL ≥ 04[b] AQS RECEIVER BOARD RXAD 1000 ECL ≥ 04[b]	
- [c]	6	25958	SCREW RRCH KR M2,5 x 12,3	IP-M

a MEC Part: IP-M = Part contained in AQS/2-M MEC-PARTS IPSO MRI (Z105994)
b ECL 02 or ECL 03 need additional MRI ARRAY-PREAMP SUPPLY 10V (Z110658)
c used for pos. 23, 26 and 29

Table 3.12. Bill of material: Rack 3

Pos.	Units	Part Number	Description	MP[a]
29	1	Z103493	AQS/2-M CHASSIS WIRED ECL ≥ 01	
30	1	H9489	AQS POWER SUPPLY DIGITAL 350W ECL ≥ 11	
31	1	Z104432	AQS RF-SPLITTER	
32	1	Z12170	BSMS FRONTPLATE BLIND 12TE	IP-M
33	1	Z102023	AQS PSM5 POWER SUPPLY MODULE	
34	1	Z003402	AQS PSM1 POWER SUPPLY MODULE	
35	1	Z2778	BSMS FRONTPLATE BLIND 4TE	IP-M
36	7	Z102520	AQS DRU -E	
37	7	Z102116 Z102117 Z102118	AQS RECEIVER BOARD RXAD 400 ECL ≥ 04[b] AQS RECEIVER BOARD RXAD 600 ECL ≥ 04[b] AQS RECEIVER BOARD RXAD 1000 ECL ≥ 04[b]	
- [c]	6	25958	SCREW RRCH KR M2,5 x 12,3	IP-M

a MEC Part: IP-M = Part contained in AQS/2-M MEC-PARTS IPSO MRI (Z105994)
b ECL 02 or ECL 03 need additional MRI ARRAY-PREAMP SUPPLY 10V (Z110658)
c used for pos. 23, 26 and 29

Rackcode Setting *3.10.2*

Rack 1:

The rackcode must be set to ‘0x01’ (rotary switches on the AQS/3 user bus rear side: SW2 = 0, SW1 = 1).

For chassis with ECL ≤ 01 see ***"Rackcode Settings" on page 72***

The power-up delay must be set to ‘0’ (rotary switch on chassis rear side).

! ***Pulse Switch Setting:***

All pulse switches must be opened via AQS controller.

Rack 2:

The rack code must be set to ‘0x102’ (rotary switches SW3..1 on the AQS/2-M user bus rear side).

The power-up delay must be set to ‘1’ (rotary switch on chassis rear side).

! ***Pulse Switch Setting:***

All pulse switches must be closed via AQS controller.

Rack 3:

The rack code must be set to ‘0x202’ (rotary switches SW3..1 on the AQS/2-M user bus rear side).

The power-up delay must be set to ‘2’ (rotary switch on chassis rear side).

! ***Pulse Switch Setting:***

All pulse switches must be closed via AQS controller.

Guide Rail changes *3.10.3*

Rack 1:

To change the guide rails correctly please follow the exact order as described below.

1. Move guide rail from pos. 83 to pos. 71
2. Move guide rail from pos. 67 to pos. 77
3. Move guide rail from pos. 74 to pos. 83

Rack 2 & 3:

No changes

Board location ***3.10.4***

Figure 3.11. AQS/3 for 16 RX Channel AQS BioSpec (2-4TX/16RX) AVANCE

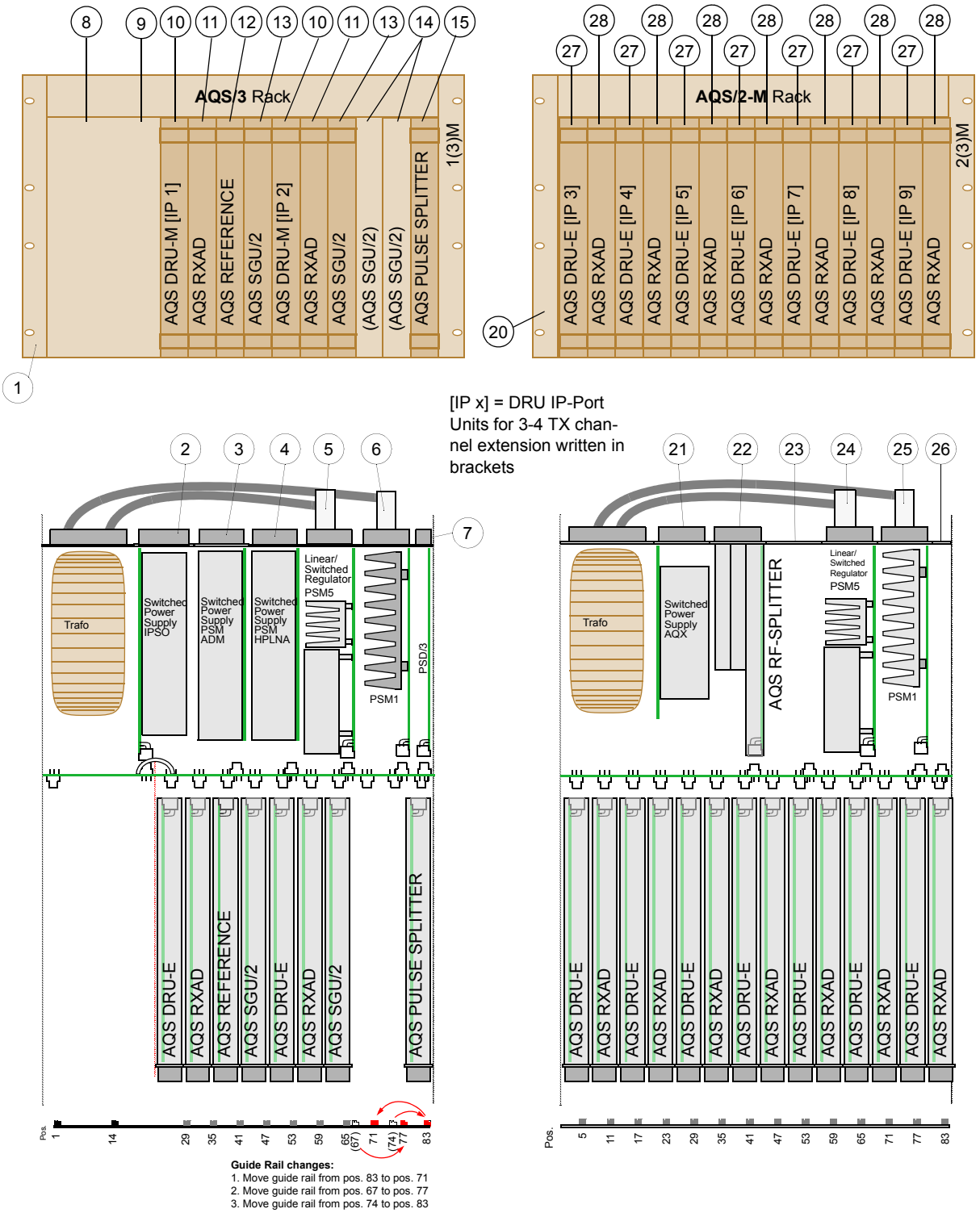
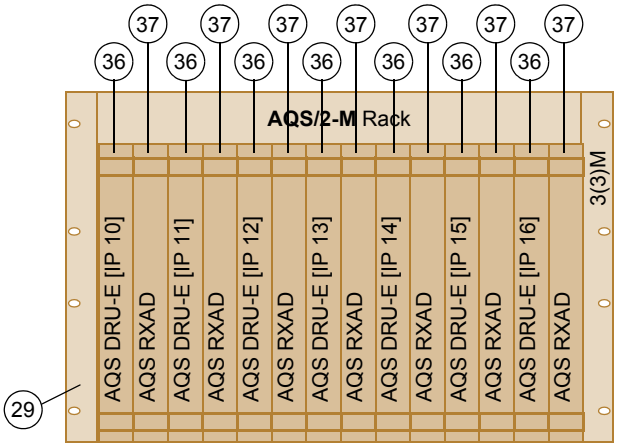
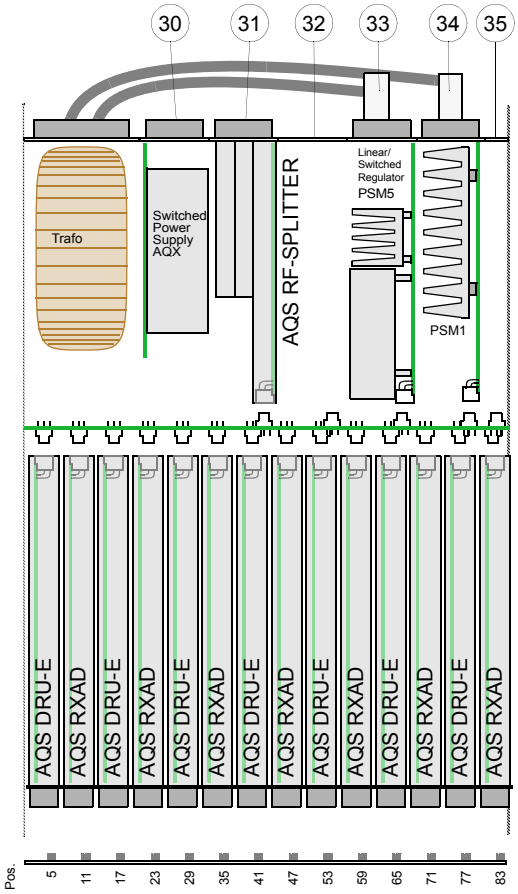


Figure 3.12. AQS/3 for 16 RX Channel AQS BioSpec (2-4TX/16RX) AVANCE



[IP x] = DRU IP-Port



AQS/3 Mainframe 4

Introduction 4.1

The AQS/3 mainframe consists of a IPSO bus part (previous AQS: VME) and a 10 slot user bus part.

The IPSO part can be equipped with the AQS IPSO unit. The user bus part is designed to be equipped with AQS RF units (e.g. SGU, Reference Board, RXAD, DRU, AQS Preamp, AQS amplifiers, 1to4 Router, Pulse Splitter).

On the rear side, linear power supply modules (PSM1, PSM2, PSM5) and switched power supply modules for the IPSO part and for the internal RF power amplifiers are placed, as well as the PSD board.

The transformer, which feeds the linear power supply modules, is part of the mainframe and is located on the rear side.

The mainframe is cooled with 8 fans, which are located in a fan tray on top of the mainframe. The fan tray is serviceable without removing the mainframe from the spectrometer cabinet. (see ***"Fan Tray Service Instructions" on page 69***)
The fan tray is the same as in the AQS/2 chassis.

Technical Data 4.2

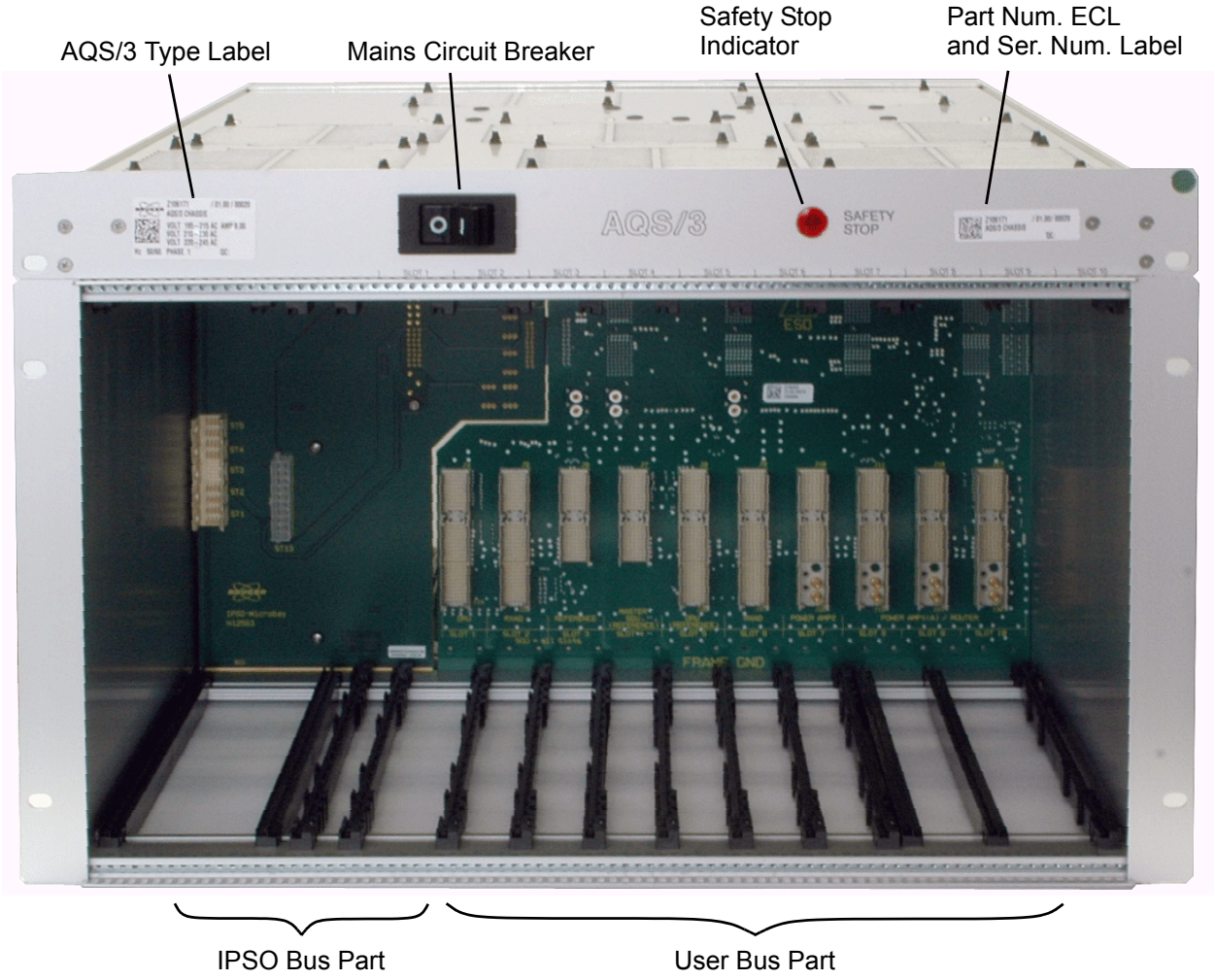
AC input voltage	208..230	V~
AC frequency range	47..63	Hz
AC input current	max. 8	A~
AC input inrush current	limited to approx. 20	Apk
AC fuse 5x20mm (2pcs. 5x20mm, time-lag T, type H)	8A~ / 250V~	
Dimensions (hight x width x depth)	310 x 483 x 570	mm
Weight (without units)	approx. 20	kg

Environmental conditions:

The AQS/3 mainframe is designed as a subunit in the electronics cabinet of the spectrometer. For the environmental conditions outside the cabinet please refer to the site planning guide of the spectrometer system.

Front View *4.3*

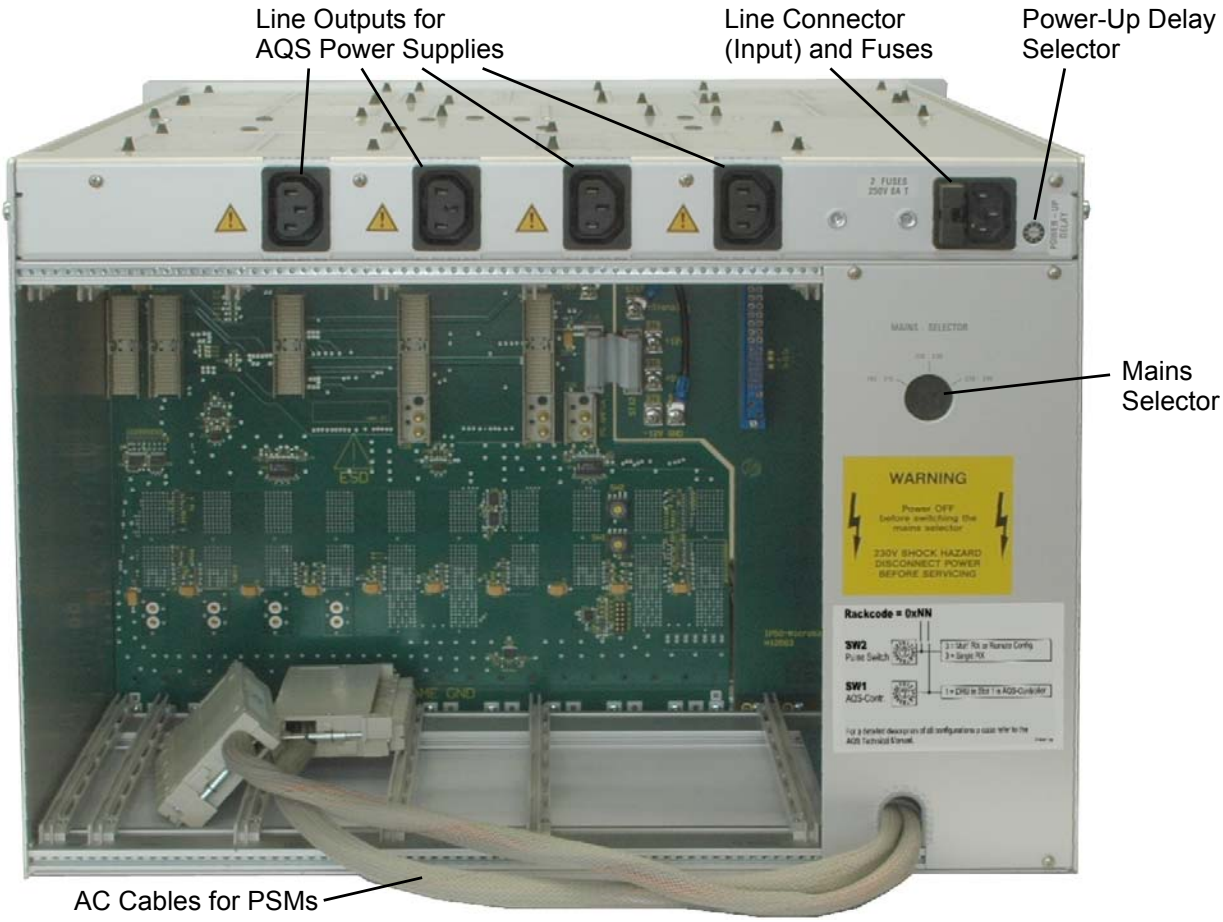
Figure 4.1. AQS/3 Chassis front view



Rear View 4.4

The rear view shows the housing of the power supply boards. On the right hand side is the transformer housing with the appropriate AC cables located.

Figure 4.2. AQS/3 Chassis rear view



Line Outputs:

Only connect AQS POWER SUPPLY units to these connectors.

- IPSO AQS POWER SUPPLY (87577)
- AQS PSM5 POWER SUPPLY MODULE (Z102023)
- POWER SUPPLY COMPACT 28V 20A (W1345050)
- AQS PSM HPLNA (Z104783)
- AQS PSM ADM (Z107413)

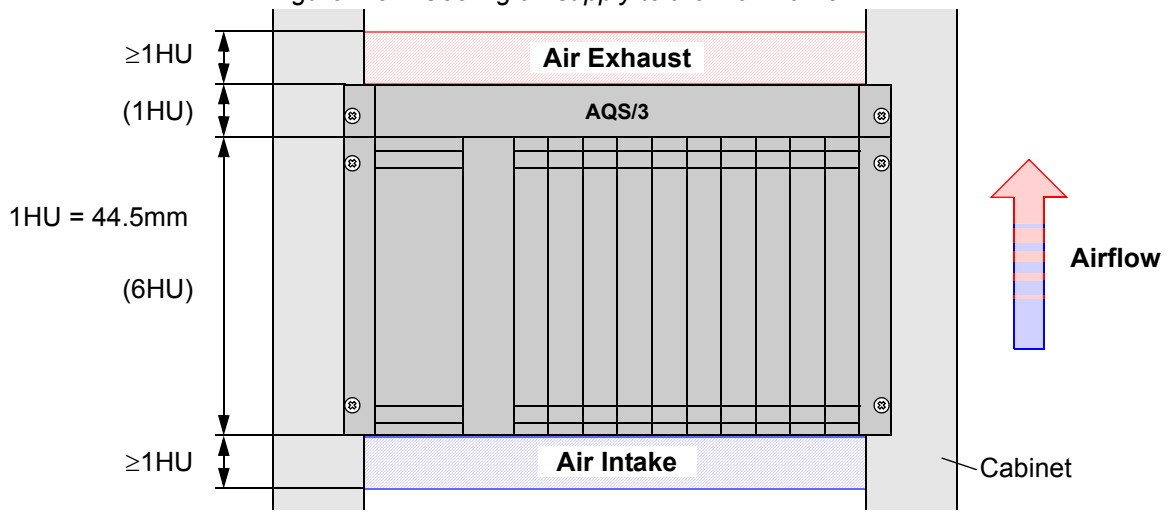
Installation in electronics cabinet 4.5

The AQS/3 mainframe must be installed at it's designated position in the electronics cabinet to ensure proper air ventilation for the cooling fans. The position may vary in different cabinet types and sizes.

! ***At least one height unit (1HU) above and below the mainframe must be reserved for the cooling air supply.***

Special air baffle plates may be used to support efficient ventilation. Typically the air intake is from the front and the exhaust towards the back of the cabinet.

Figure 4.3. Cooling air supply to the mainframe



The mainframe must be fixed by at least 4 screws into the cabinet. The power cable is included in the cabinet wiring.

Preparation for Use 4.6

Prior to the first power-up of the AQS/3 mainframe, it must be ensured that the mains selection switch is in the correct position. (see selector on the back side of the AQS/3)

The size of the linear power supply modules is designed for minimal power dissipation; therefore the transformer input voltage should be matched to the mains voltage at the installation site.

Generally, the mains selection switch should be set to the corresponding voltage range, even if the mains power is weak (max. fluctuations ± 6%).

- Factory setting for 230V~ mains supply = 220-245V~

Selector Setting for combined Voltages 4.6.1

In countries with 110-120V~ mains supply such as USA and Canada combined line voltages may be used. In this case set the selector switch to 195-215V~.

AC Power Line Fuses 4.7

The AQS/3 is protected by two fuses as specified on the power supply nameplate. The fuses are located in a removable fuse holder next to the AC power connector. Always use time-lag T fuse types with high breaking capacity H.

Power-Up Delay 4.8

The power-up delay can be selected with a rotary switch next to the power connector at the back of the mainframe. Please set the switch according to your configuration as described in the configurations section within this manual. The minimal power-up delay is 0.5s due to the inrush current limiter circuit.

Table 4.1. Power-Up Delay

Setting	Delay
0	0.5 s
1	2 s
2	4 s
3	6 s

Setting	Delay
4	8 s
5	10 s
6	12 s

Setting	Delay
7	14 s
8	16 s
9	18 s

Inrush Current Limiter 4.9

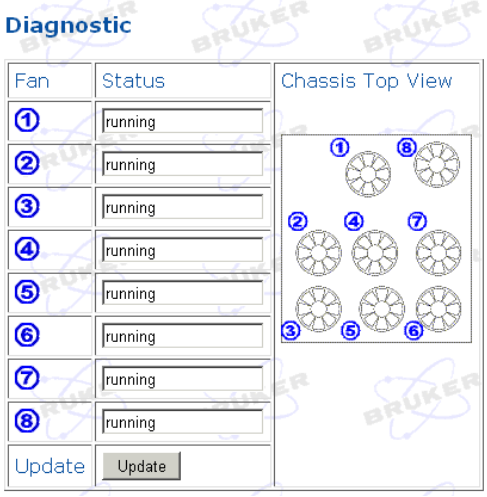
The mainframe is equipped with an inrush current limiter which limits the peak current to approx. 20A. The limiter is always active, even after a „hot start“ when the chassis is switched OFF / ON within a short timespan.

AC Power Loss 4.10

In the event of an AC power loss in the spectrometer cabinet, the chassis turns itself of and restarts automatically when the power is restored. To prevent a short time power loss an external UPS (uninterruptible power supply) must be used.

The operation of all fans is individually controlled by the AQS controller and the control circuit on the AQS/3 user bus. The fan status can be checked via the AQS chassis page in the DRU service web.

Figure 4.4. DRU Service Web: AQS Chassis Diagnostic



Safety Stop *4.12*

If the temperature inside the mainframe exceeds the absolute maximum limit of save operation, the mains supply to the chassis is switched off automatically (and without warning) to prevent permanent damage to the AQS units. This „Safety Stop“ condition is indicated with a red lamp on the front panel as long as the mains supply is present at the power connector.

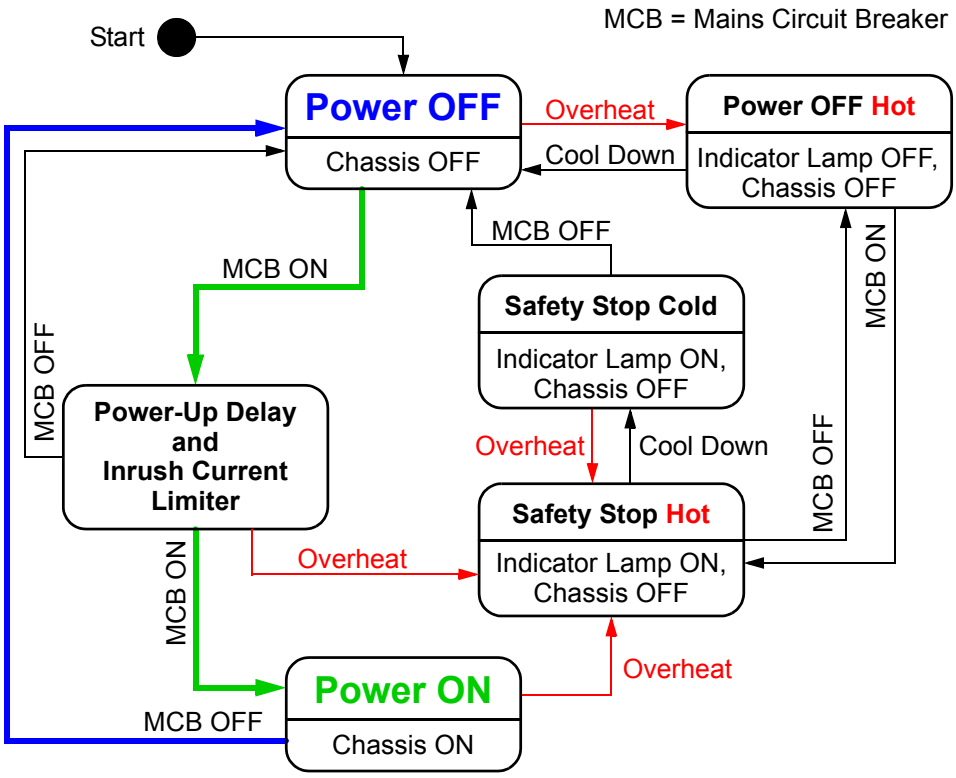
! ***Make sure to establish and remove the cause of the Safety Stop condition before you use the spectrometer again.***

The Safety Stop can be caused by a fan or power supply failure within the mainframe. Other causes can be inefficient cooling air supply to the mainframe or exceeding ambient air temperatures within or around the spectrometer cabinet.

Please contact Bruker service personnel if you cannot establish the cause of the failure.

The chassis can be returned to its normal working state by switching the mains circuit breaker manually OFF and ON. An AC power loss also resets the chassis to its working state (see ***"AC Power Loss"***).

Figure 4.5. Safety Stop State Diagram



AC Wiring 4.13

Figure 4.6. AQS/3 AC Wiring

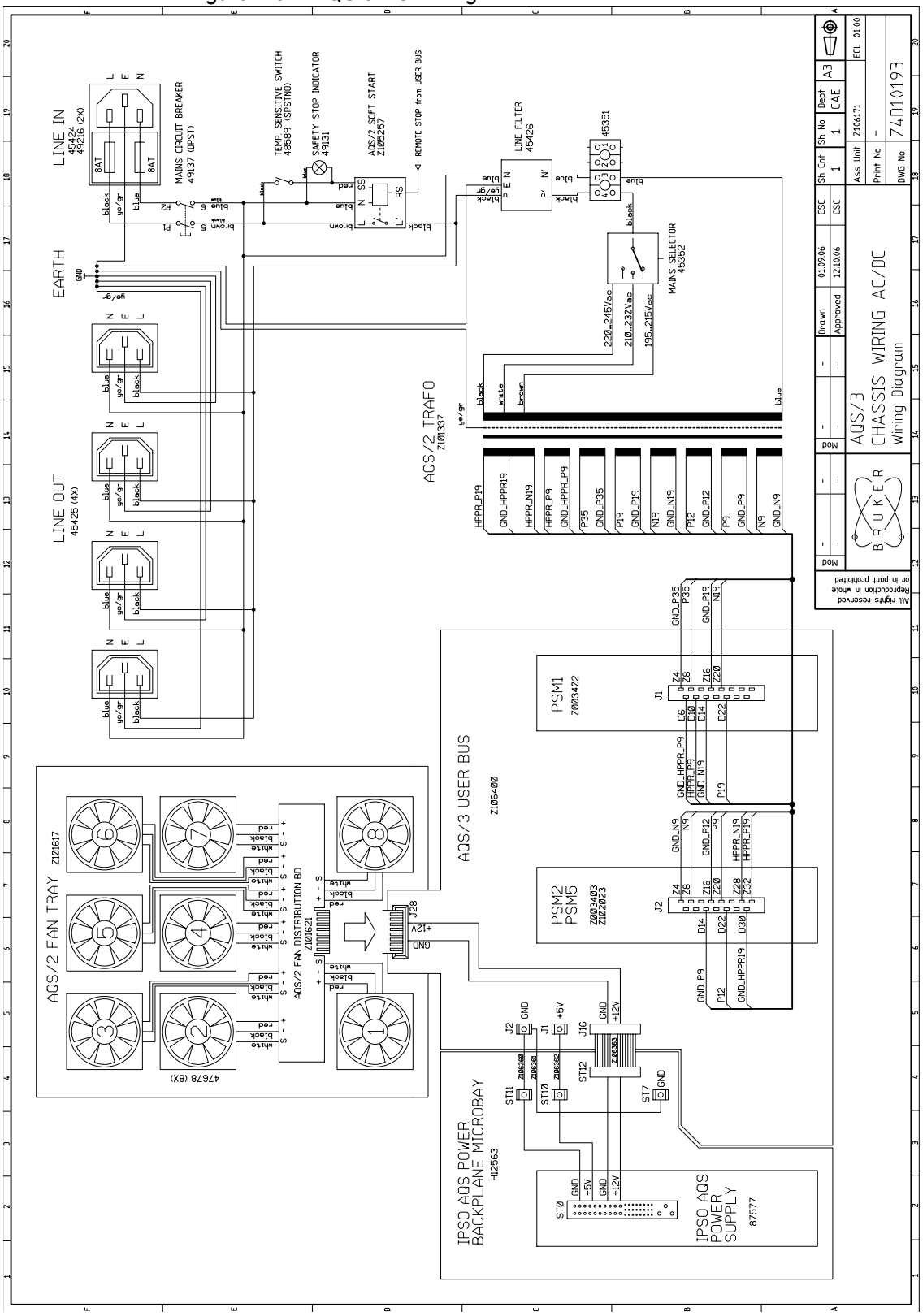
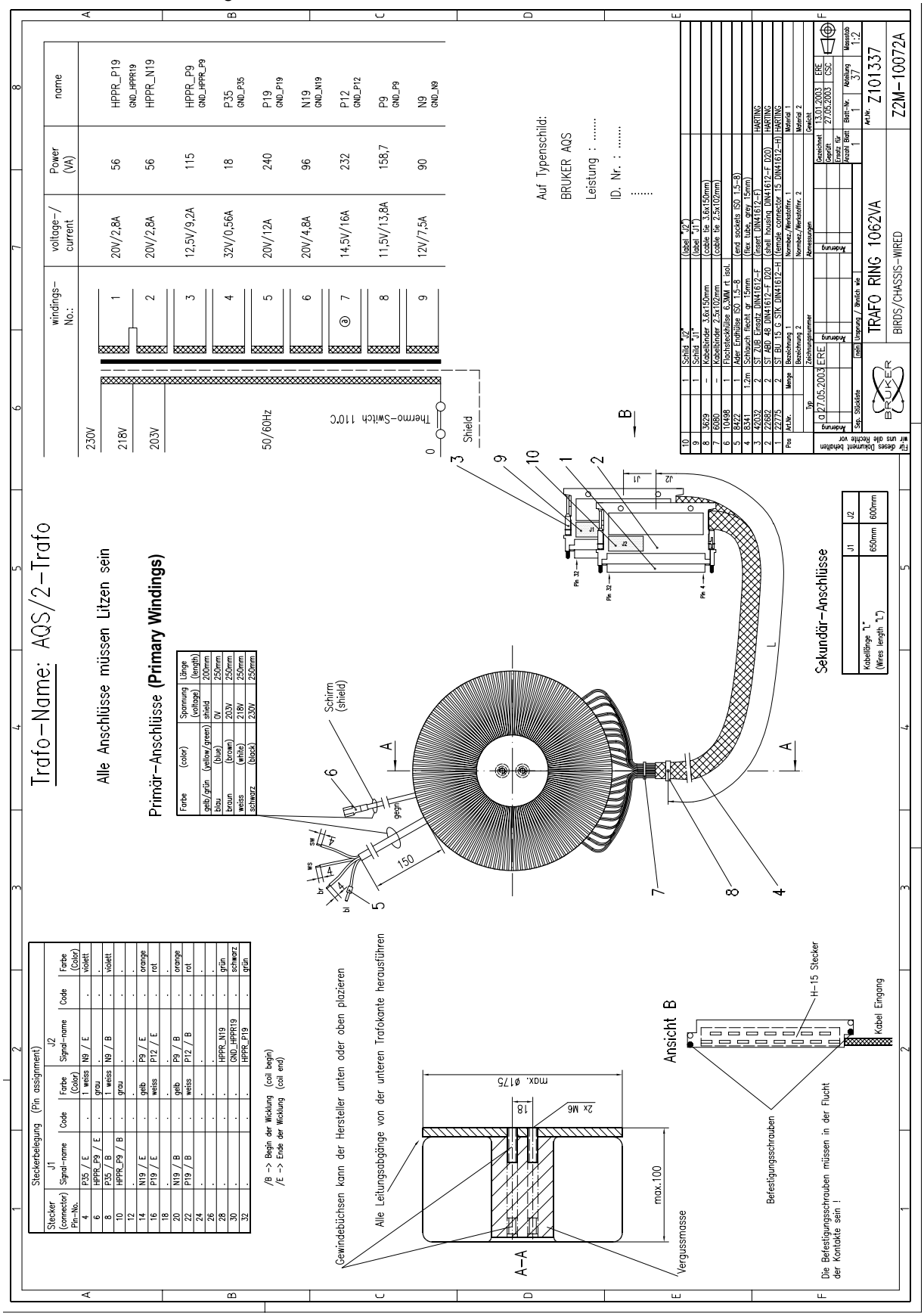


Figure 4.7. AQS/2 Transformer



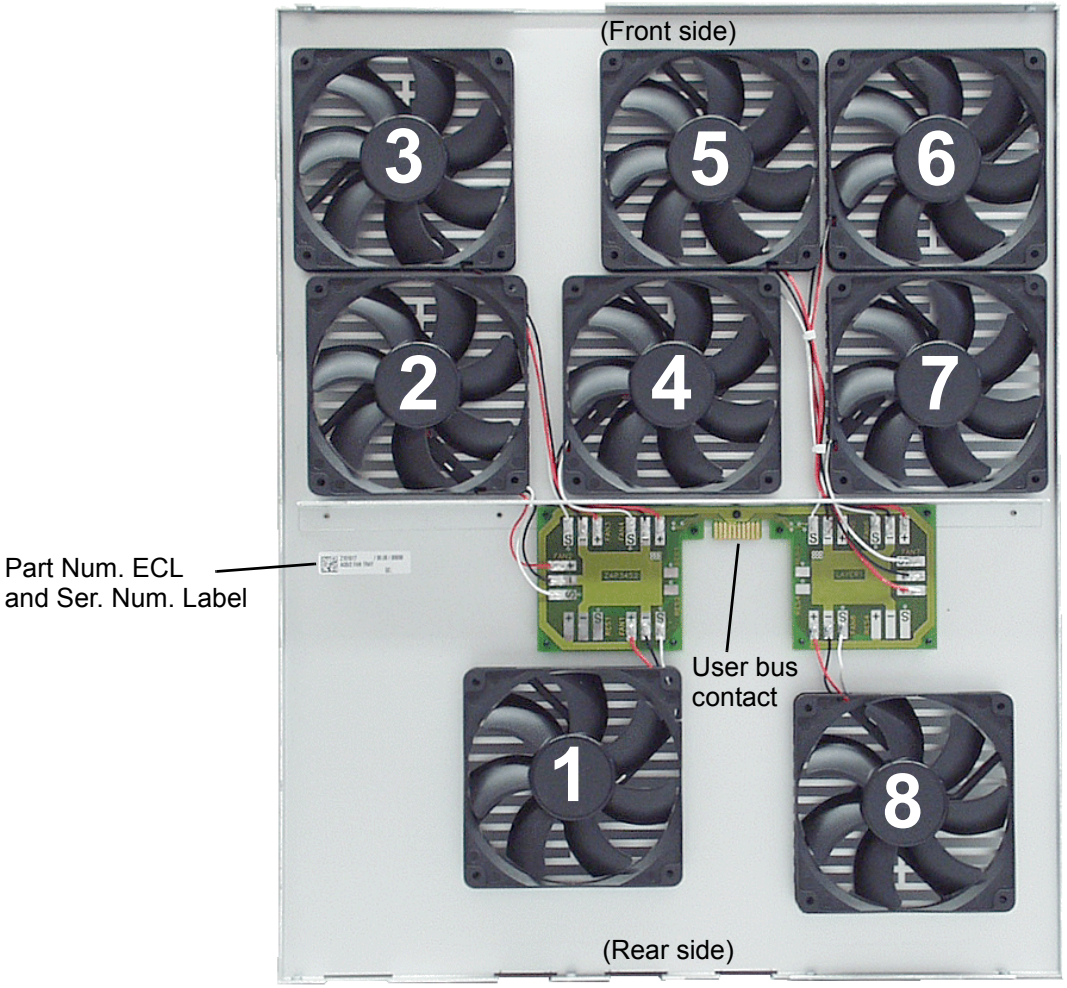
The fans are located in the fan tray on top of the mainframe. They are supplied and controlled via the AQS/3 user bus.

The fan tray is serviceable without removing the mainframe from the spectrometer cabinet. (see ***"Fan Tray Service Instructions" on page 69***)

The AQS/3 mainframe uses the same fan tray as the AQS/2 or AQS/2-M mainframe.

! ***Only use AQS/2 FAN TRAY (Z101617) with ECL03 or higher as a replacement.***

Figure 4.8. AQS/2 Fan Tray (Bottom view)



Fan Tray Service Instructions 4.15

! ***Only qualified Bruker personnel are allowed to service the AQS/3 mainframe.***

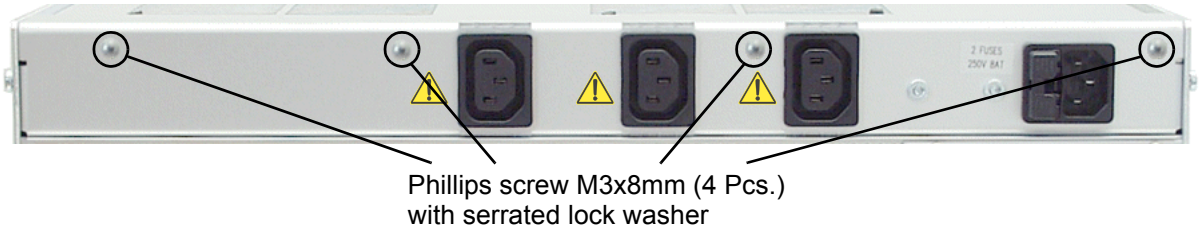
The fan tray removal and reassembly is the same as in the AQS/2 chassis. Please do not be confused if the pictures of the AQS/2 chassis are used in the following instructions.

Fan Tray removal 4.15.1

To remove the fan tray from the mainframe please follow the steps exactly as described below:

1. Turn of chassis with mains circuit breaker
2. Remove AC power line (rear side)
3. Remove 4 screws on the rear side

Figure 4.9. Fan Tray screws rear side

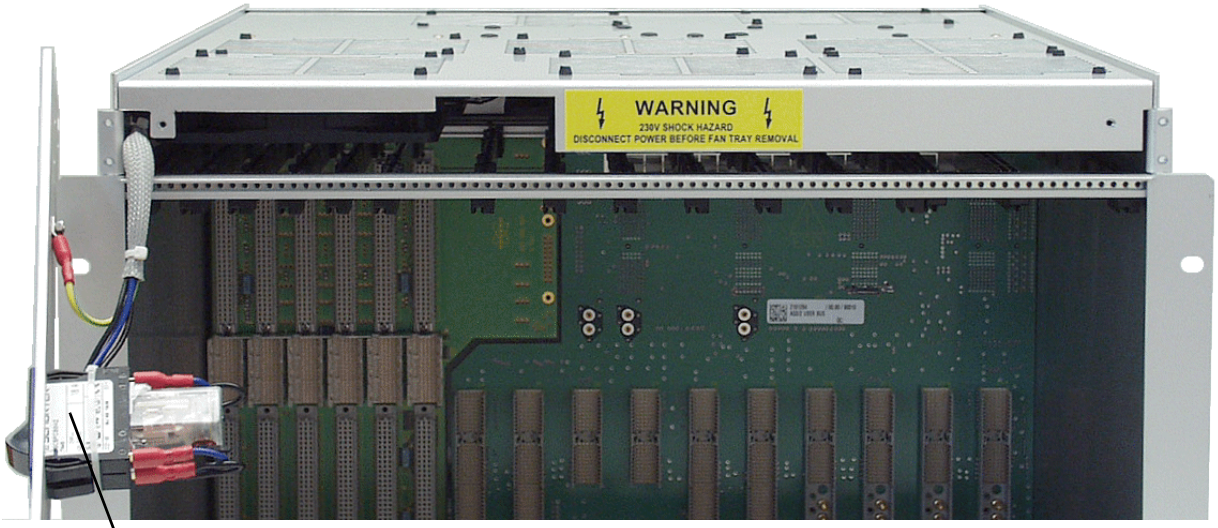


4. Remove 6 screws on the front side

Figure 4.10. Fan Tray screws front side

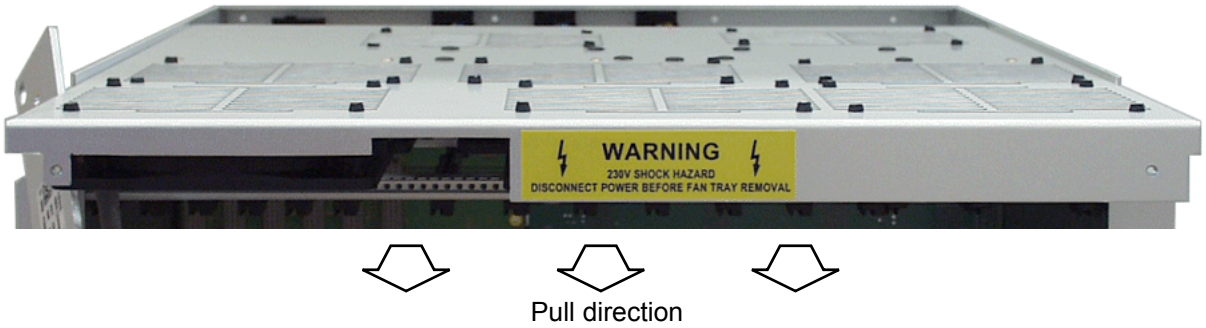
5. Carefully pull the front panel away from the mainframe and place it towards the left side (dangling from the cable)

Figure 4.11. Front panel removal



6. Remove the fan tray by pulling it gently towards the front

Figure 4.12. Fan Tray removal



Fan Tray reassembly *4.15.2*

To replace the fan tray in the mainframe follow the steps as described above in ***reverse order***.

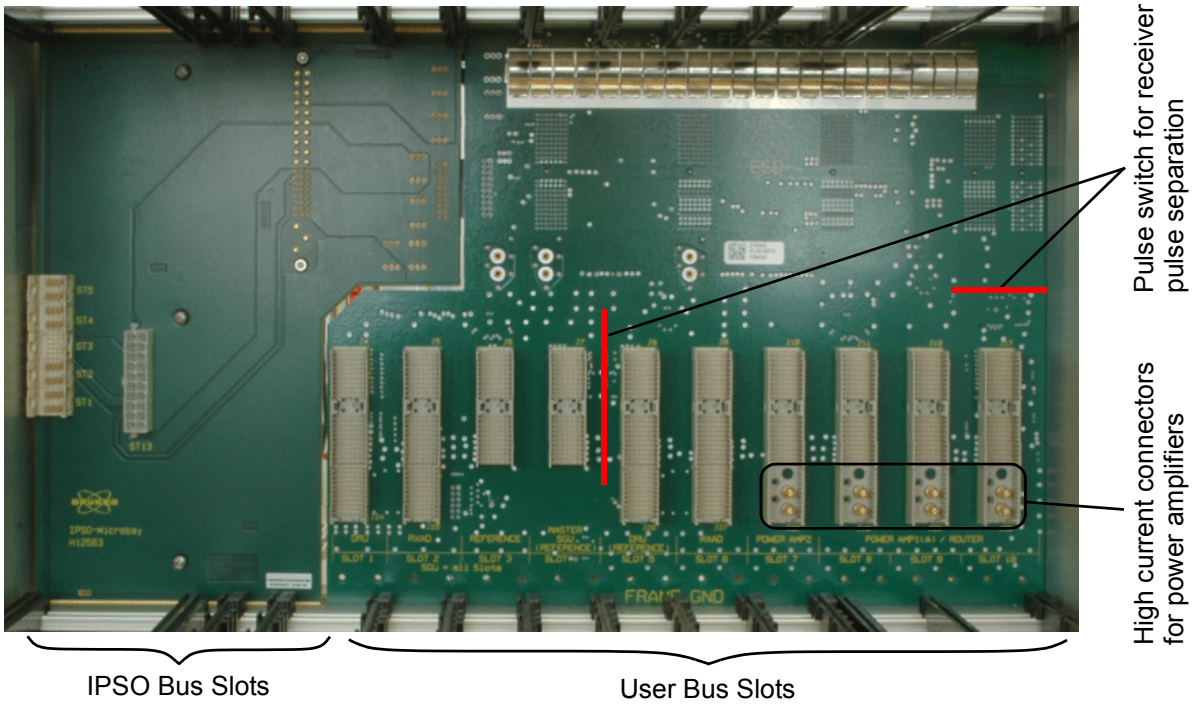
Make sure that:

- the fan tray sits flat on the guide rails on either side of the mainframe before final insertion
- no wires are squeezed in between the front panel and the fan tray
- all screws are secured and fastened properly (rear side screws with serrated lock washers)
- all fans turn freely after power up

Backplane (User Bus) 4.16

The User Bus is designed to route all signals and power supplies to the specific boards. It represents the ground point of the AQS/3 and is connected to the chassis frame. For detailed information about user bus signals see ***"AQS/2 signal and information paths" on page 15***, ***"Synchronous signals" on page 20*** and***"20MHz Clock Distribution" on page 29***.

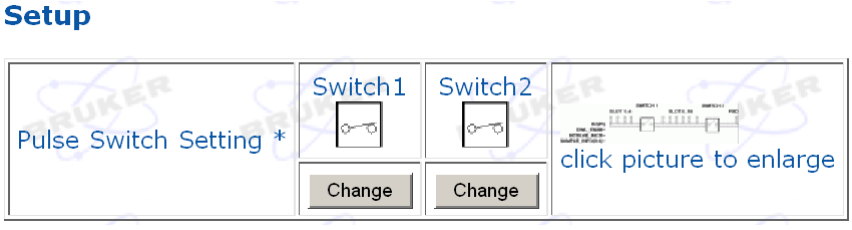
Figure 4.13. AQS/3 IPSO and User Bus (front view)



Pulse switch for receiver pulse separation 4.16.1

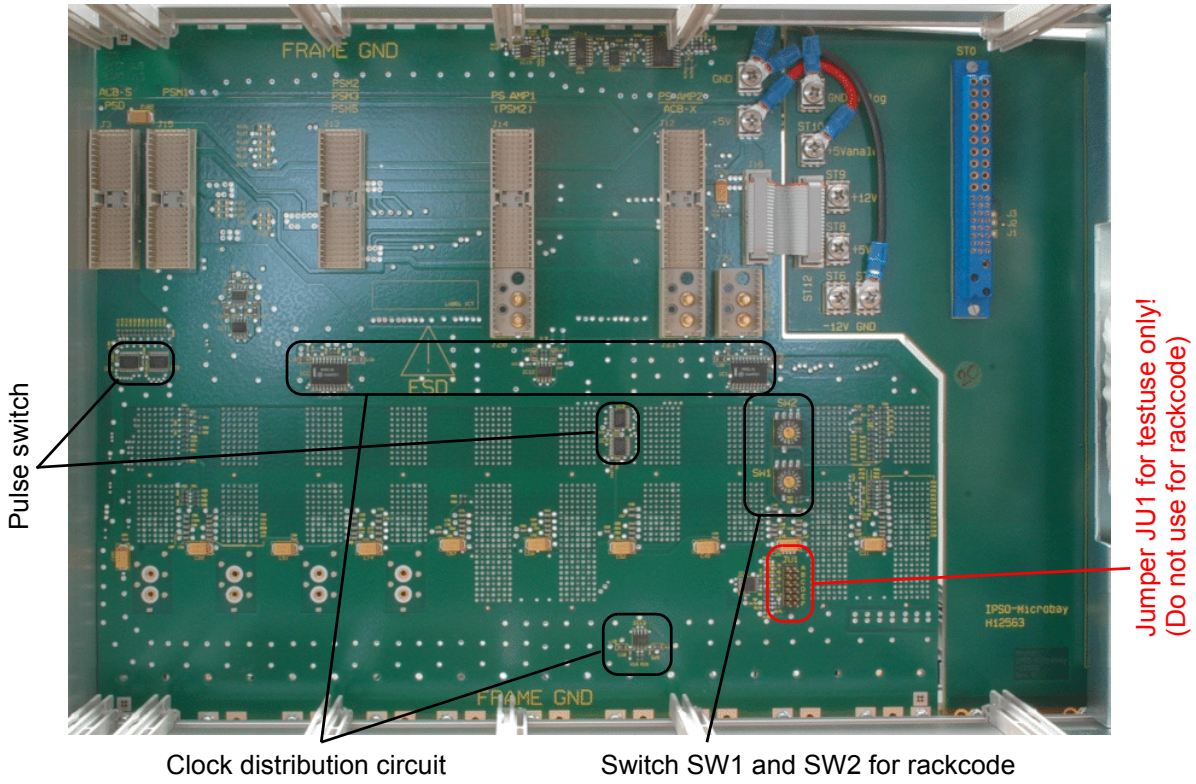
The User Bus is equipped with two pulse switches. One is located between slots 4 and 5, the other between slot 10 and the PSD slot. All switches are either controlled via the AQS controller or with a rotary switch (SW2) on the rear side of the user bus. The switch status can be checked and set via the AQS chassis page in the DRU service web.

Figure 4.14. DRU Service Web: AQS Chassis Setup



For a more detailed description of the SW2 switch functions see ***"Rackcode Settings" on page 72***.

Figure 4.15. AQS/3 IPSO and User Bus (ECL02, rear view)



Rackcode Settings ≥ ECL02:

The rackcode must be set according to the chassis configuration as described in the configurations section of this manual.

Table 4.2. Rackcode Switch Function

Switch [a]	Function	Setting [b,c]			
		0	1	2	**3**
SW2	Pulse Switch 1 = Slot 4 // 5	O	X	O	X
	Pulse Switch 2 = Slot 10 // PSD/3	O	O	X	X
SW1	AQS Controller	**1** = DRU in Slot 1			

a Example setting: Rackcode 0x31 = all pulse switches are closed and the DRU in Slot 1 is AQS controller.

b SW2 setting 4..F are note used

c O = open or remote controlled, X = permanently closed

Rackcode Settings ≤ ECL01:

Chassis with ECL ≤01 have jumpers JU1 A..F instead of the switches SW1 and SW2 for the rackcode setting. The rackcode setting scheme is the same as used with the AQS/2 chassis.

- JU1 A..D = AQS controller setting (HEX number)
- JU1 E = pulse switch between slots 4 and 5
- JU1 F = pulse switch between slot 10 and PSD/3

Table 4.3. Rackcode Setting Jumper JU1

0x	**N**		**N**				**Rackcode**
Jumper JU1 (Value)	F (2)	E (1)	D (8)	C (4)	B (2)	A (1)	Configuration
0x 3..	■	■					Single RX
0x 0..	-	-					Multi-RX or pulse switch controlled by AQS controller
0x ..1			-	-	-	■	AQS controller = DRU1 in Slot 1

■ = Jumper closed [-] = Jumper open

Example setting: Rackcode 0x31 = Single RX with DRU controller
(Jumper JU1A, JU1E and JU1F must be closed)

Figure 4.16. User Bus Block Diagram

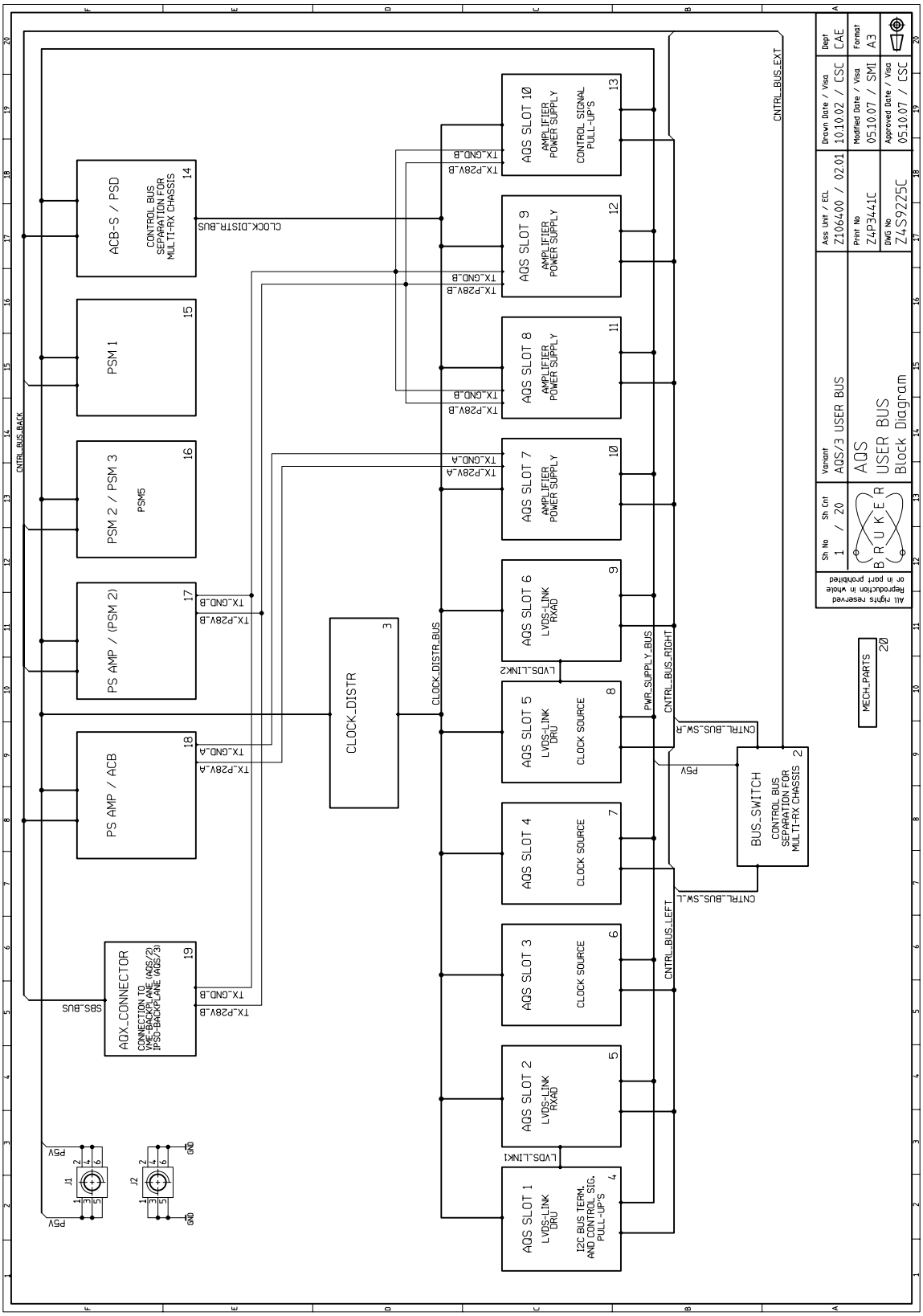


Figure 4.17. Fan Control & Pulse Switch

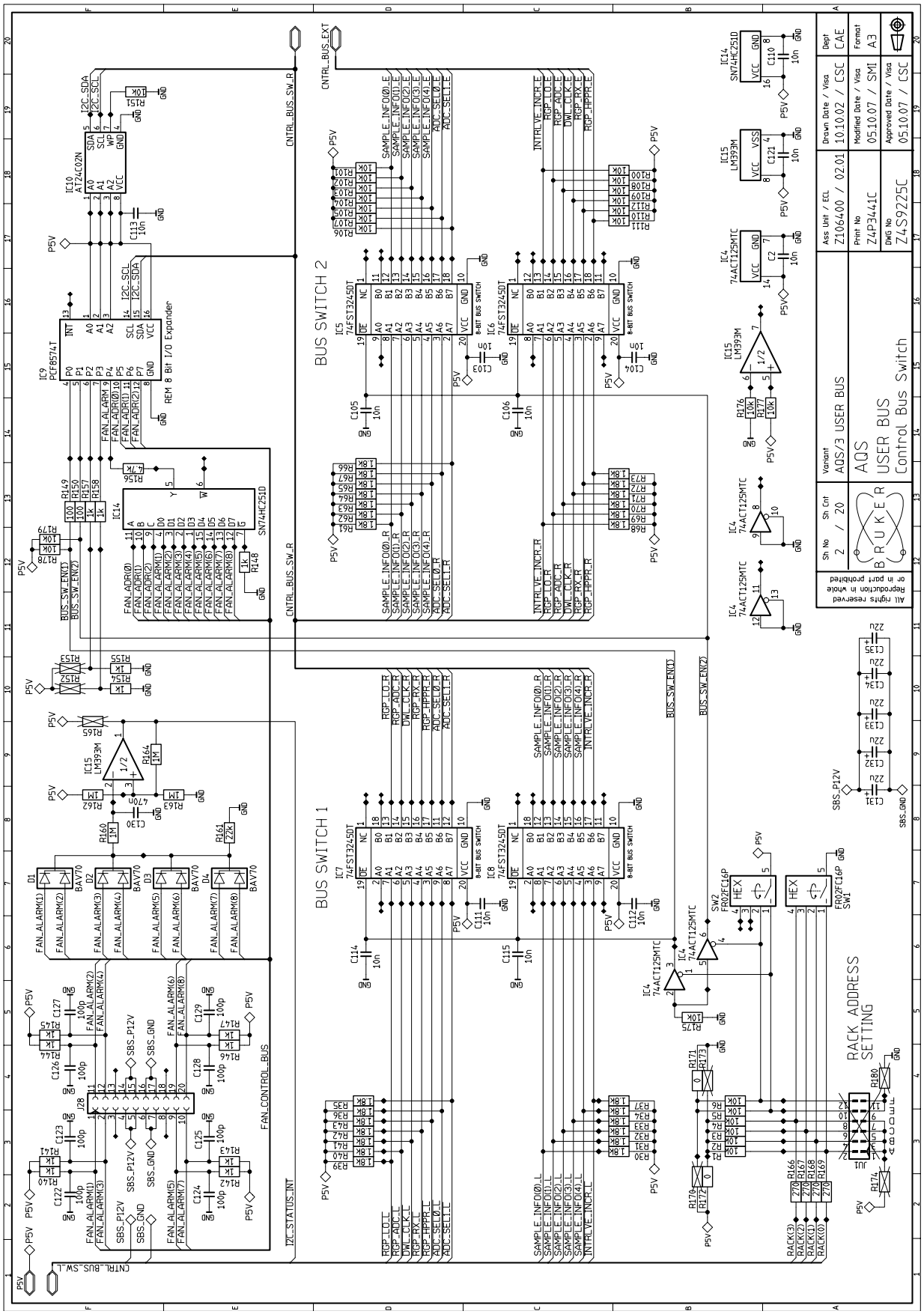


Figure 4.18. Clock Distribution

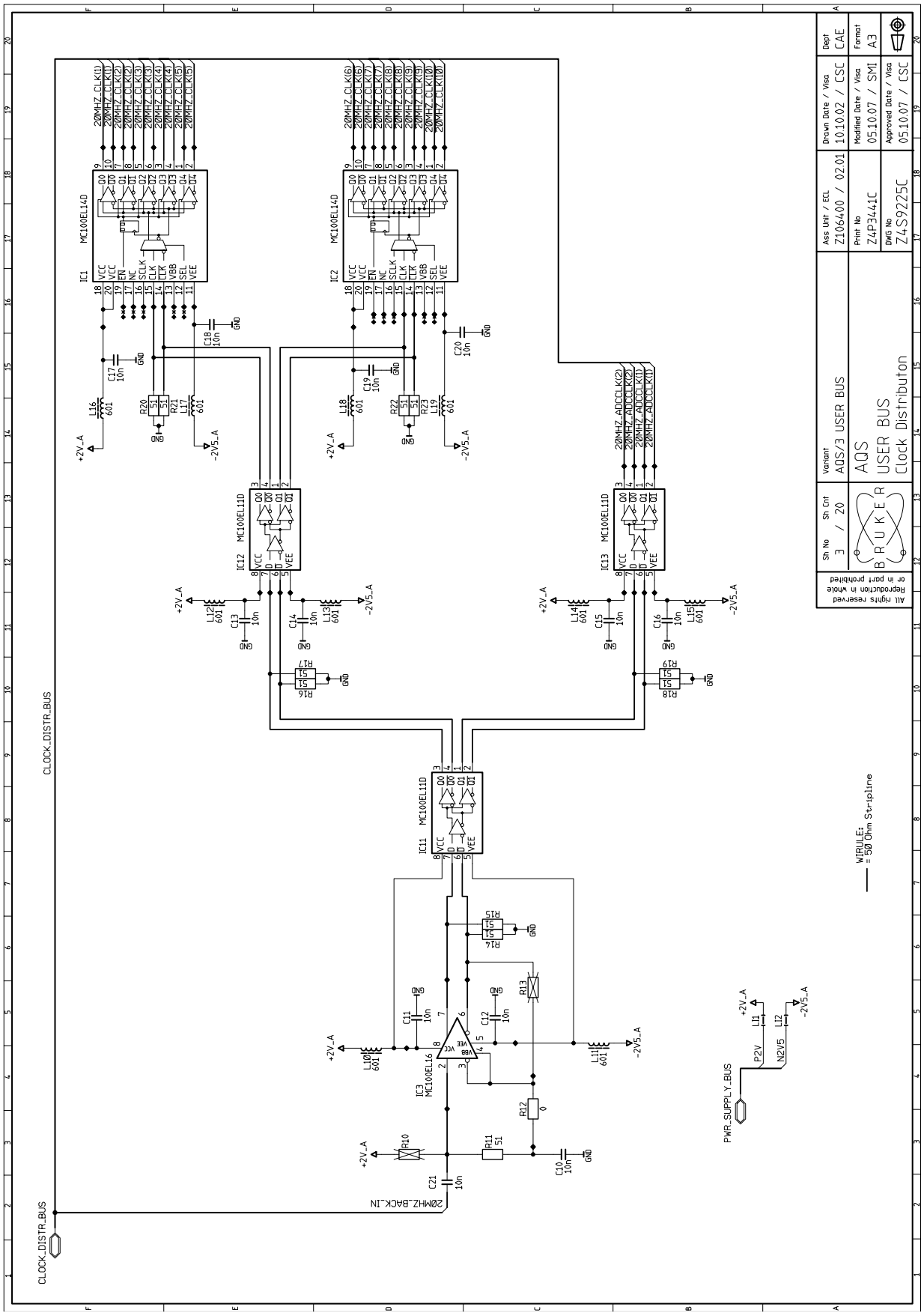


Figure 4.19. User Bus Slot 1

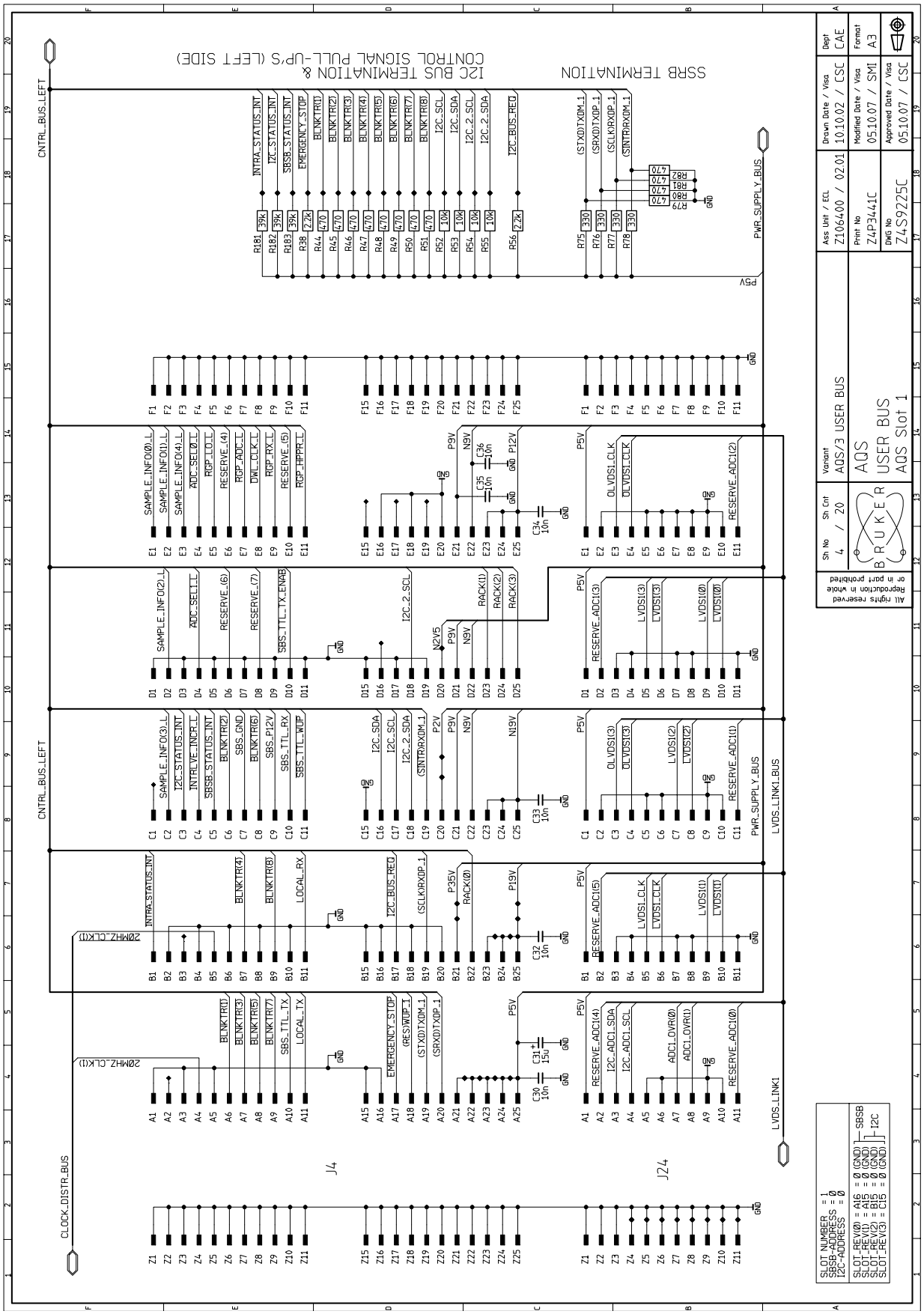


Figure 4.20. User Bus Slot 2

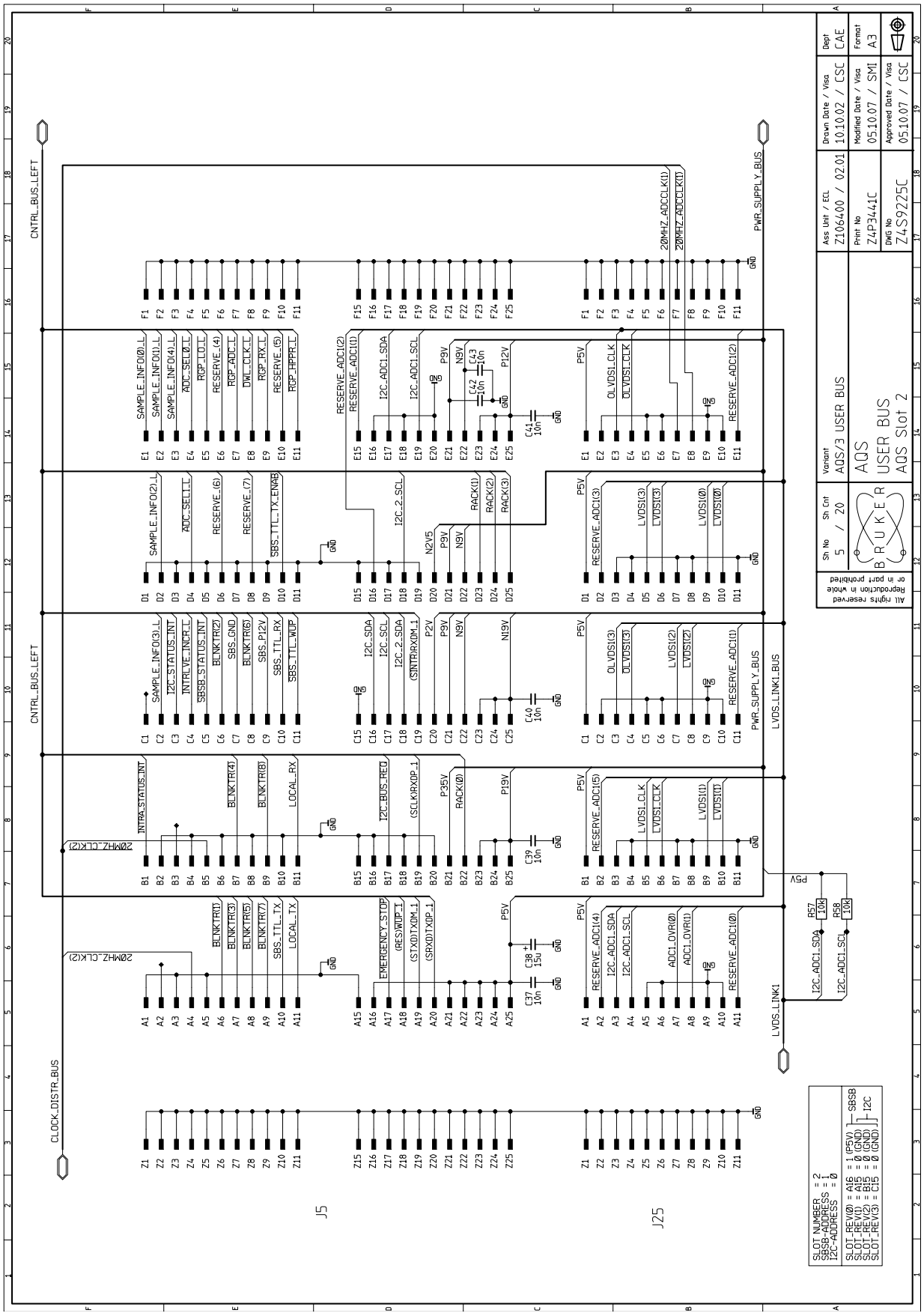


Figure 4.21. User Bus Slot 3

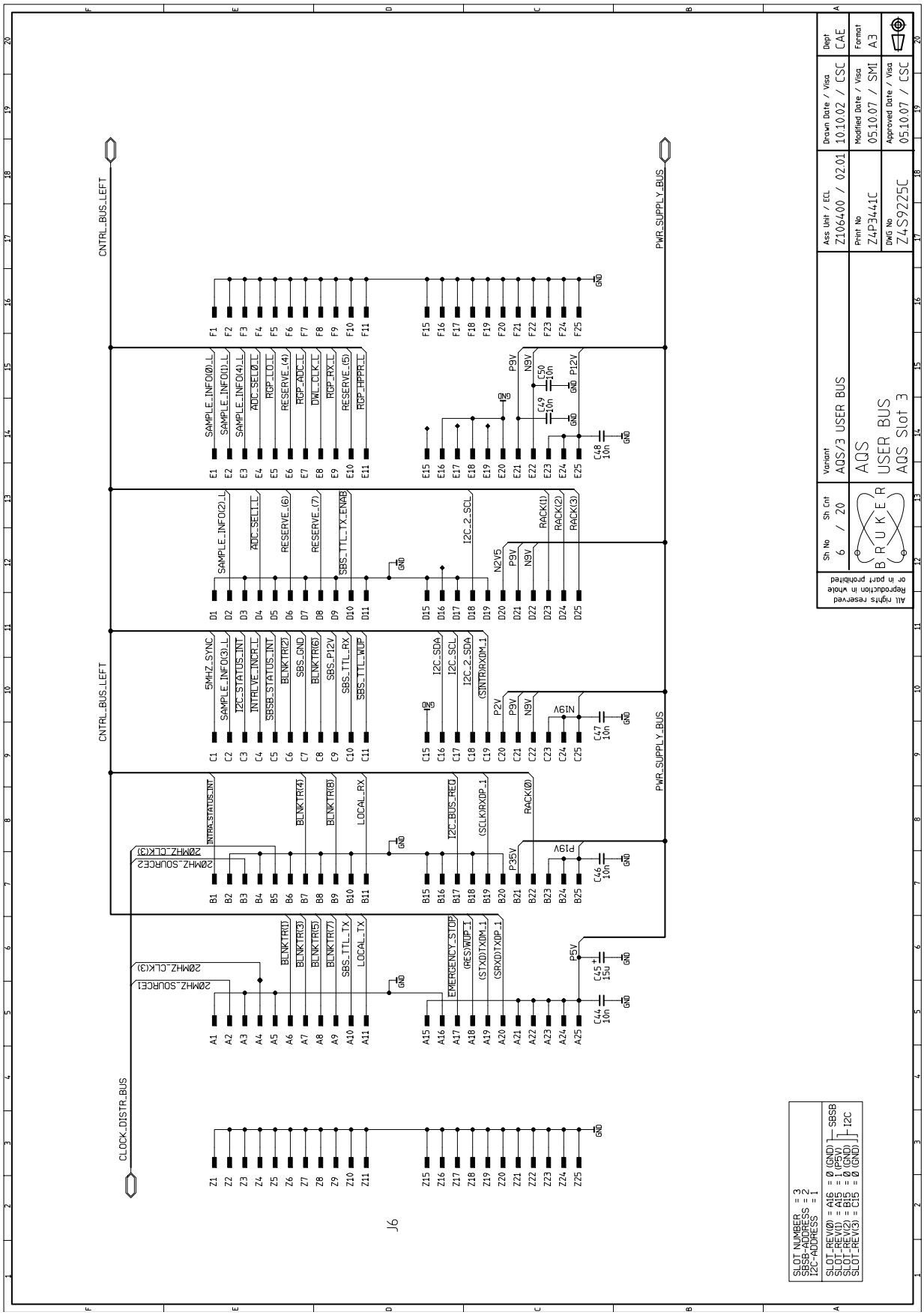


Figure 4.22. User Bus Slot 4

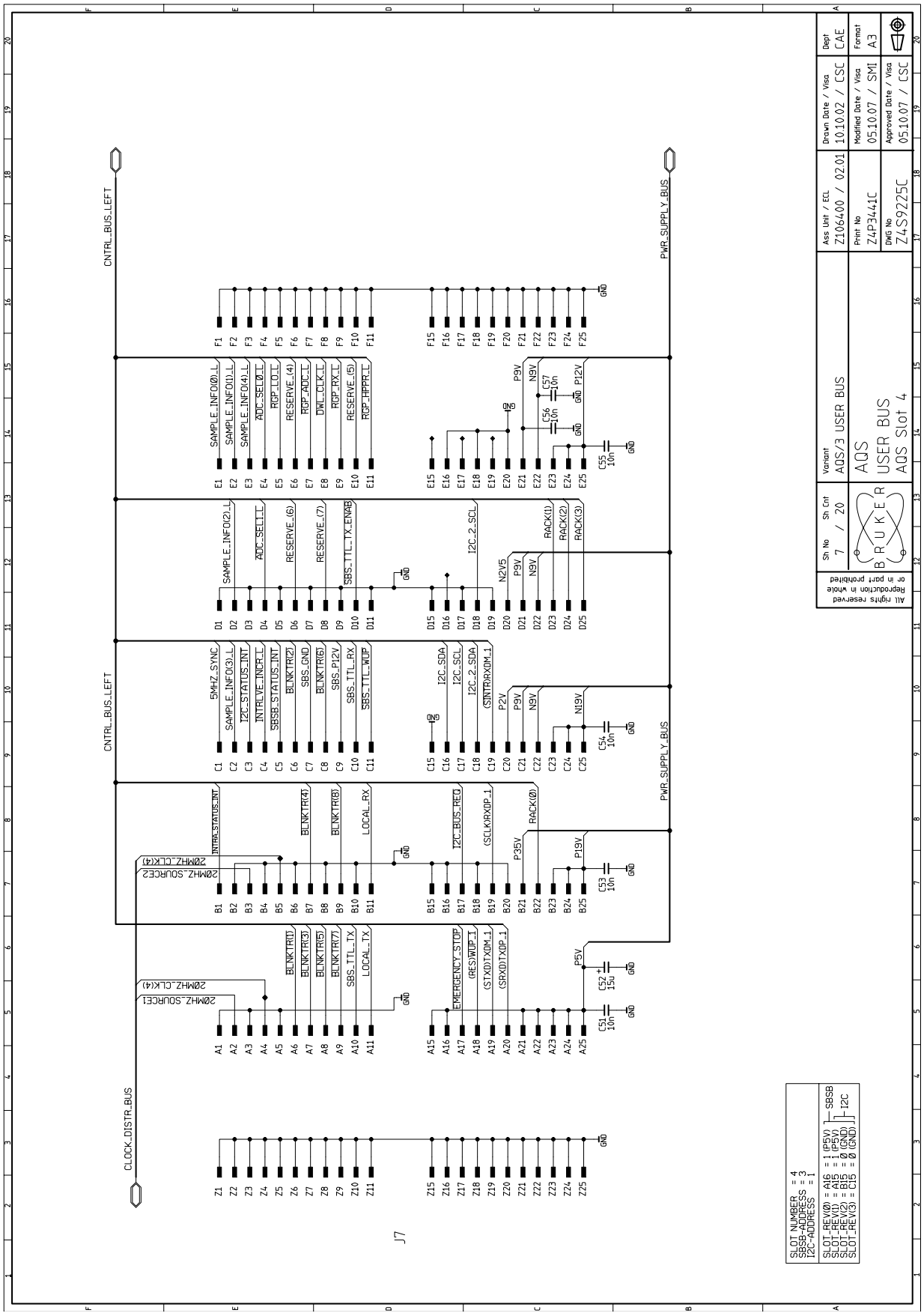


Figure 4.23. User Bus Slot 5

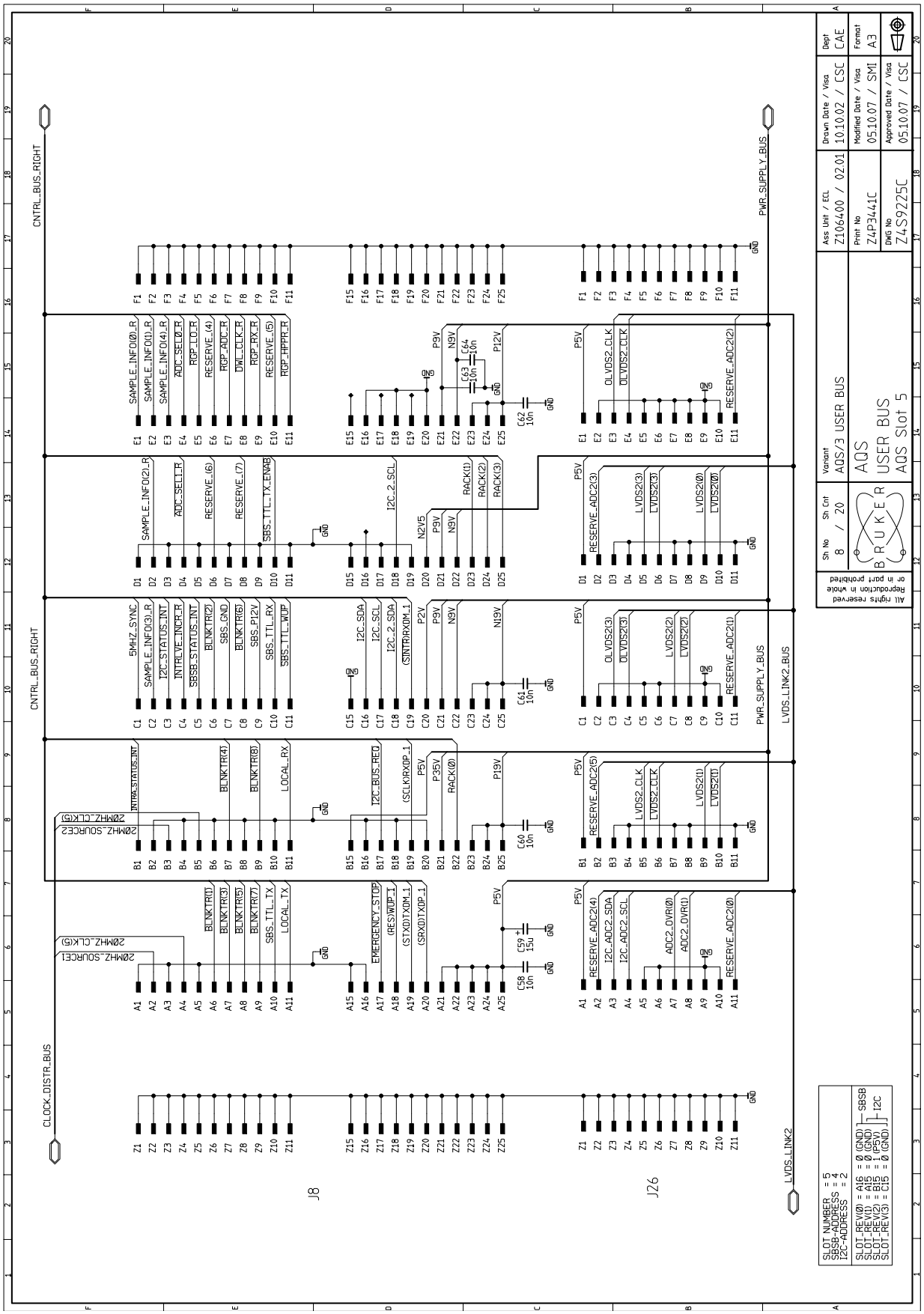


Figure 4.24. User Bus Slot 6

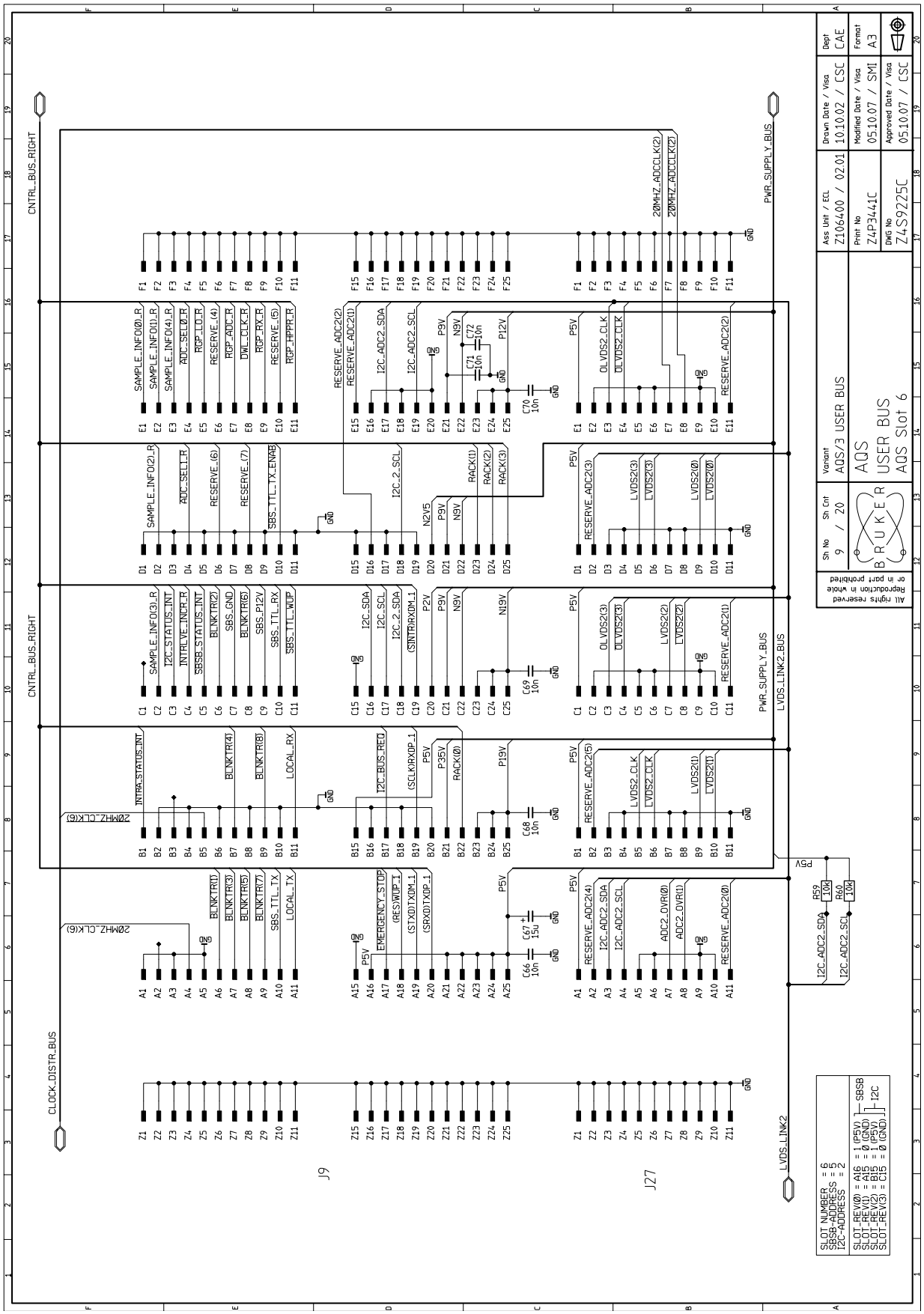


Figure 4.25. User Bus Slot 7

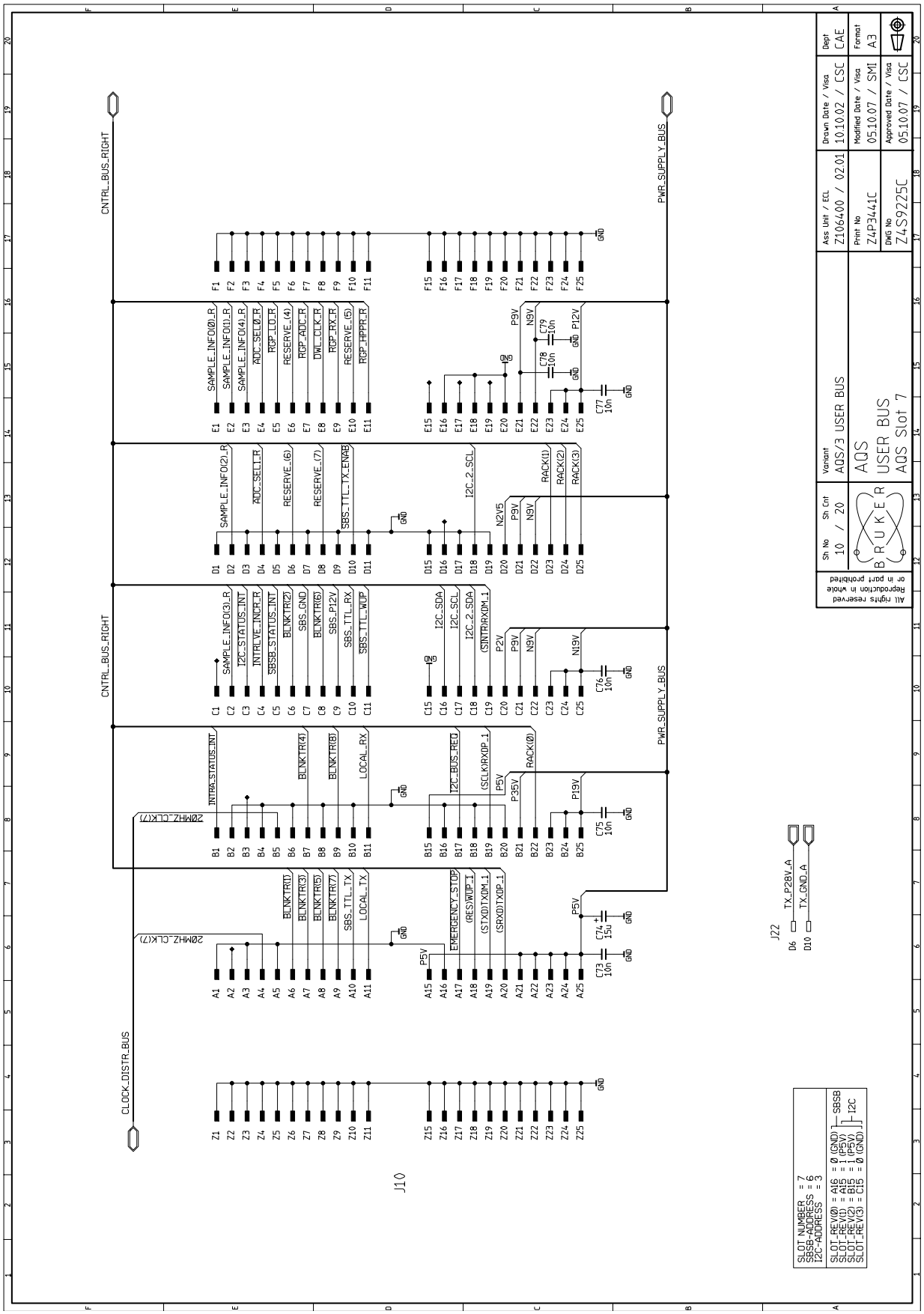


Figure 4.26. User Bus Slot 8

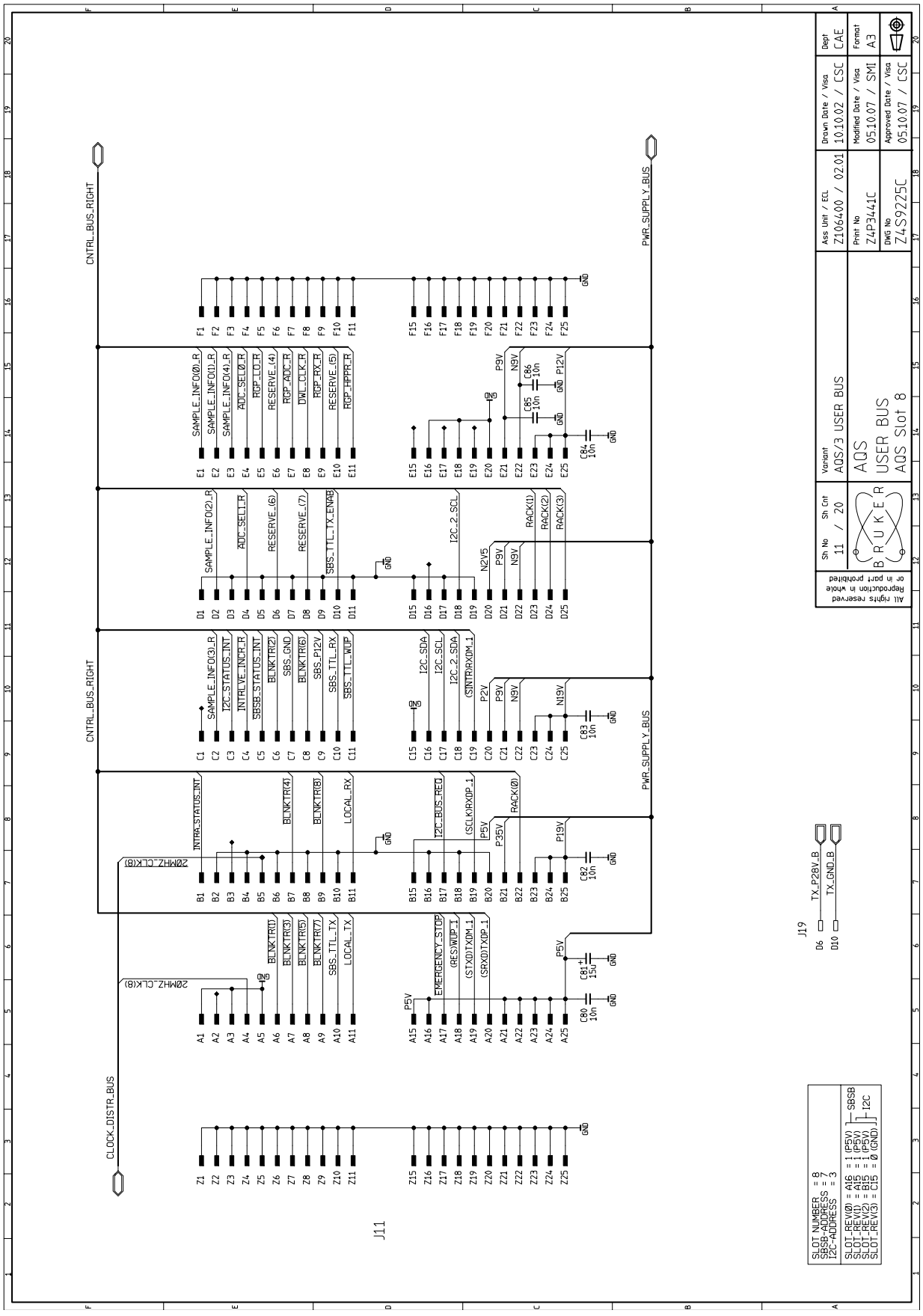


Figure 4.27. User Bus Slot 9

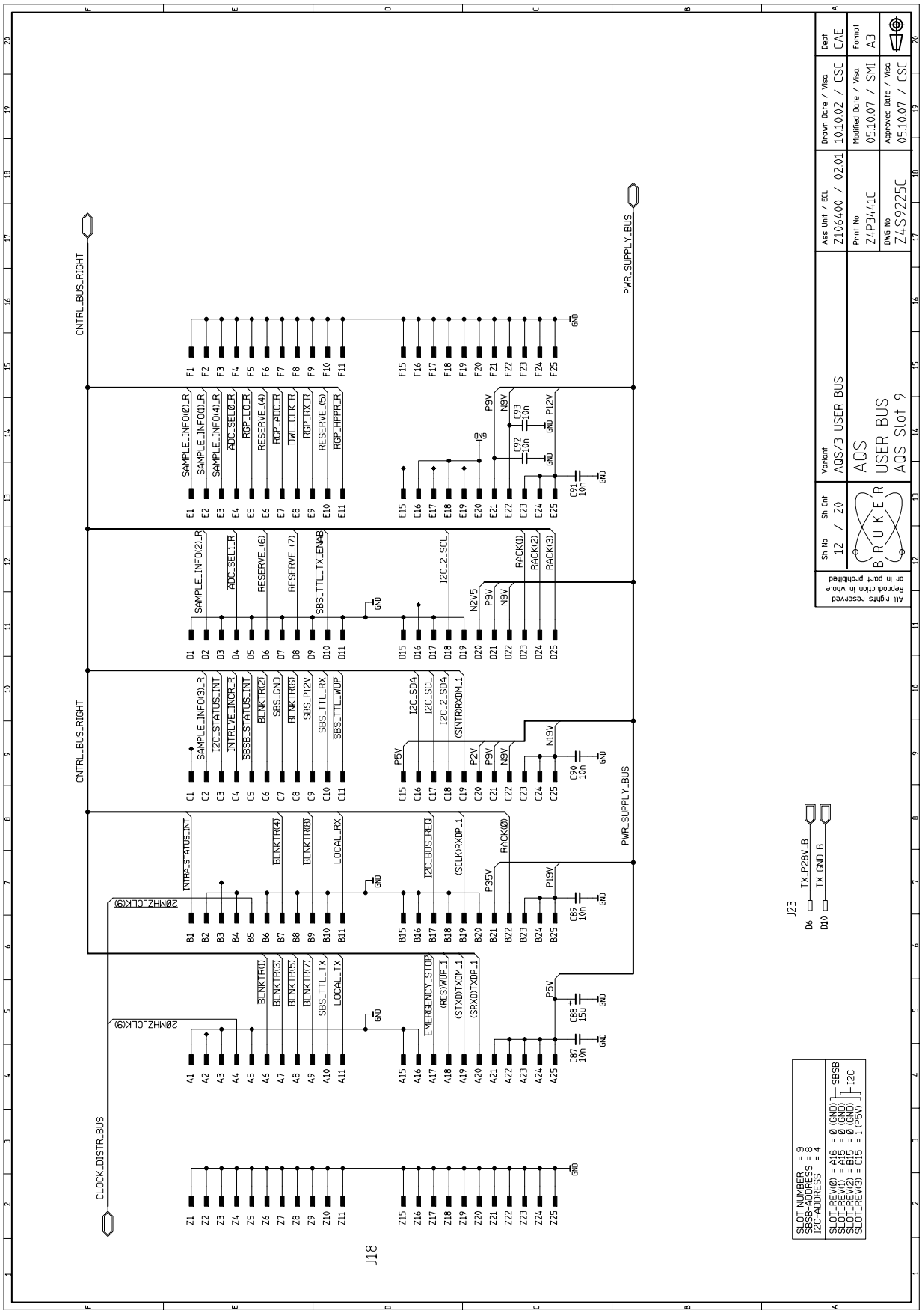


Figure 4.28. User Bus Slot 10

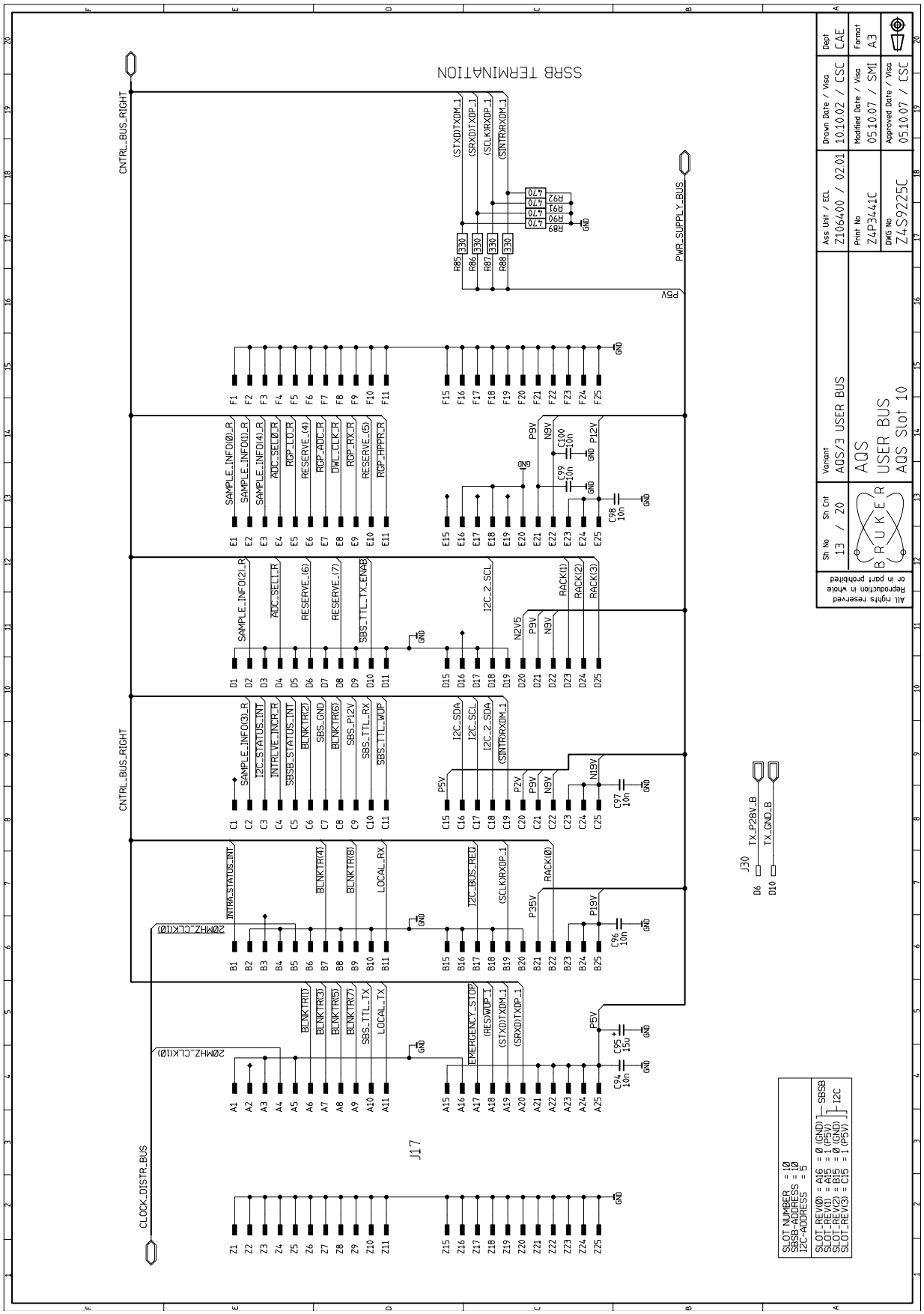


Figure 4.29. ACB Standard/ PSD Slot

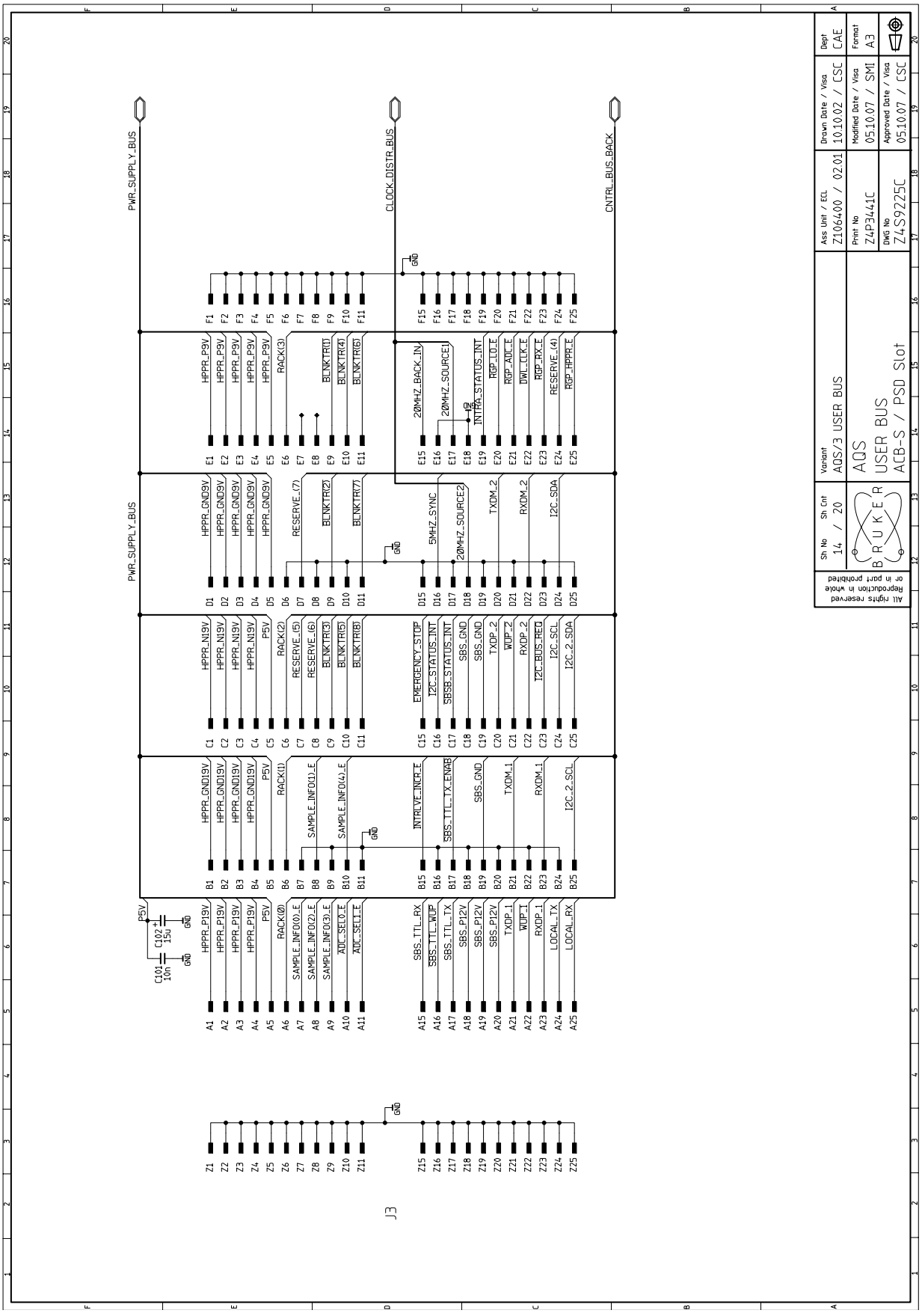


Figure 4.30. Power Supply Slot 1

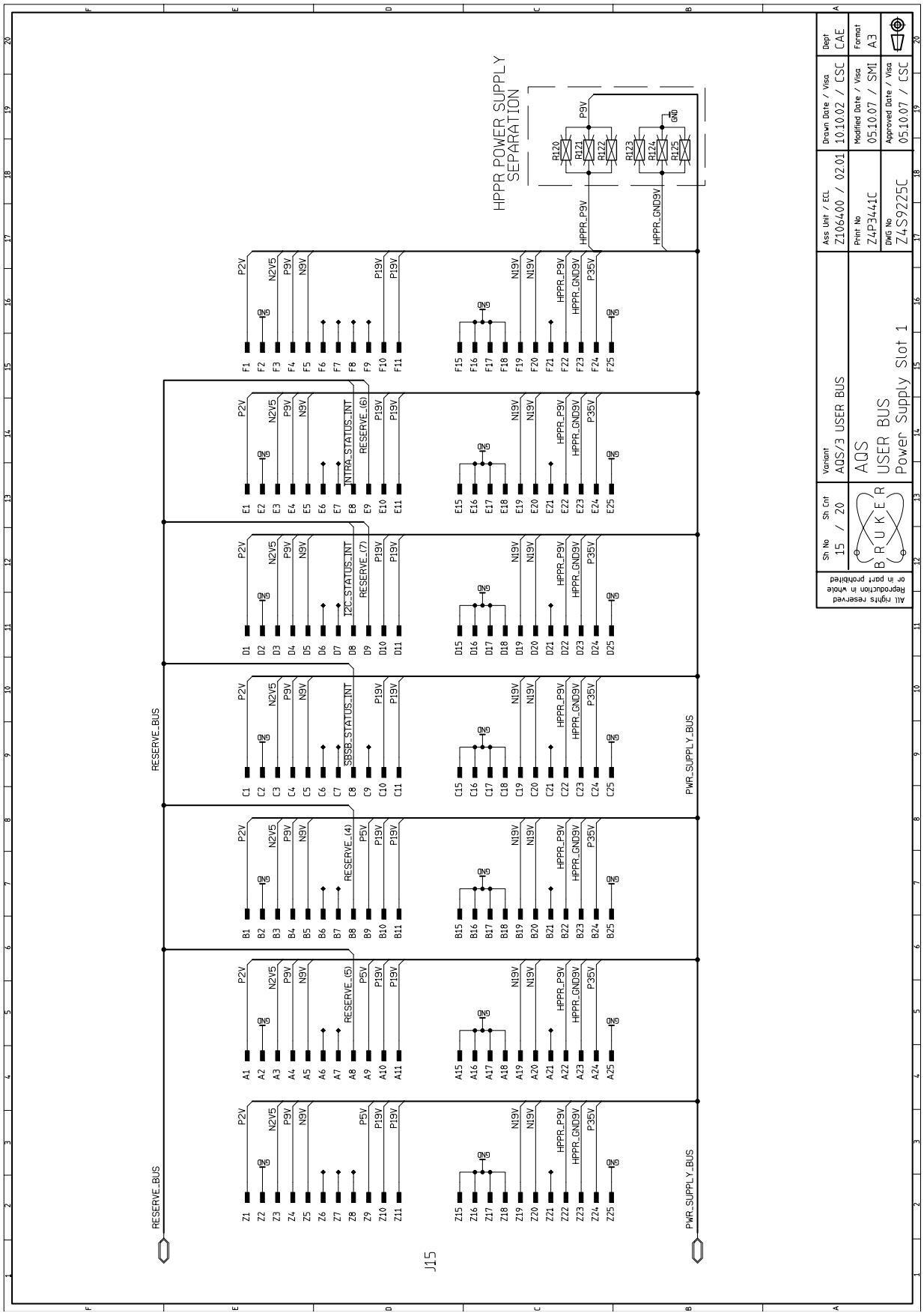


Figure 4.31. Power Supply Slot 2

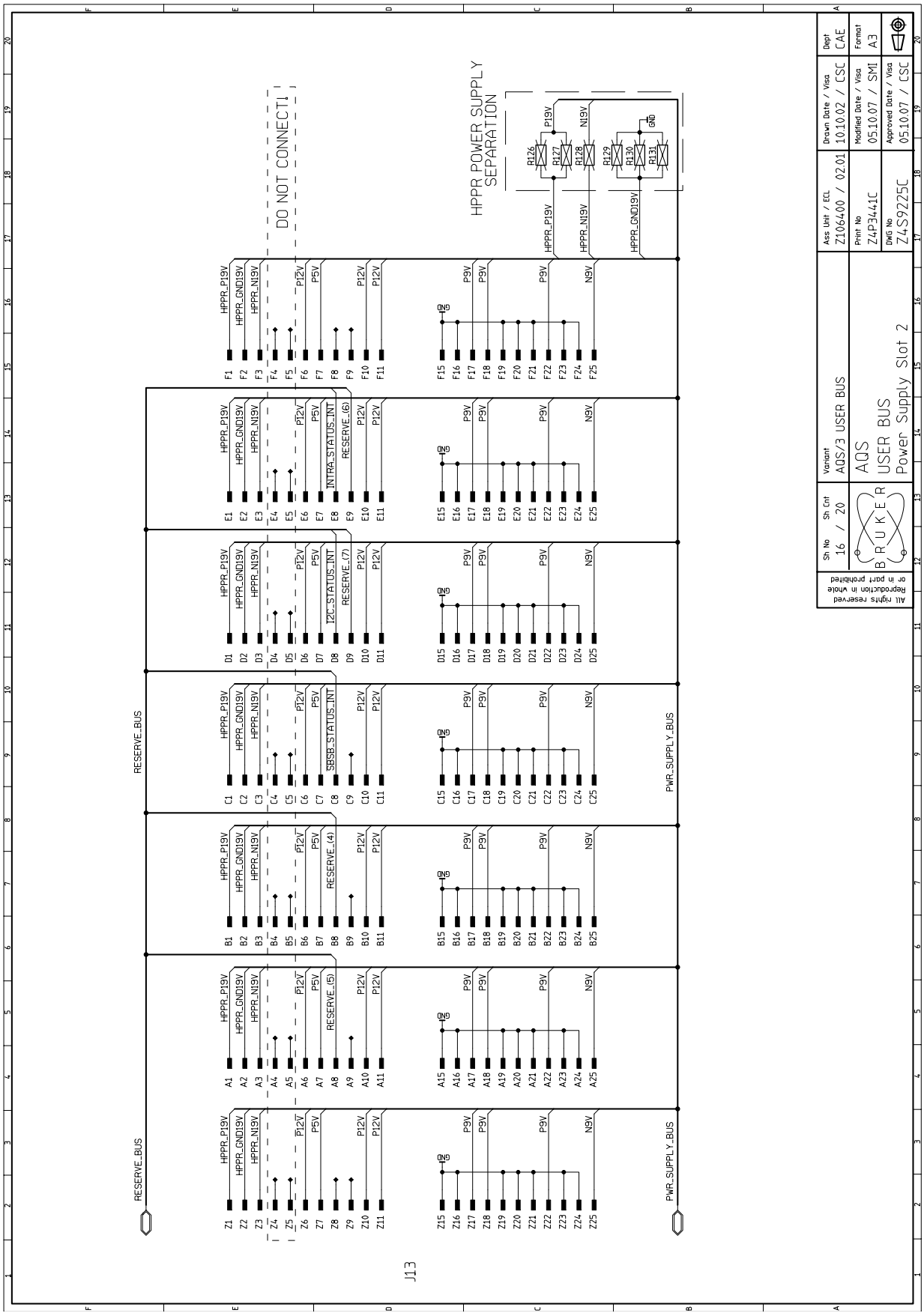


Figure 4.32. Power Supply Slot 3

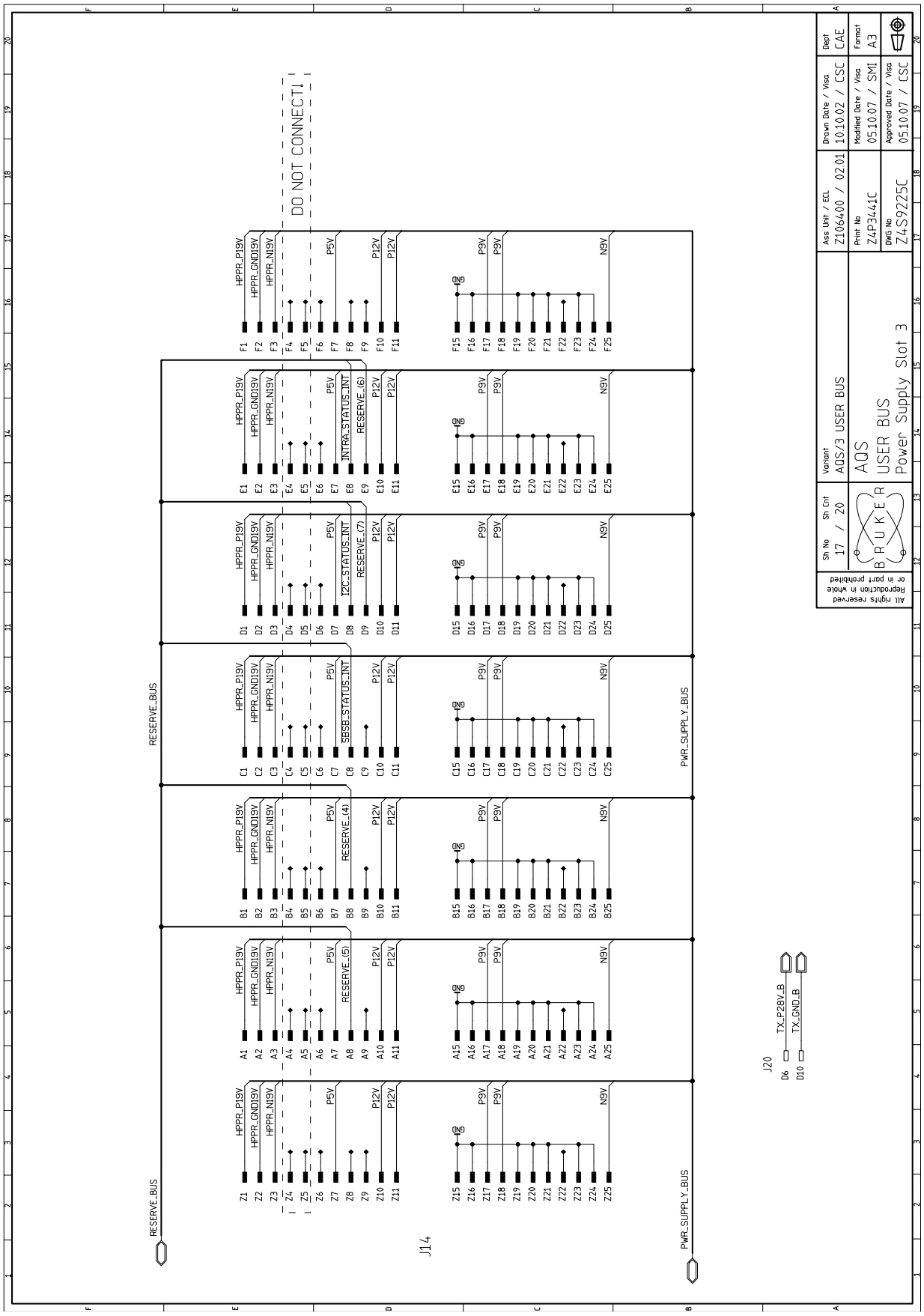


Figure 4.33. ACB-X Slot (PS Slot 4)

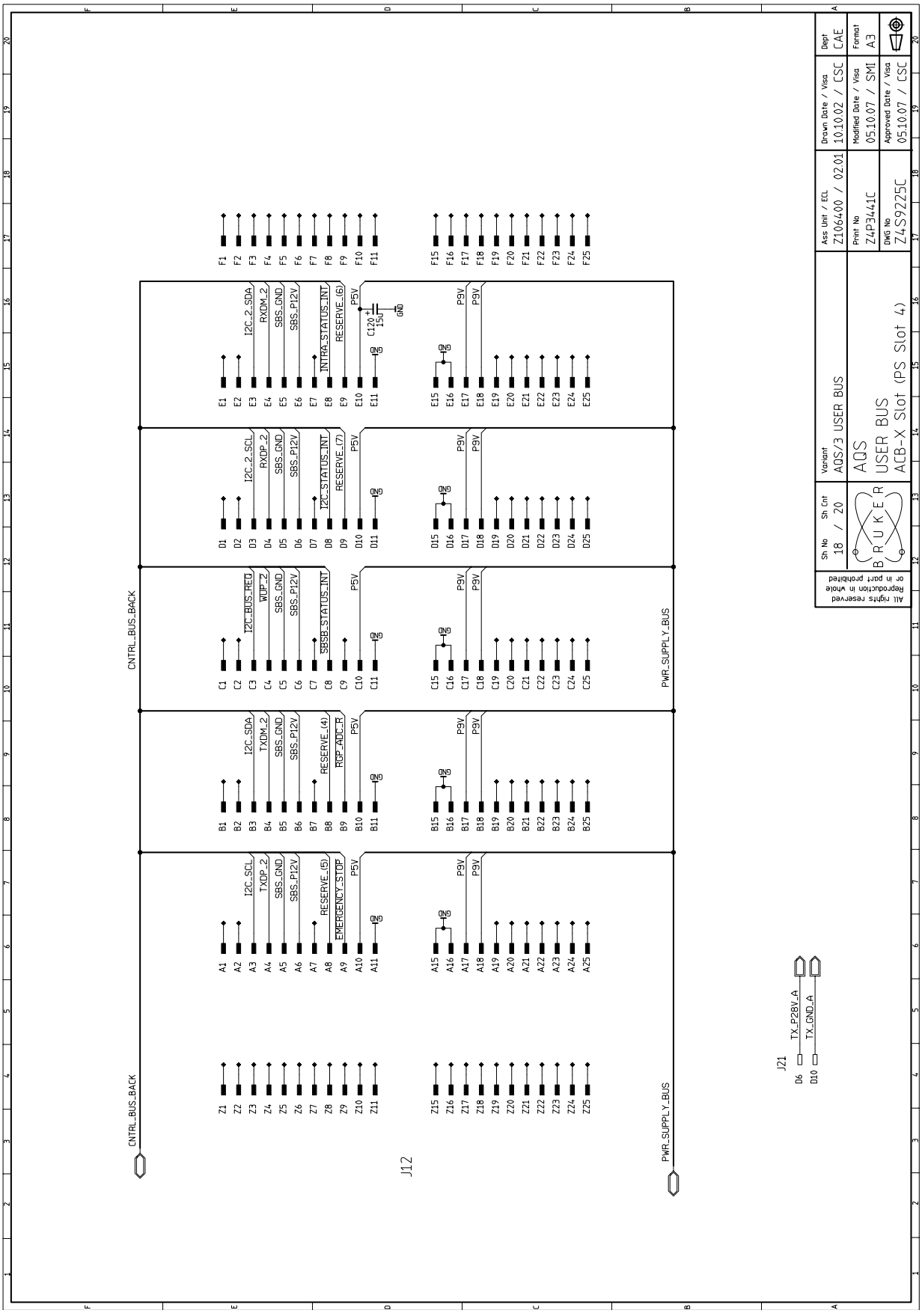
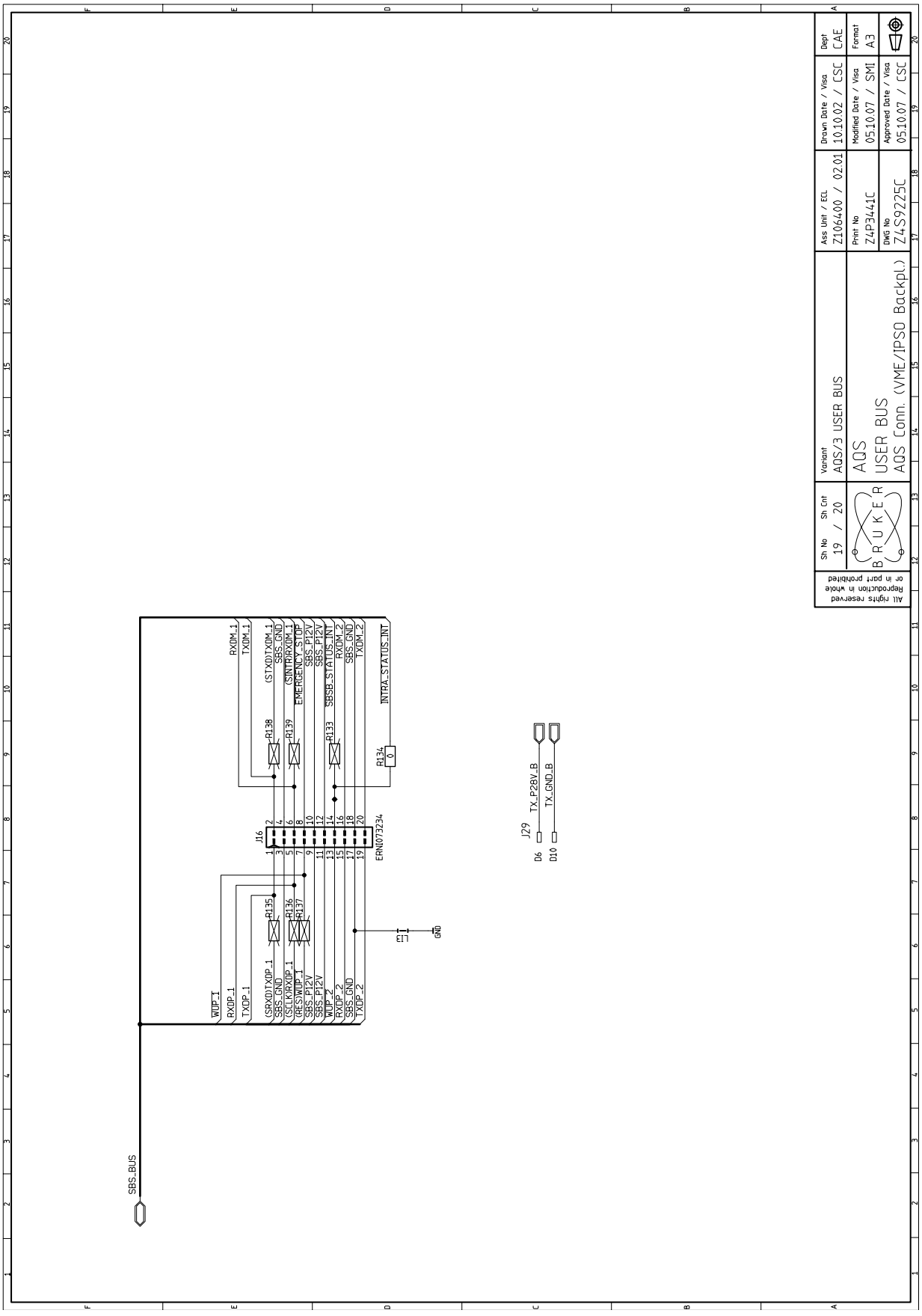


Figure 4.34. AQS Connector (to IPSO Backplane)



AQS/2-M Mainframe 5

Introduction 5.1

The AQS/2-M mainframe is a variant version of the AQS/2 mainframe. One chassis may contain up to 7 receiver channels. It has 14 aqs-slot on the user bus and no VME-bus.

The user bus is designed to be equipped with AQS RF receiver units (DRU and RXAD). For special configurations other units like SGU, Reference Board, 1-4 Router or AQS Preamp may be used.

! ***Units like 3-Channel Router, SADC, HADC/2, RX-22 Receiver or power amplifiers such as BLA2BB or 2H-TX cannot be used in this chassis.***

On the rear side, linear power supply modules (PSM1 &PSM5) and the switched power supply (PS Digital) are placed. One slot (AUX2) is reserved for the AQS RF-SPLITTER board.

The transformer, which feeds the linear power supply modules, is part of the mainframe and is located on the rear side.

The mainframe is cooled with 8 fans, which are located in a fan tray on top of the mainframe. The fan tray is serviceable without removing the mainframe from the spectrometer cabinet. (see ***"Fan Tray Service Instructions" on page 103***)
The fan tray is the same as in the AQS/2 chassis.

Technical Data 5.2

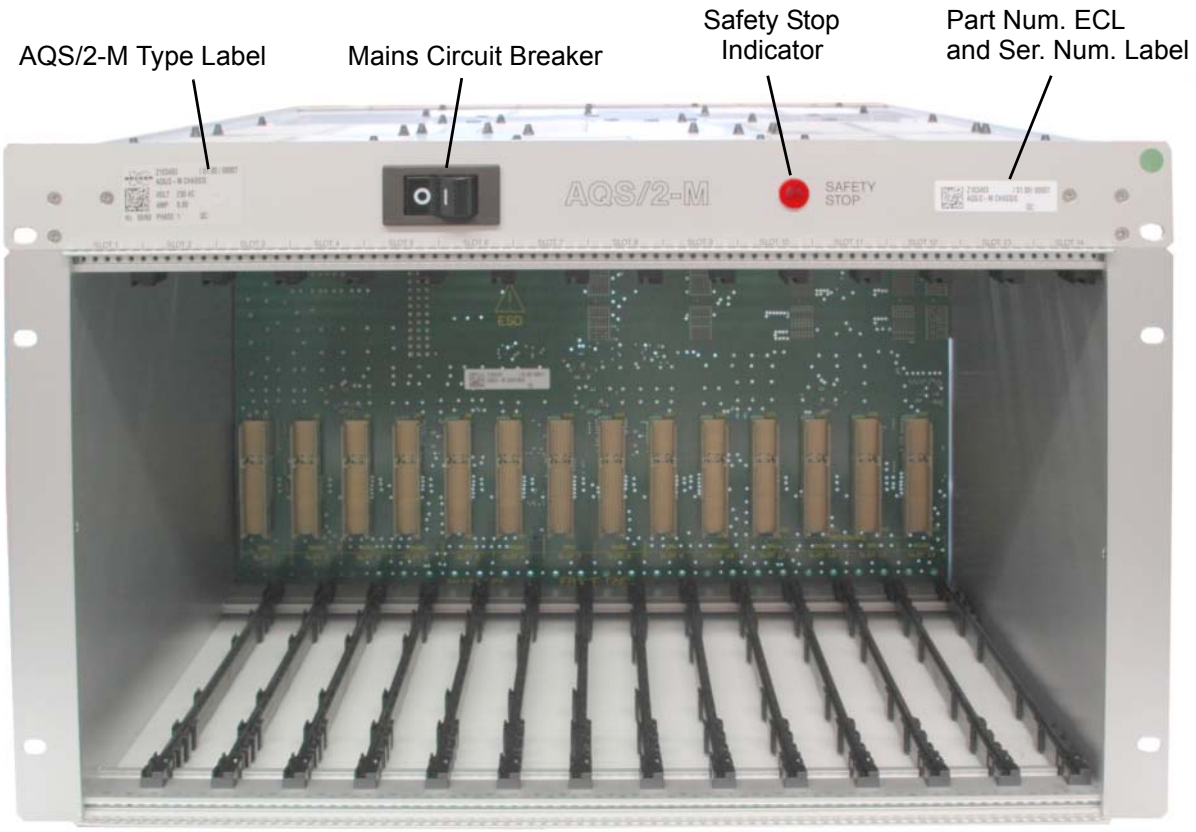
AC input voltage	208..230	V~
AC frequency range	47..63	Hz
AC input current	max. 8	A~
AC input inrush current	limited to approx. 20	Apk
AC fuse (2pcs. 5x20mm, time-lag T, type H)	8A~ / 250V~	
Dimensions (hight x width x depth)	310 x 483 x 570	mm
Weight (without units)	approx. 20	kg

Environmental conditions:

The AQS/2-M mainframe is designed as a subunit in the electronics cabinet of the spectrometer. For the environmental conditions outside the cabinet please refer to the site planning guide of the spectrometer system.

Front View *5.3*

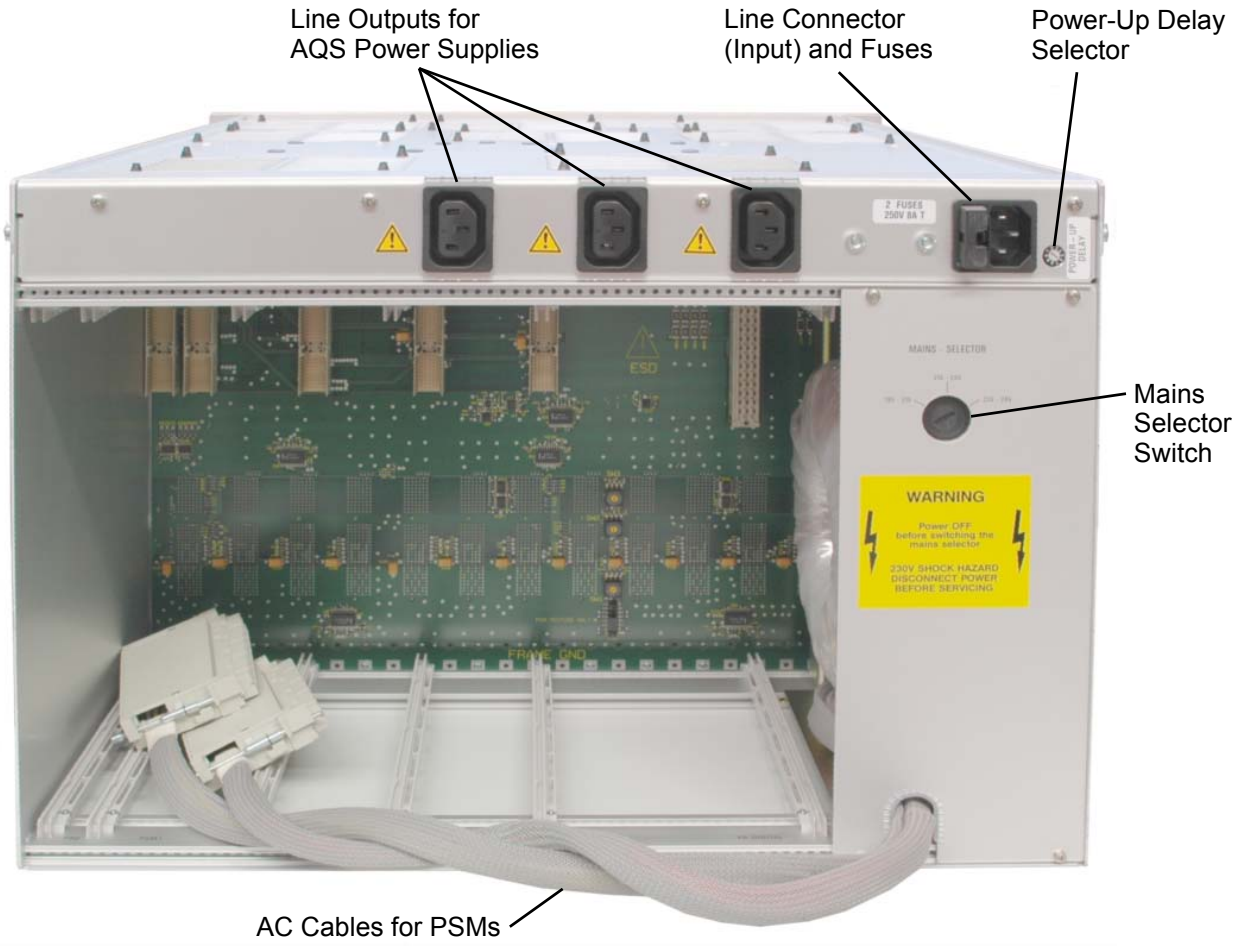
Figure 5.1. AQS/2-M Chassis front view



Rear View 5.4

The rear view shows the housing of the power supply boards. On the right hand side is the transformer housing with the appropriate AC cables.

Figure 5.2. AQS/2-M Chassis rear view



Line Outputs:

Only connect AQS POWER SUPPLY units to these connectors.

- AQS POWER SUPPLY DIGITAL 350W (H9489)
- AQS PSM5 POWER SUPPLY MODULE (Z102023)
- AQS PSM HPLNA (Z104783)
- AQS PSM ADM (Z107413)

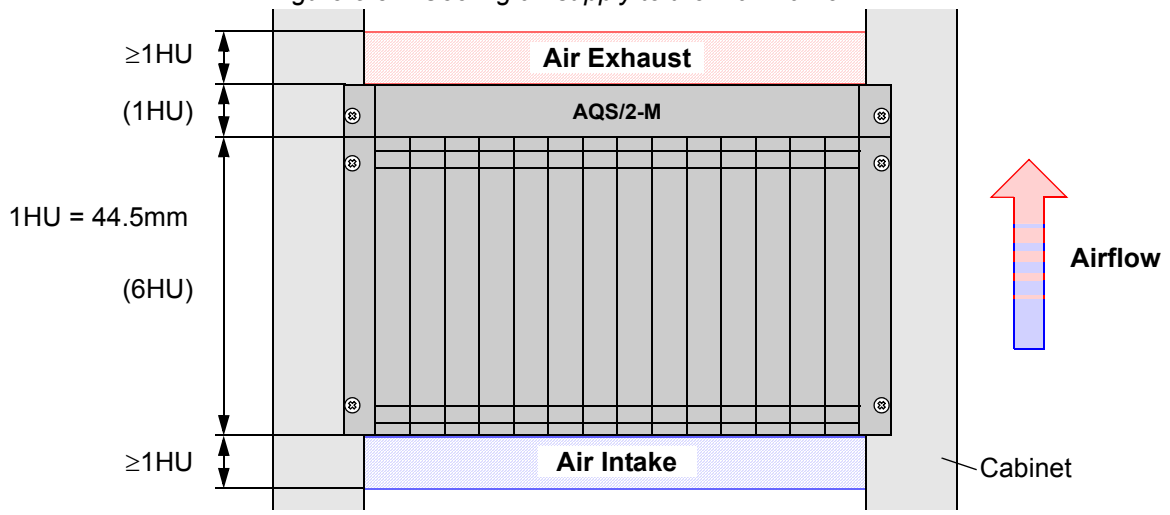
Installation in electronics cabinet 5.5

The AQS/2-M mainframe must be installed at it's designated position in the electronics cabinet to ensure proper air ventilation for the cooling fans. The position may vary in different cabinet types and sizes.

! ***At least one height unit (1HU) above and below the mainframe must be reserved for the cooling air supply.***

Special air baffle plates may be used to support efficient ventilation. Typically the air intake is from the front and the exhaust towards the back of the cabinet.

Figure 5.3. Cooling air supply to the mainframe



The mainframe must be fixed by at least 4 screws into the cabinet. The power cable is included in the cabinet wiring.

Preparation for Use 5.6

Prior to the first power-up of the AQS/2-M mainframe, it must be ensured that the mains selection switch is in the correct position. (see selector on the back side of the AQS/2-M)

The size of the linear power supply modules are designed for minimal power dissipation; therefore the transformer input voltage should be matched to the mains voltage at the installation site.

Generally, the mains selection switch should be set to the corresponding voltage range, even if the mains power is weak (max. fluctuations ± 6%).

- Factory setting for 230V~ mains supply = 220-245V~

Selector Setting for combined Voltages 5.6.1

In countries with 110-120V~ mains supply such as USA and Canada combined line voltages may be used. In this case set the selector switch to 195-215V~.

AC Power Line Fuses 5.7

The AQS/2-M is protected by two fuses as specified on the power supply nameplate. The fuses are located in a removable fuse holder next to the AC power connector. Always use time-lag T fuse types with high breaking capacity H.

Power-Up Delay 5.8

The power-up delay can be selected with a rotary switch next to the power connector at the back of the mainframe. Please set the switch according to your configuration as described in the configurations section within this manual. The minimal power-up delay is 0.5s due to the inrush current limiter circuit.

Table 5.1. Power-Up Delay

Setting	Delay
0	0.5 s
1	2 s
2	4 s
3	6 s

Setting	Delay
4	8 s
5	10 s
6	12 s

Setting	Delay
7	14 s
8	16 s
9	18 s

Inrush Current Limiter 5.9

The mainframe is equipped with an inrush current limiter which limits the peak current to approx. 20A. The limiter is always active, even after a „hot start“ when the chassis is switched OFF / ON within a short timespan.

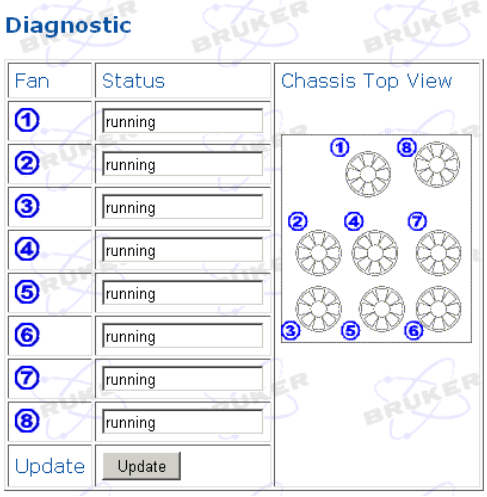
AC Power Loss 5.10

In the event of an AC power loss in the spectrometer cabinet, the chassis turns itself of and restarts automatically when the power is restored. To prevent a short time power loss an external UPS (uninterruptible power supply) must be used.

Fan Control *5.11*

The operation of all fans is individually controlled by the AQS controller and the control circuit on the AQS/2-M user bus. The fan status can be checked via the AQS chassis page in the DRU service web.

Figure 5.4. DRU Service Web: AQS Chassis Diagnostic



Safety Stop *5.12*

If the temperature inside the mainframe exceeds the absolute maximum limit of save operation, the mains supply to the chassis is switched off automatically (and without warning) to prevent permanent damage to the AQS units. This „Safety Stop“ condition is indicated with a red lamp on the front panel as long as the mains supply is present at the power connector.

! ***Make sure to establish and remove the cause of the Safety Stop condition before you use the spectrometer again.***

The Safety Stop can be caused by a fan or power supply failure within the mainframe. Other causes can be inefficient cooling air supply to the mainframe or exceeding ambient air temperatures within or around the spectrometer cabinet.

Please contact Bruker service personnel if you cannot establish the cause of the failure.

The chassis can be returned to its normal working state by switching the mains circuit breaker manually OFF and ON. An AC power loss also resets the chassis to its working state (see ***"AC Power Loss"***).

Figure 5.5. Safety Stop State Diagram

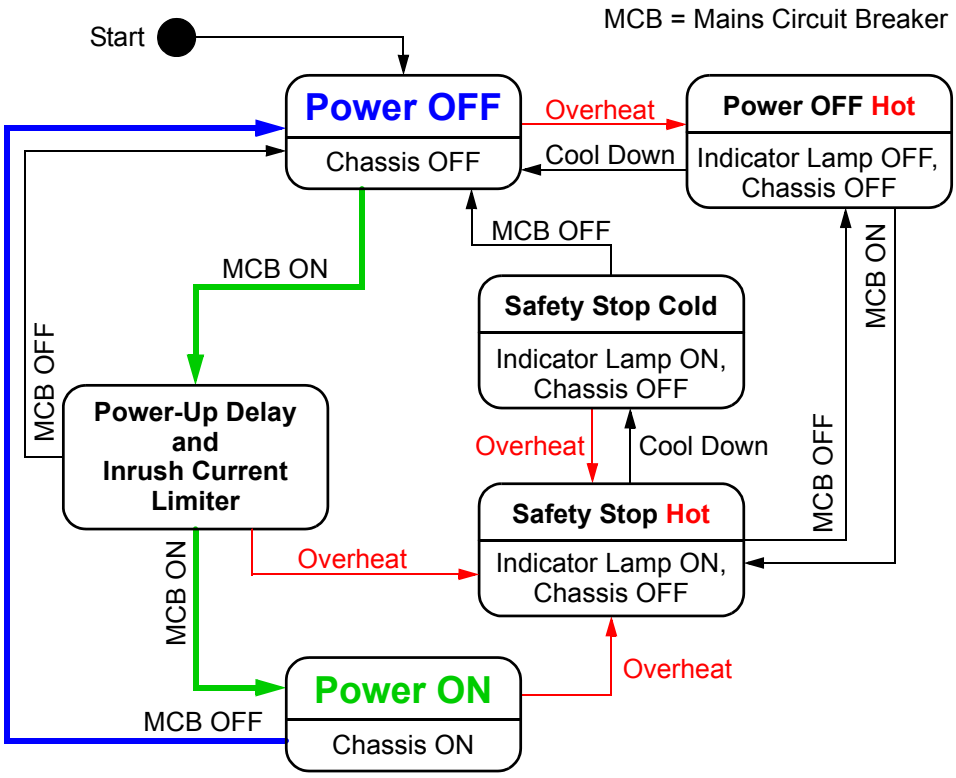


Figure 5.6. AQS/2-M AC Wiring

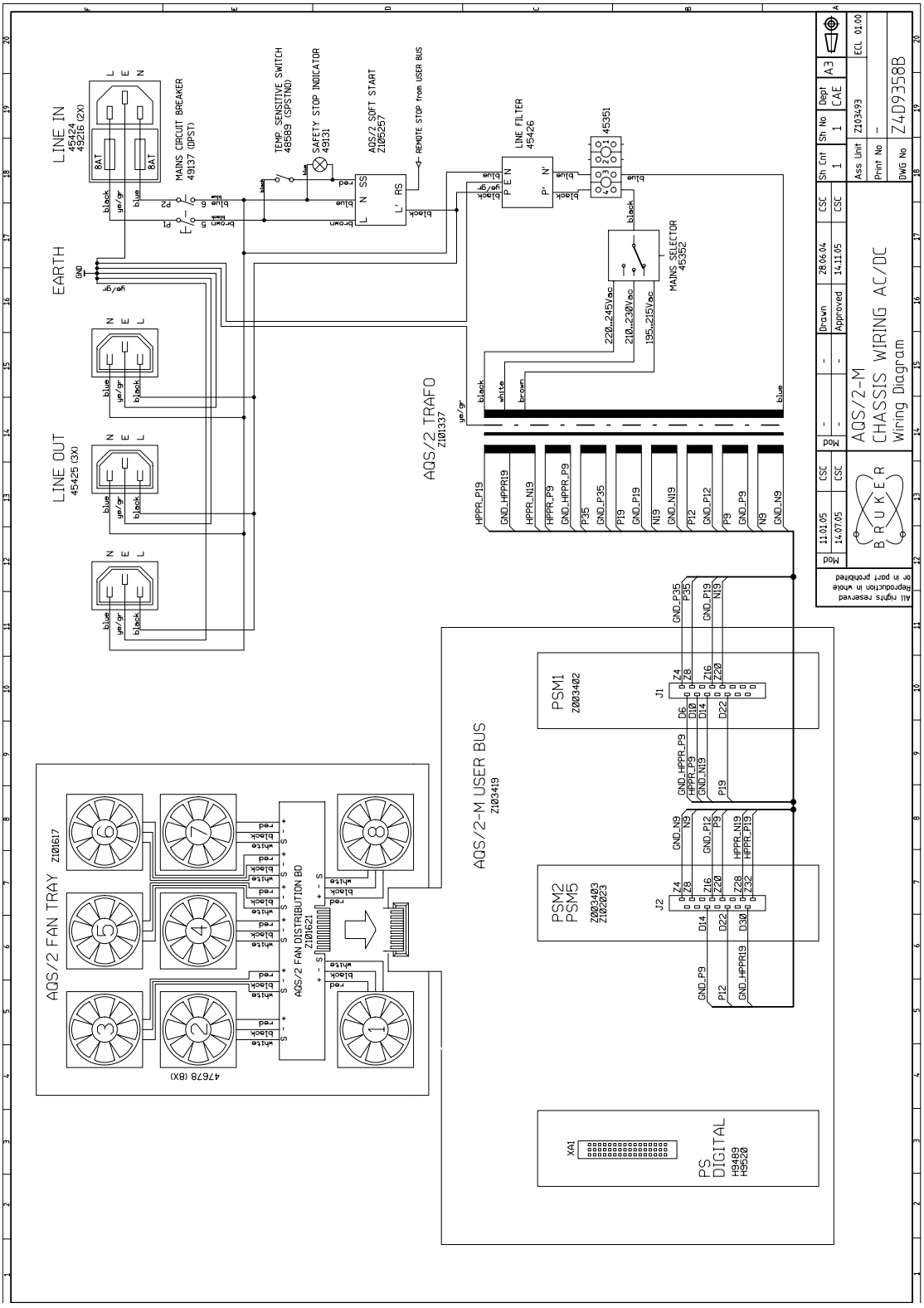
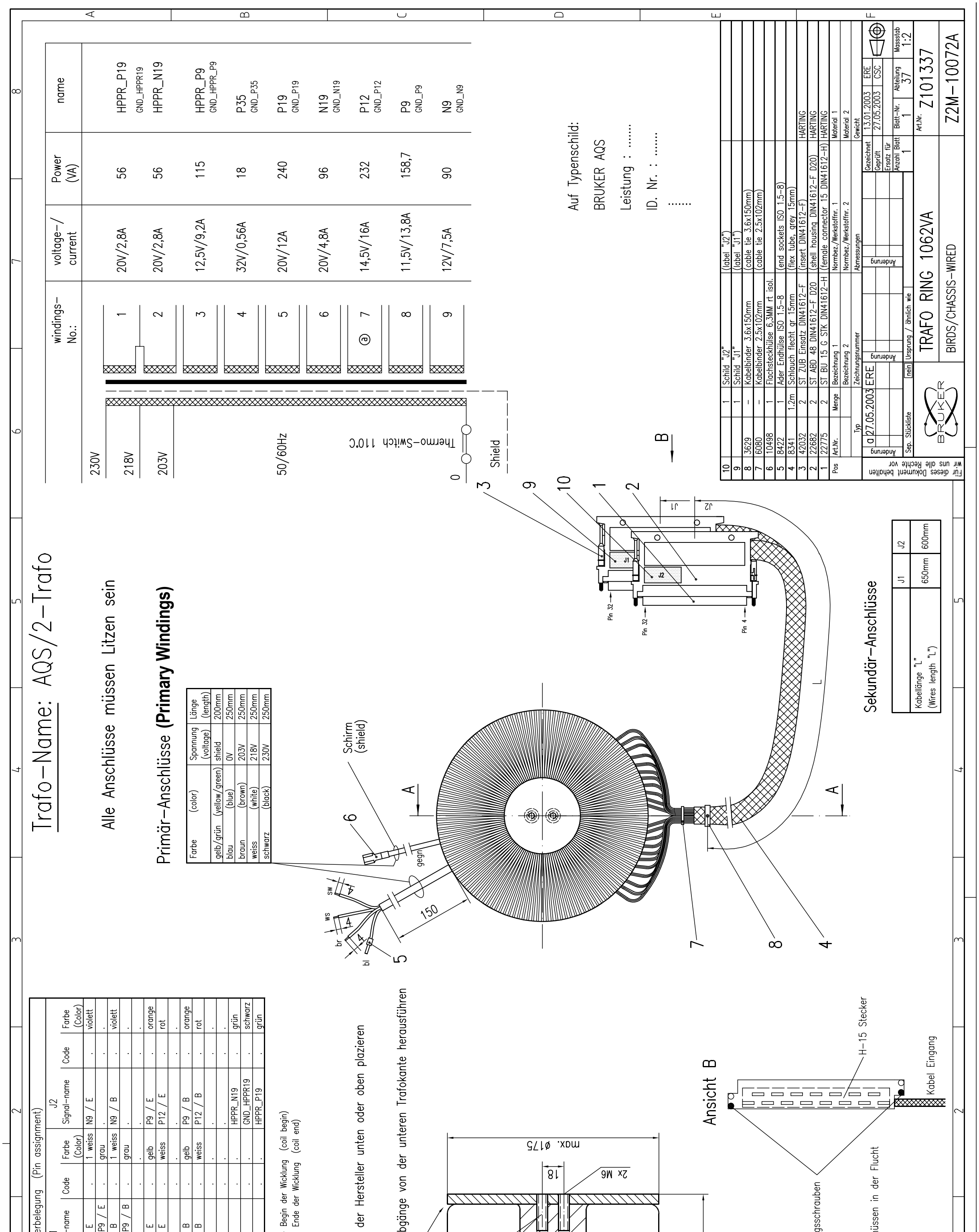


Figure 5.7. AQS/2 Transformer



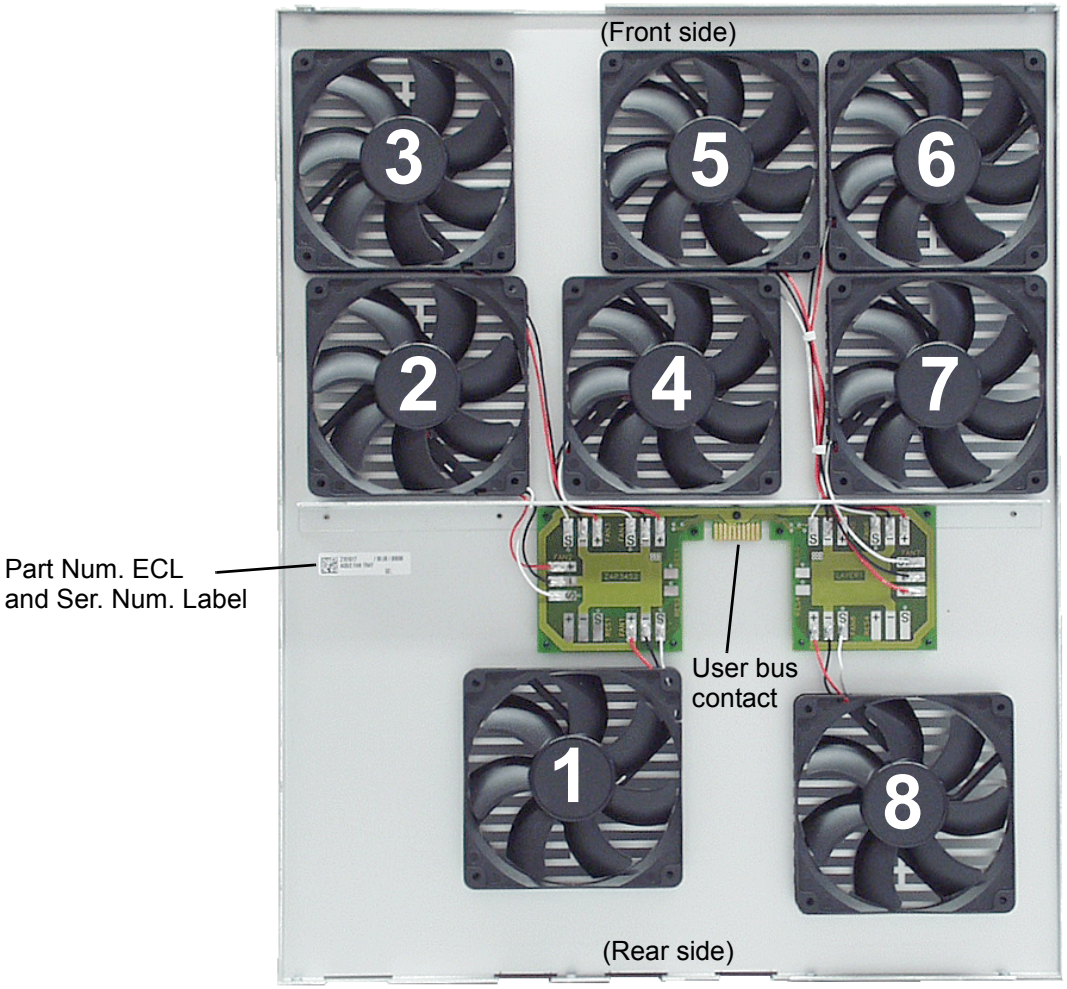
Fans *5.14*

The fans are located in the fan tray on top of the mainframe. They are supplied and controlled via the AQS/2-M user bus.

The fan tray is serviceable without removing the mainframe from the spectrometer cabinet. (see ***"Fan Tray Service Instructions" on page 103***)

! Only use AQS/2 FAN TRAY (Z101617) with ECL02 or higher as a replacement.

Figure 5.8. AQS/2 Fan Tray (Bottom view)



Fan Tray Service Instructions 5.15

! ***Only qualified Bruker personnel are allowed to service the AQS/2-M mainframe.***

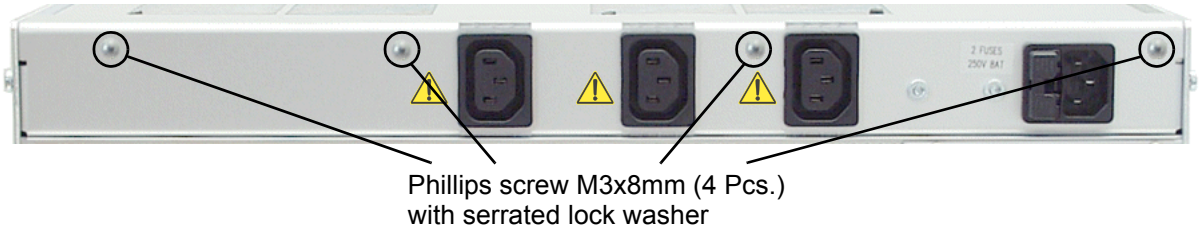
The fan tray removal and reassembly is the same as in the AQS/2 chassis. Please do not be confused if the pictures of the AQS/2 chassis are used in the following instructions.

Fan Tray removal 5.15.1

To remove the fan tray from the mainframe please follow the steps exactly as described below:

1. Turn of chassis with mains circuit breaker
2. Remove AC power line (rear side)
3. Remove 4 screws on the rear side

Figure 5.9. Fan Tray screws rear side

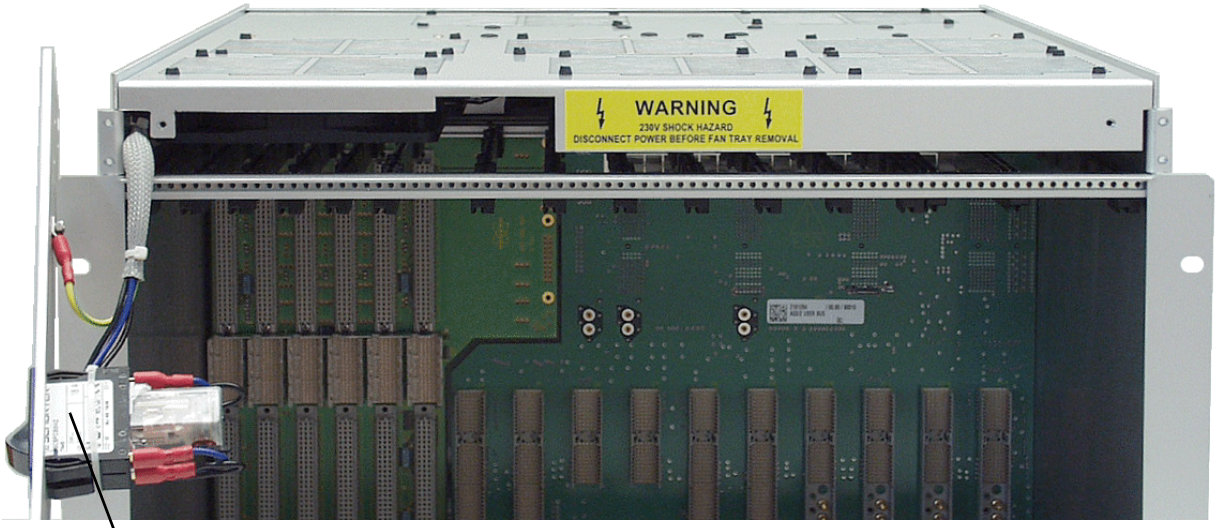


4. Remove 6 screws on the front side

Figure 5.10. Fan Tray screws front side

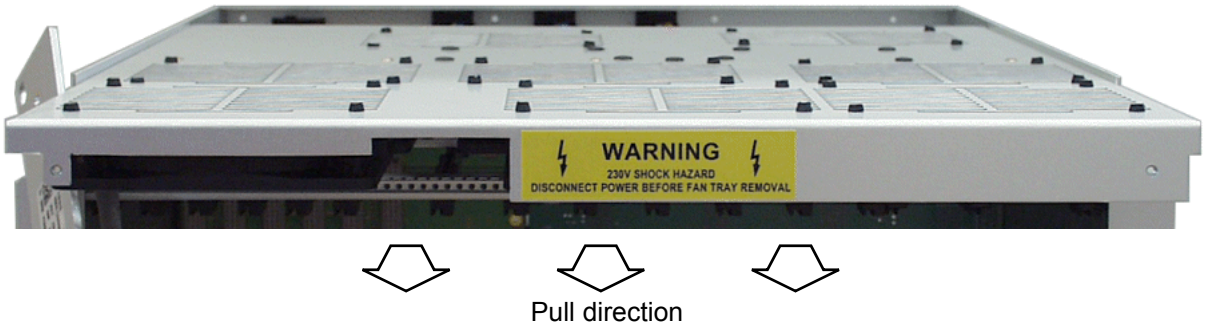
5. Carefully pull the front panel away from the mainframe and place it towards the left side (dangling from the cable)

Figure 5.11. Front panel removal



6. Remove the fan tray by pulling it gently towards the front

Figure 5.12. Fan Tray removal



Fan Tray reassembly *5.15.2*

To replace the fan tray in the AQS/2-M mainframe follow the steps as described above in ***reverse order***.

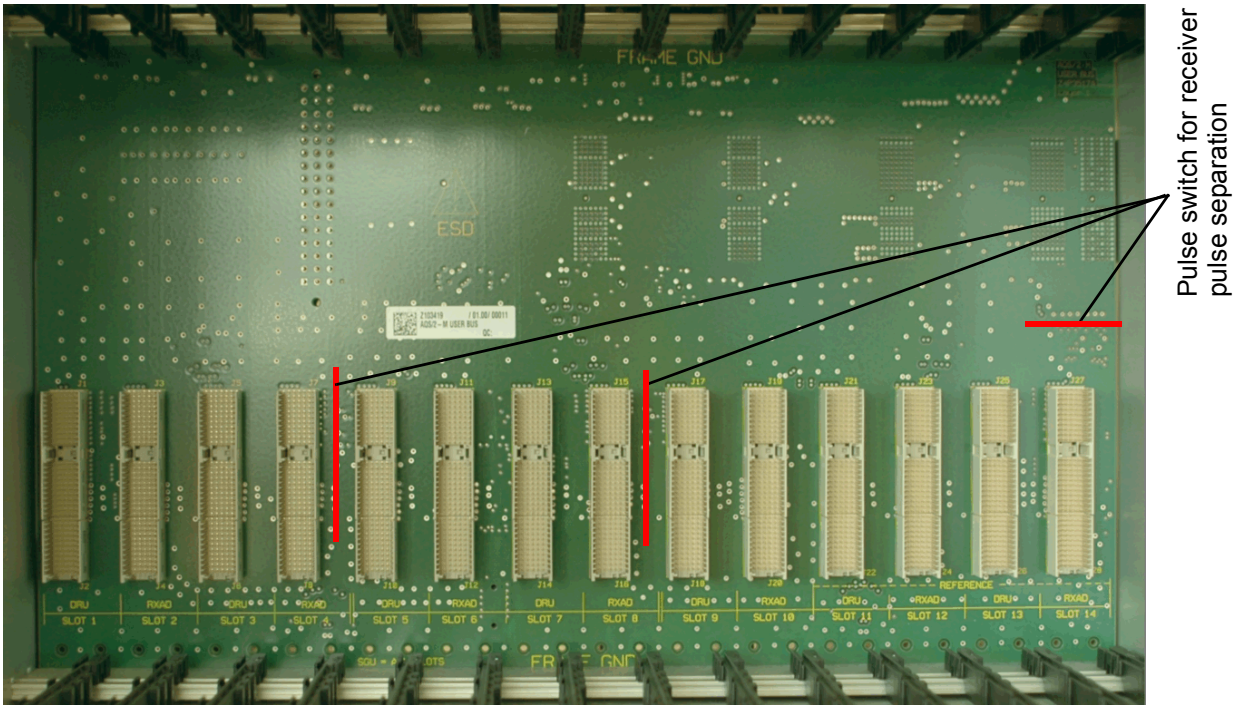
Make sure that:

- the fan tray sits flat on the guide rails on either side of the mainframe before final insertion
- no wires are squeezed in between the front panel and the fan tray
- all screws are secured and fastened properly (rear side screws with serrated lock washers)
- all fans turn freely after power up

Backplane (User Bus) 5.16

The user bus is designed to route all specific signals and power supplies to the specific boards. It represents the ground point of the AQS/2-M and is connected to the chassis frame. For detailed information about user bus signals see ***"AQS signal path" on page 13***, ***"Synchronous signals" on page 17*** and ***"20MHz Clock Distribution" on page 23***

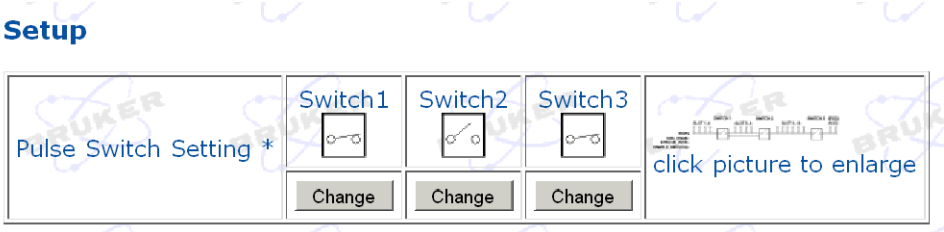
Figure 5.13. AQS/2-M User Bus (front view)



Pulse switch for receiver pulse separation 5.16.1

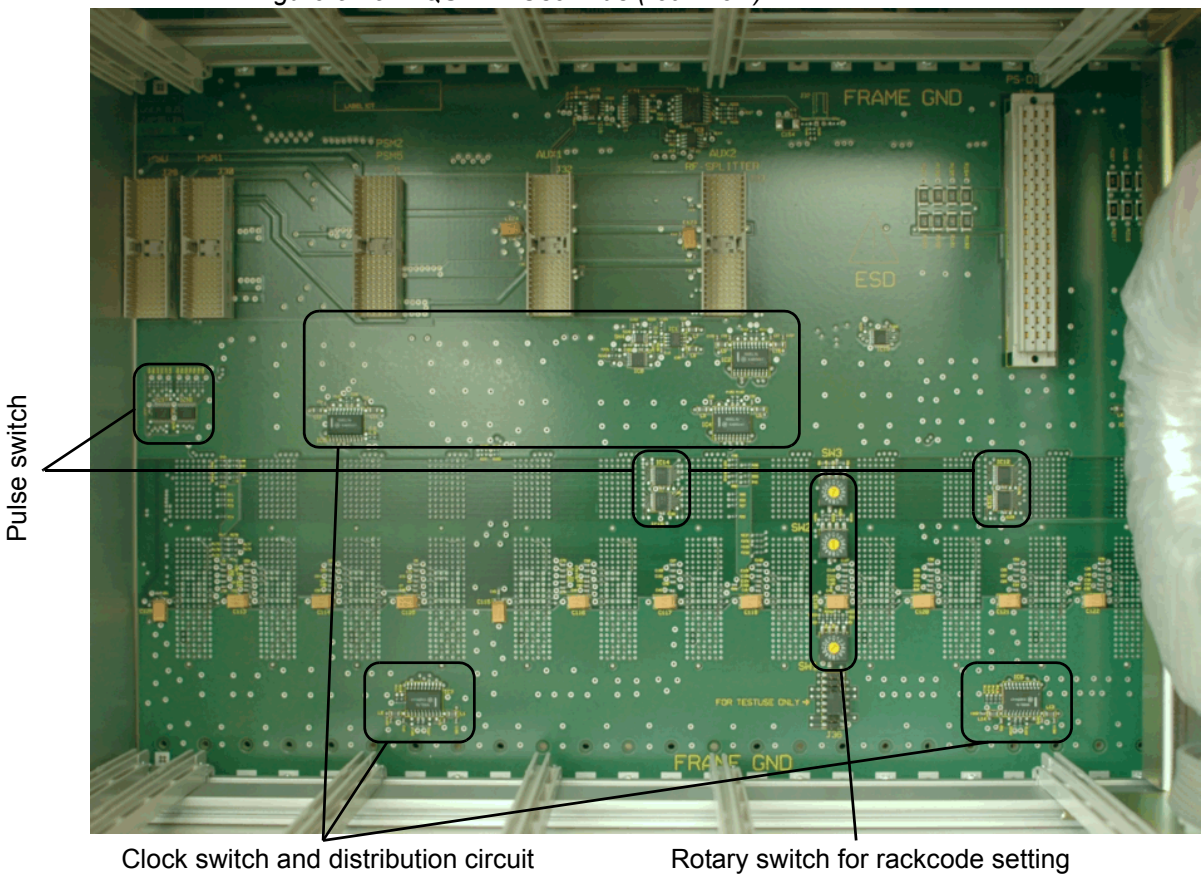
The user bus is equipped with three pulse switches. One is located between slots 4 and 5, another between slots 8 and 9 and the last between slot 14 and the PSD slot. All switches are either controlled via the AQS controller or with a rotary switch (SW2) on the rear side of the user bus. The switch status can be checked and set via the AQS chassis page in the DRU service web.

Figure 5.14. DRU Service Web: AQS Chassis Setup



For a detailed description of the SW2 switch functions see ***"Rackcode Switch Function" on page 106***.

Figure 5.15. AQS/2-M User Bus (rear view)



Rackcode Settings *5.16.2*

The rackcode must be set according to the chassis configuration as described in the configurations section of this manual.

Table 5.2. Rackcode Switch Function

Switch [a,b]	Function	Setting							
SW3	Chassis Number	**Chassis Number - 1**							
SW2	Clk Source BACK = RF-Splitter Clk Source FRONT = REF-Board	**0** 8	1 9	2 A	3 B	4 C	5 D	6 E	7 F
	Pulse Switch 1 = Slot 4 // 5 [c] Pulse Switch 2 = Slot 8 // 9 Pulse Switch 3 = Slot 14 // PSD	O O O	X O O	O X O	X X O	O O X	X O X	O X X	X X X
SW1	AQS Controller	**2** = DRU in Slot 1							

a Only chassis with ECL01 or higher have rotary switch. ECL00 uses jumpers.

b Example setting: Rackcode 0x102 = Chassis no. is 2, clock source is RF-Splitter, all pulse switches are remote controlled and the DRU in Slot 1 is AQS controller.

c O = open or remote controlled, X = permanently closed

User Bus Schematics *5.16.3*

Figure 5.16. User Bus Block Diagram

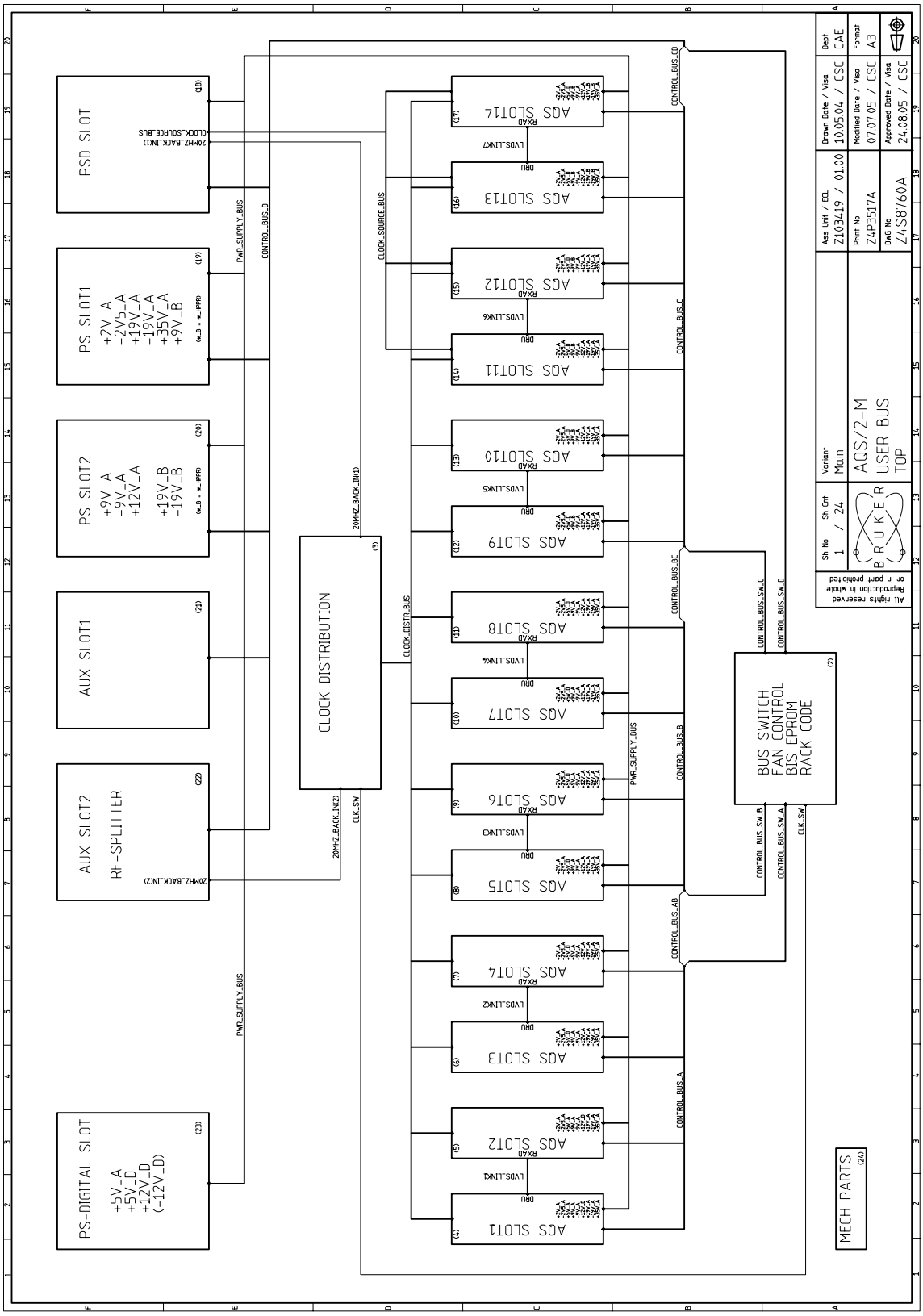


Figure 5.17. Pulse Switch, Fan Control & Rackcode

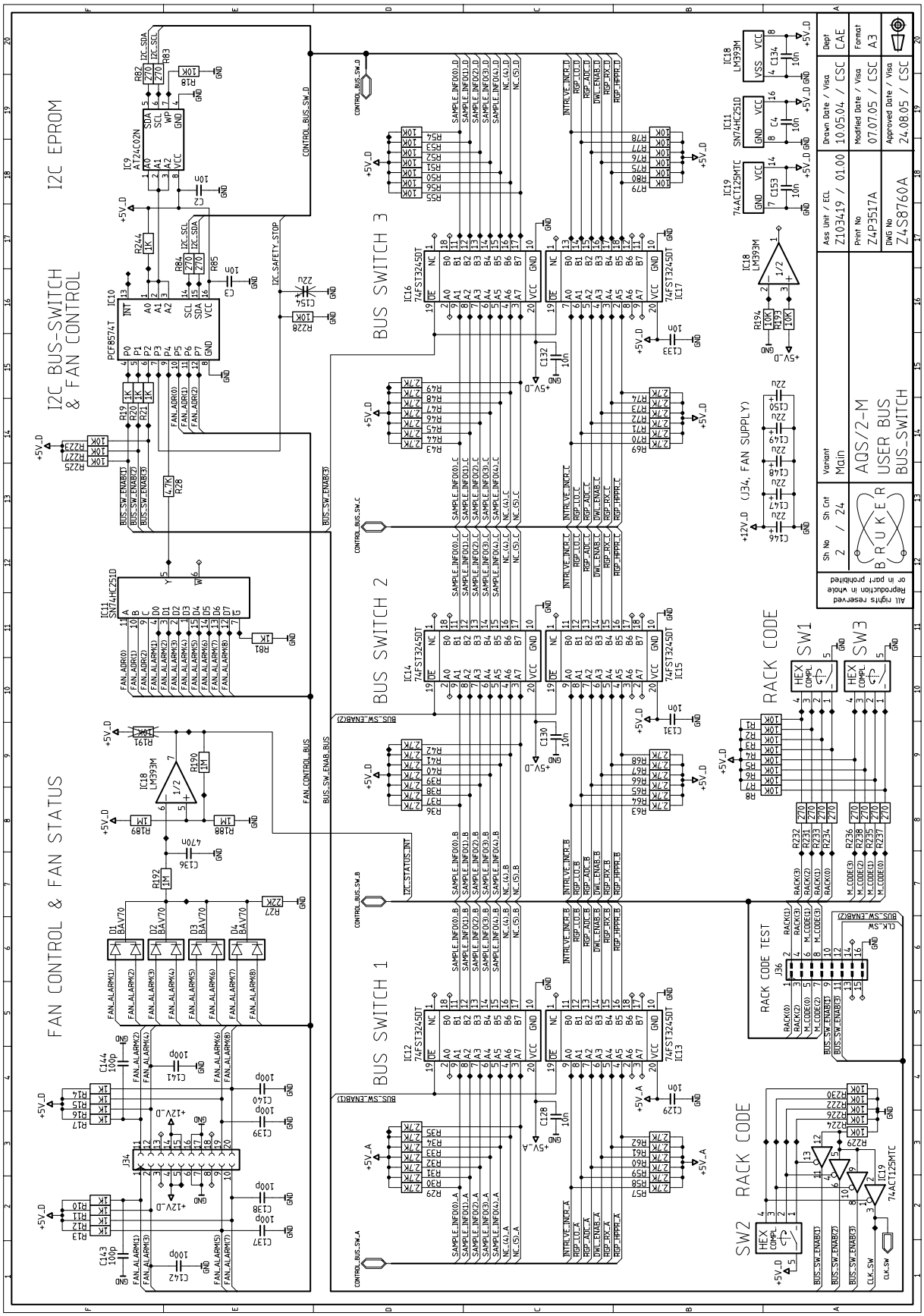


Figure 5.18. Clock Distribution

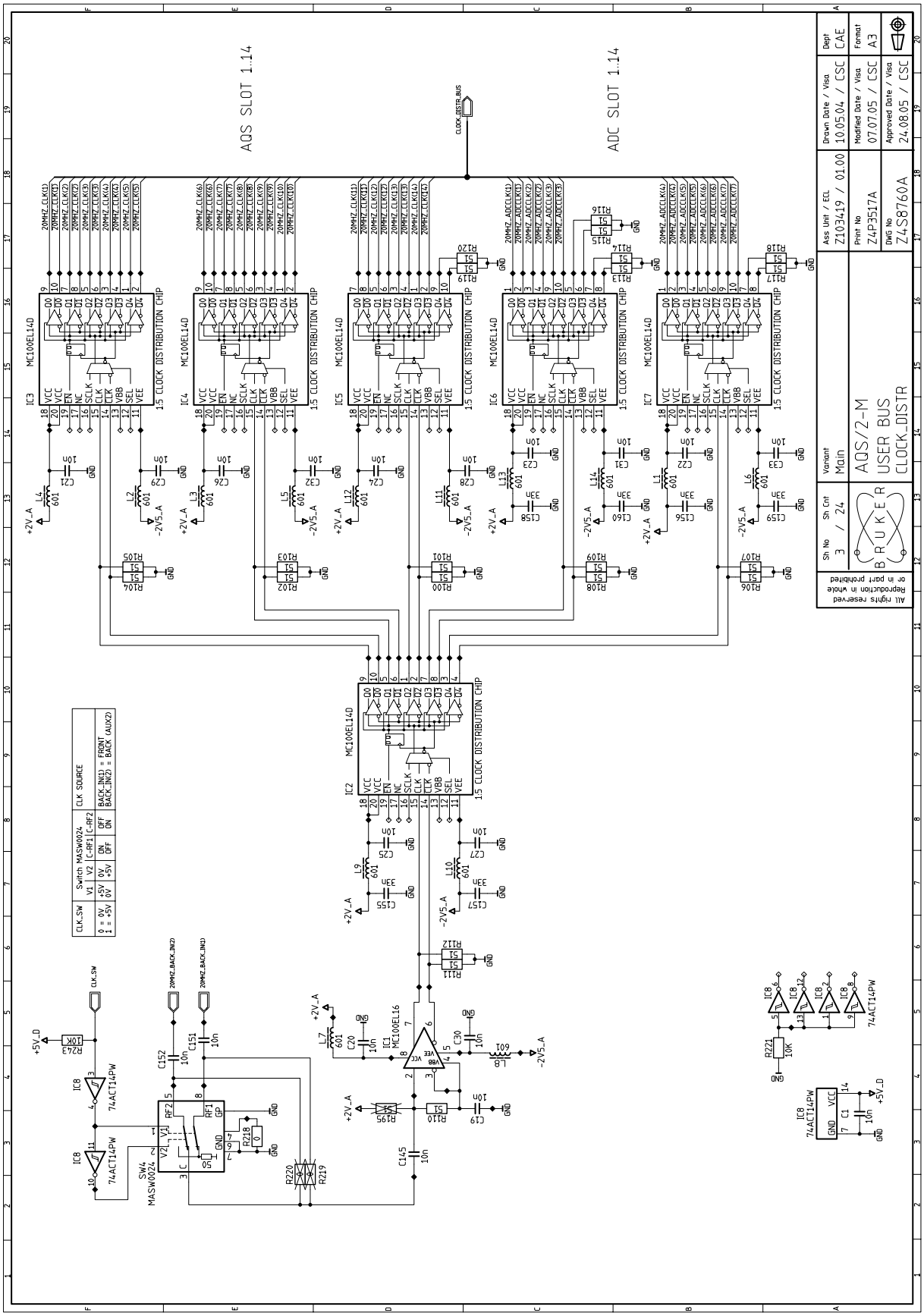


Figure 5.19. User Bus Slot 1

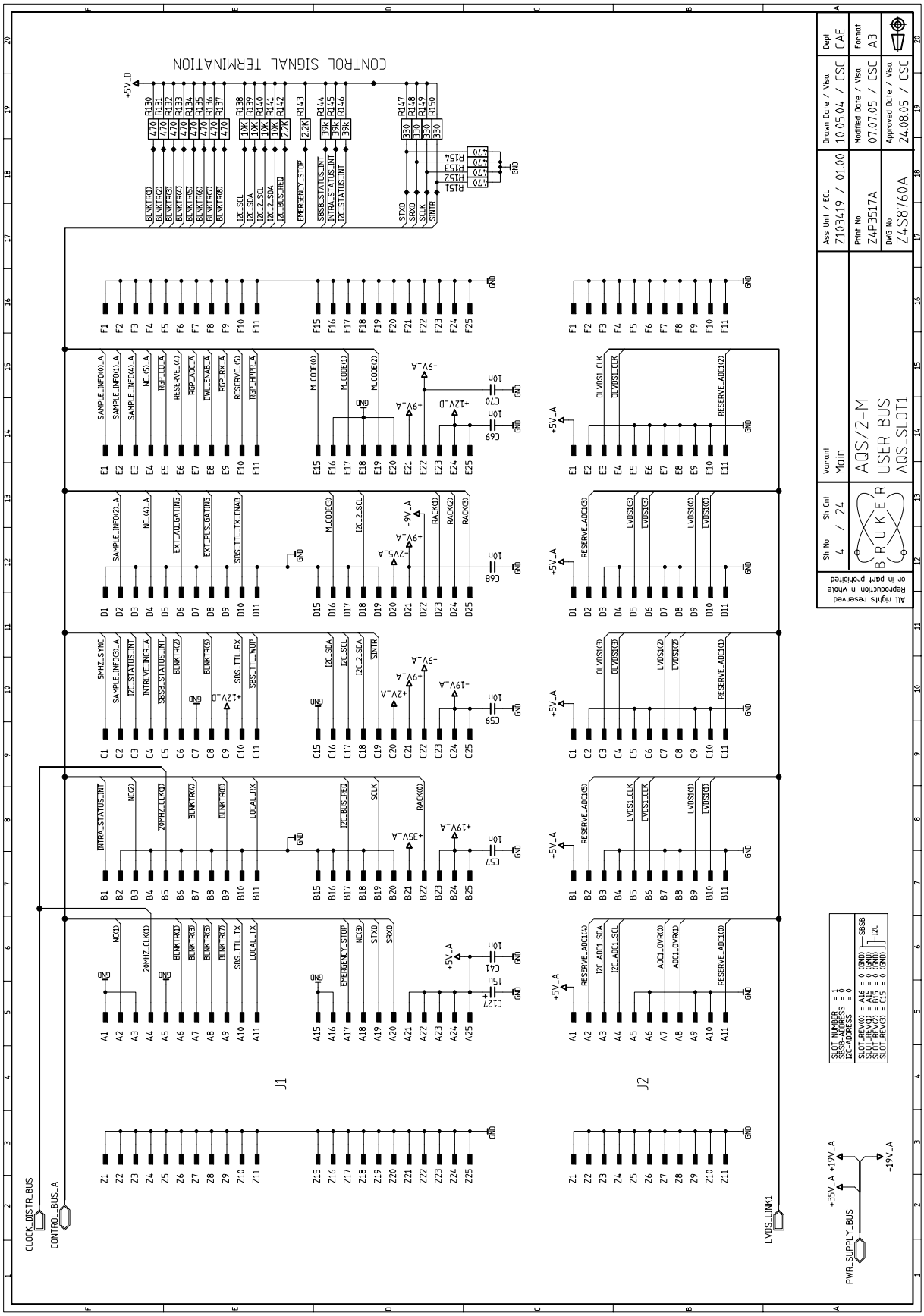


Figure 5.20. User Bus Slot 2

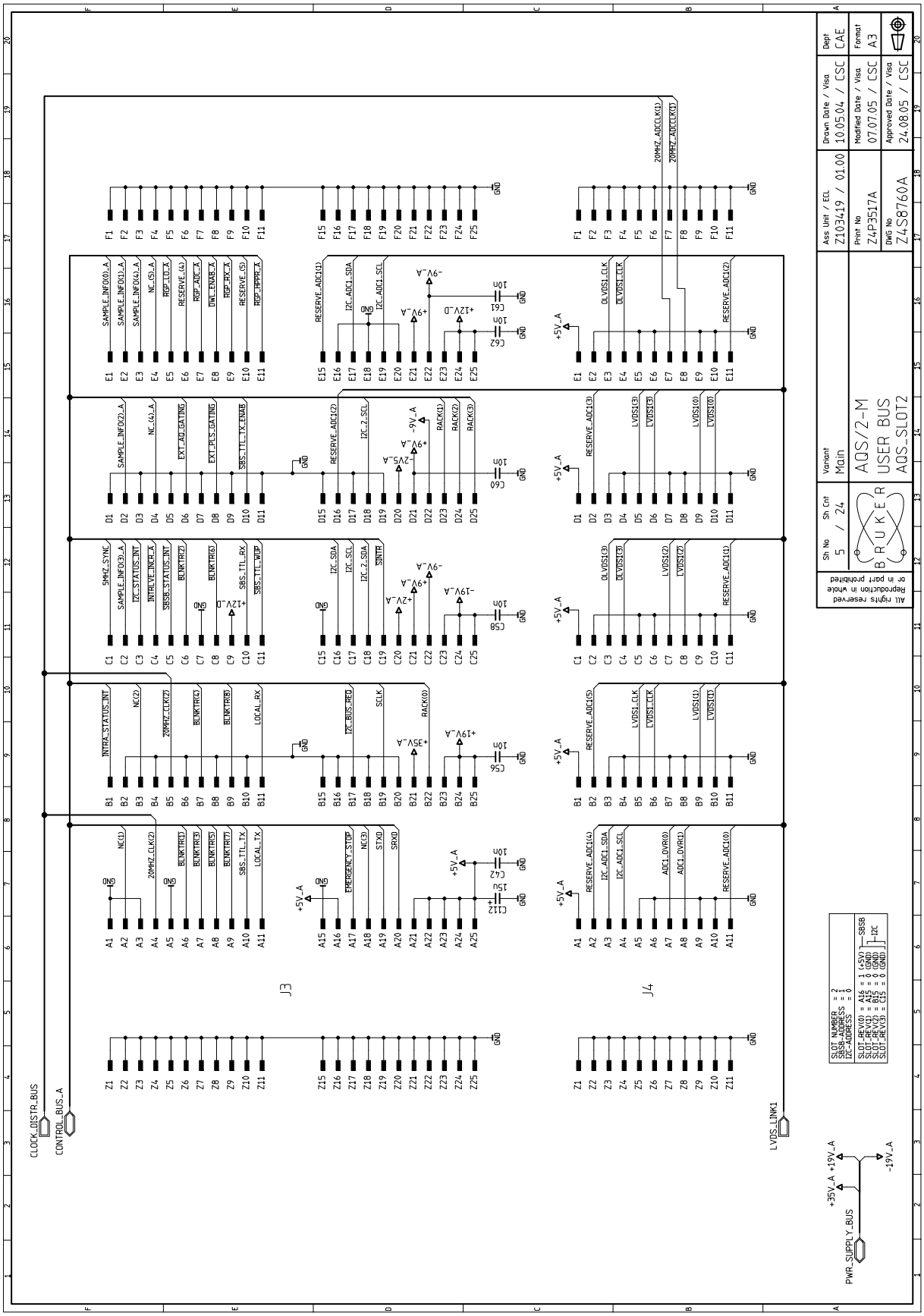


Figure 5.21. User Bus Slot 3

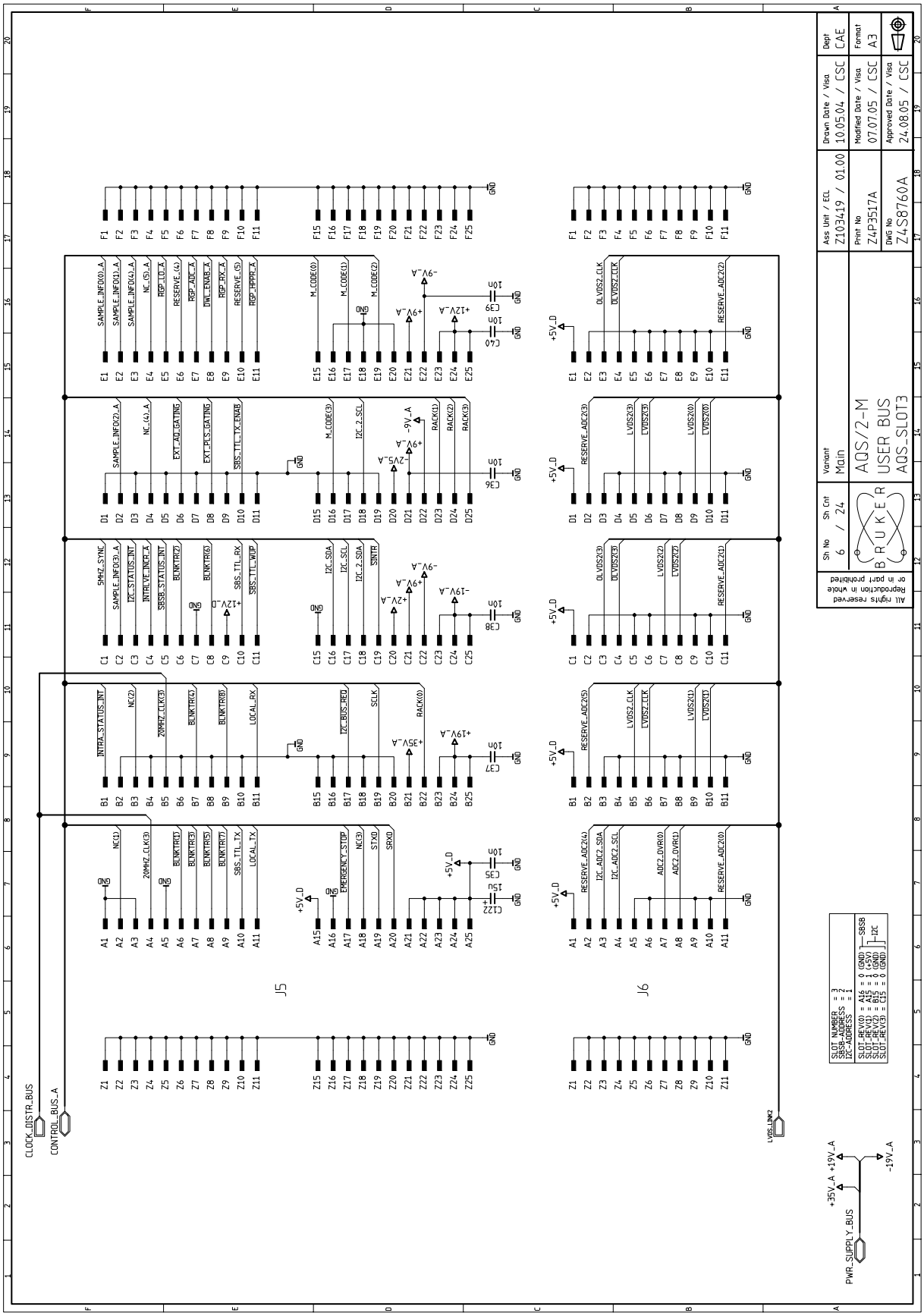


Figure 5.22. User Bus Slot 4

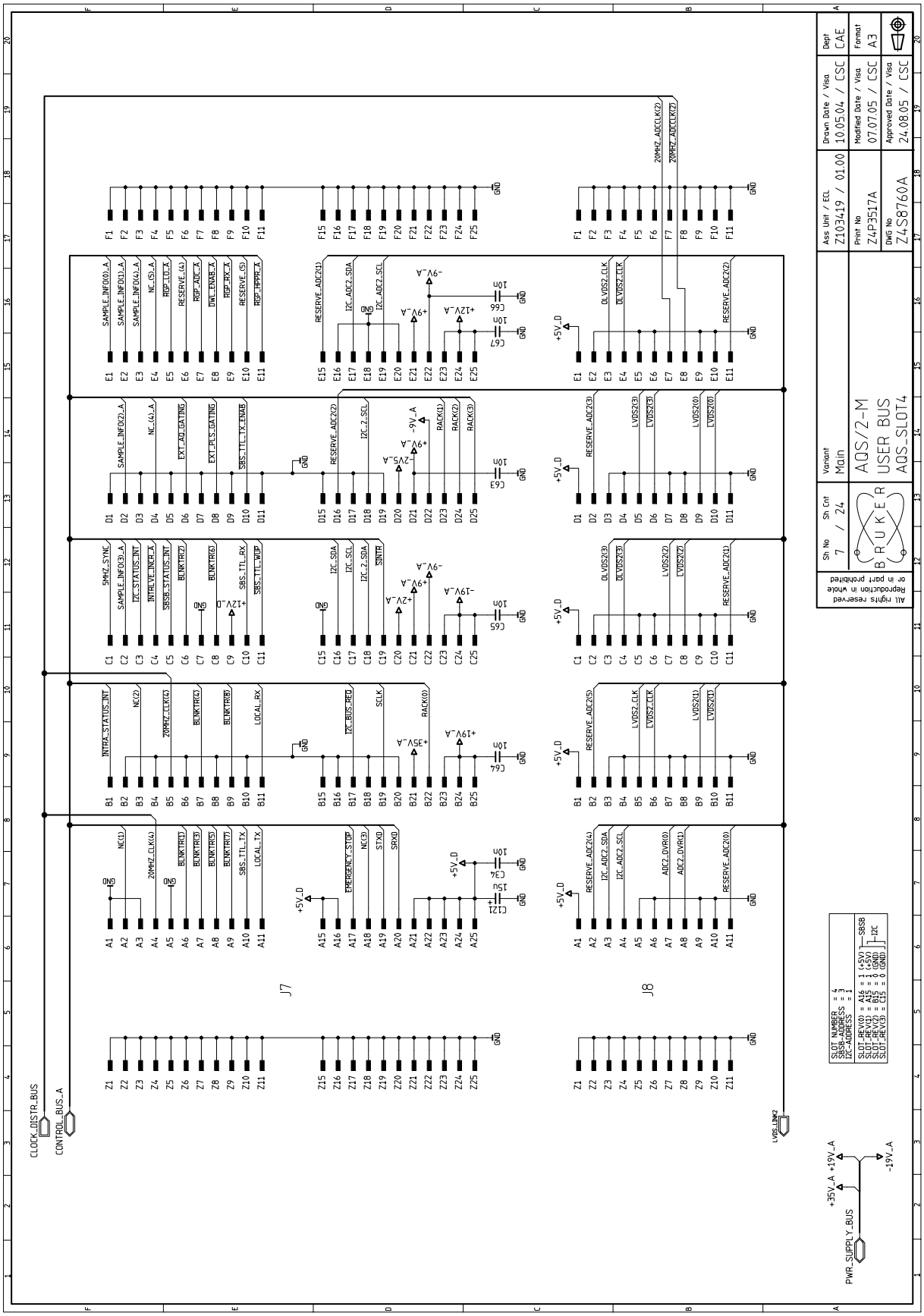


Figure 5.23. User Bus Slot 5

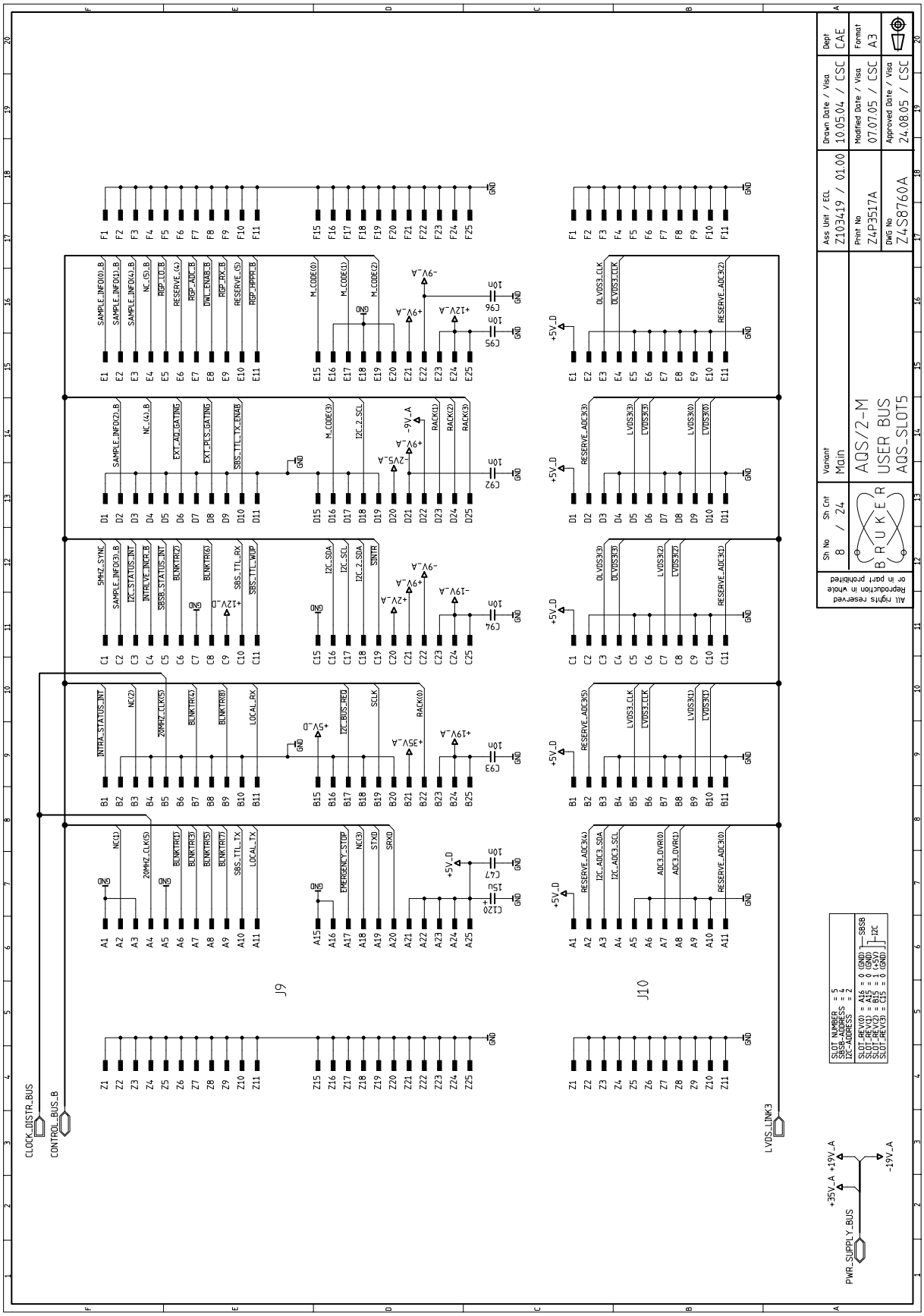


Figure 5.24. User Bus Slot 6

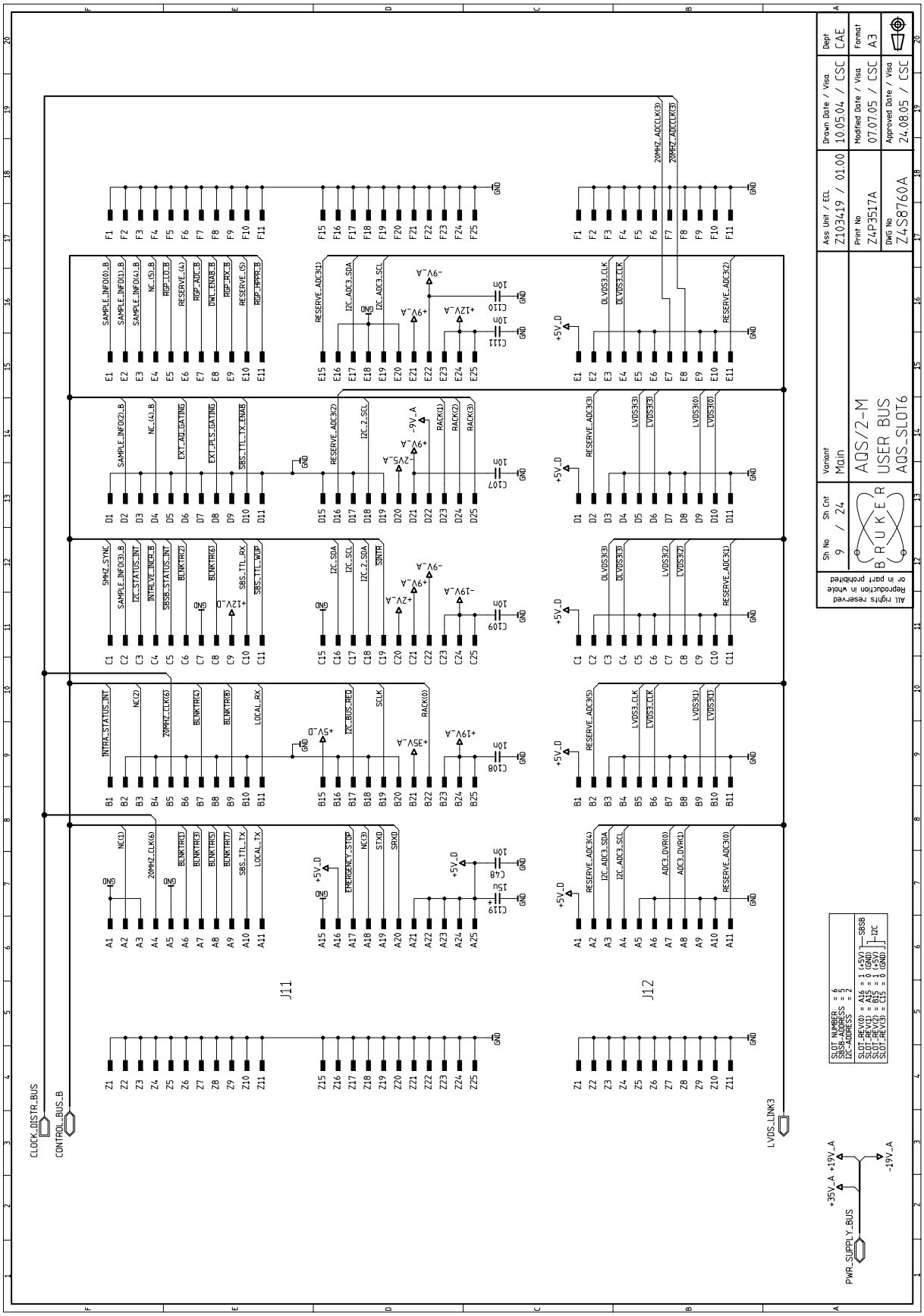


Figure 5.25. User Bus Slot 7

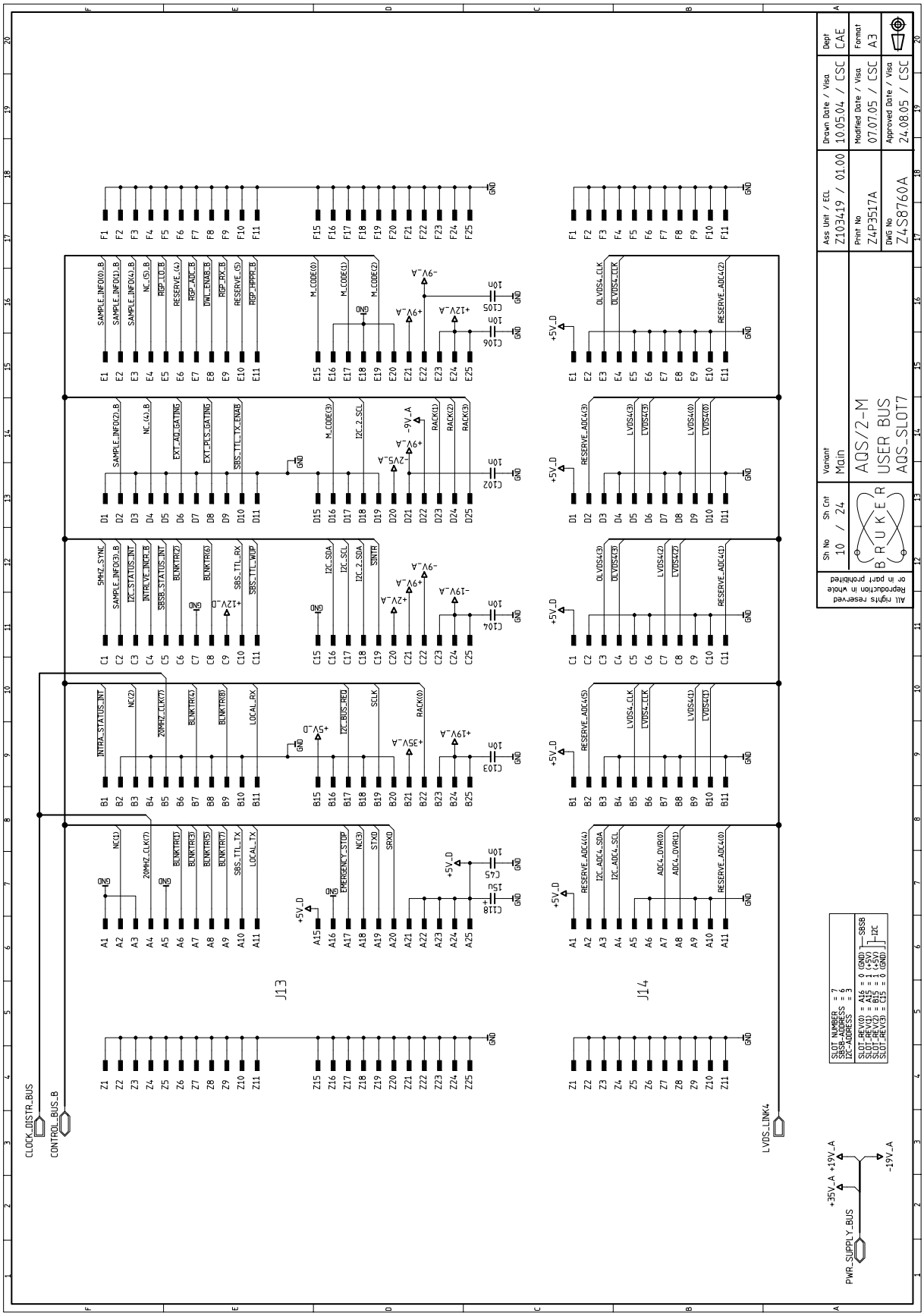


Figure 5.26. User Bus Slot 8

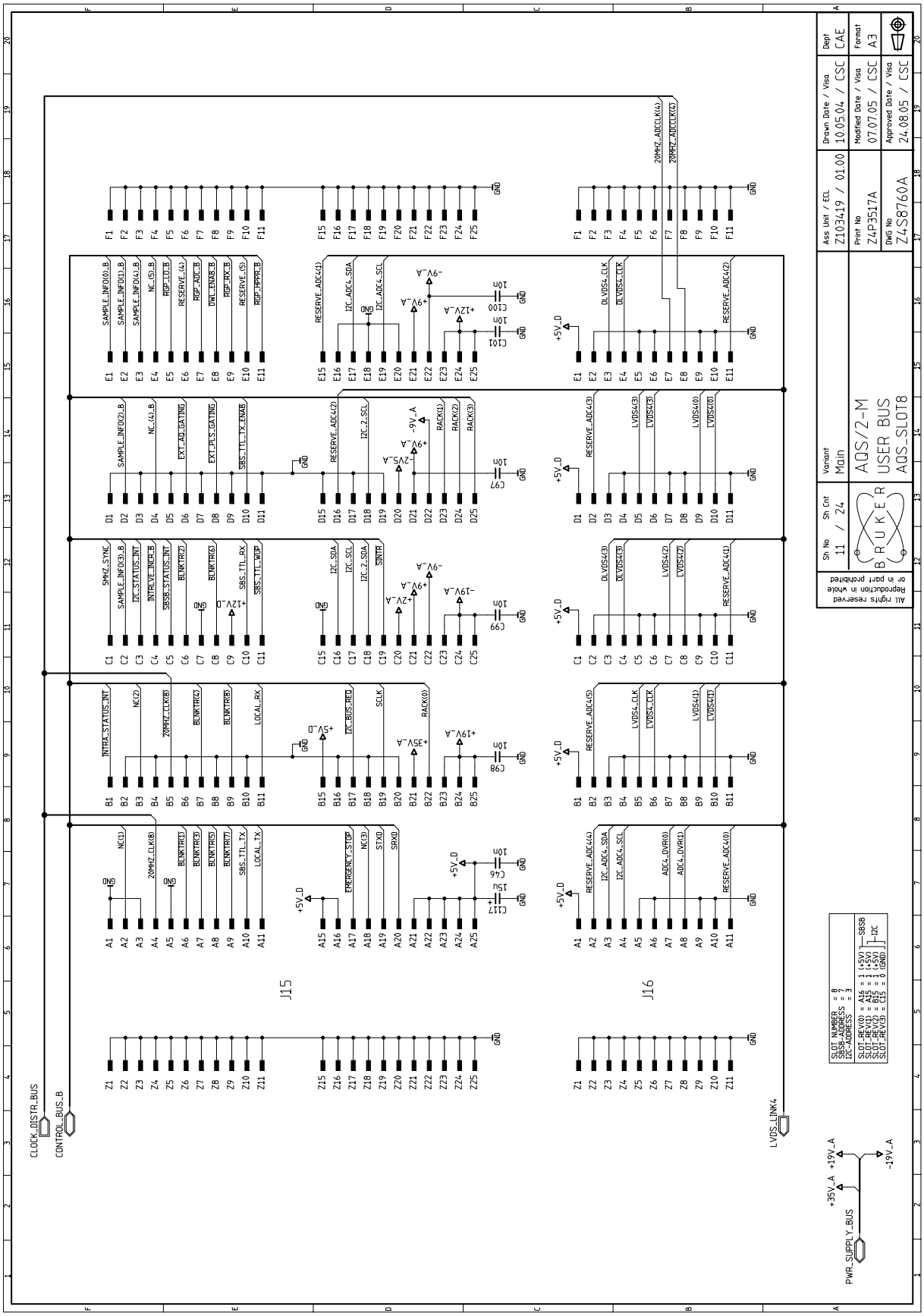


Figure 5.27. User Bus Slot 9

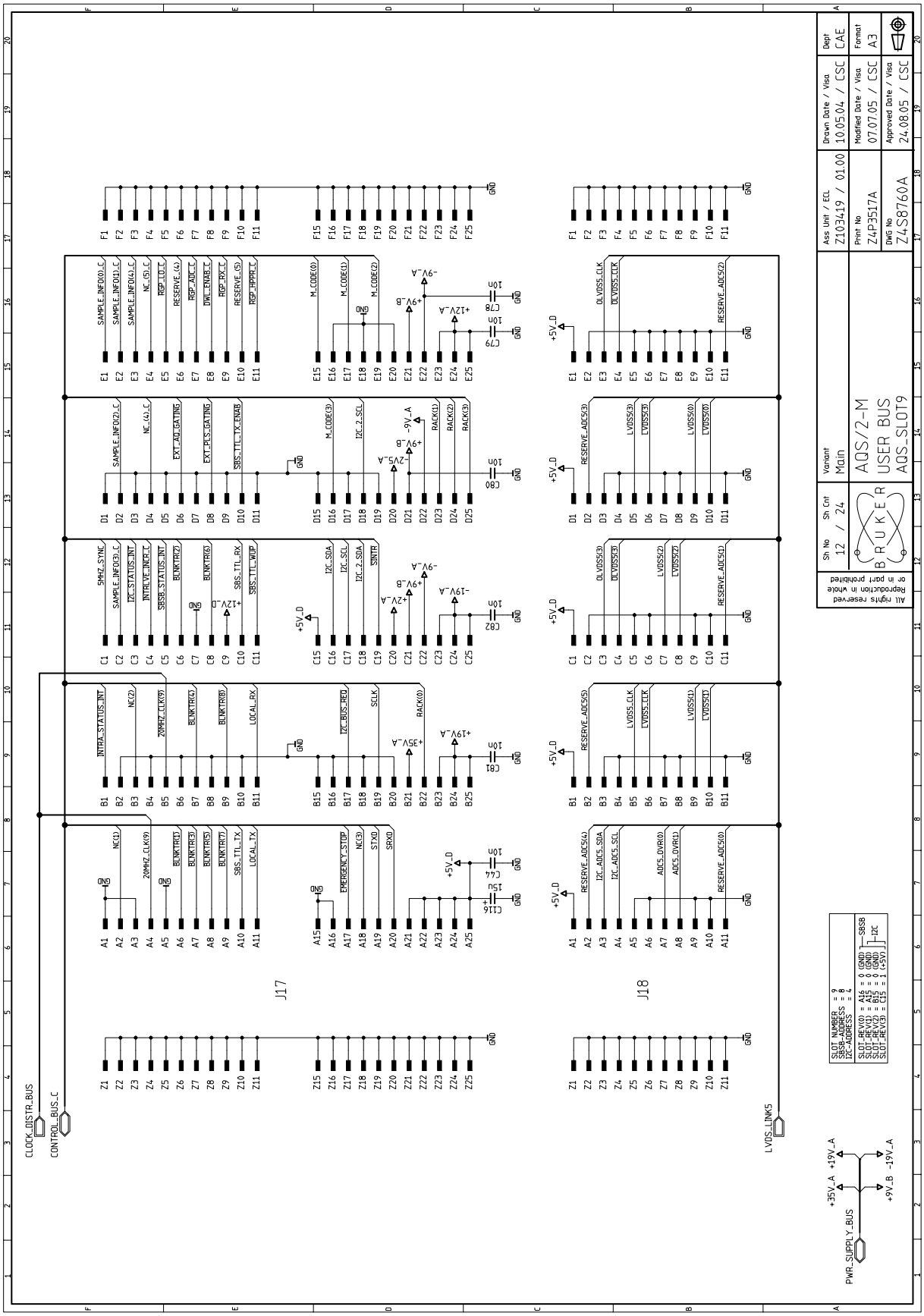


Figure 5.28. User Bus Slot 10

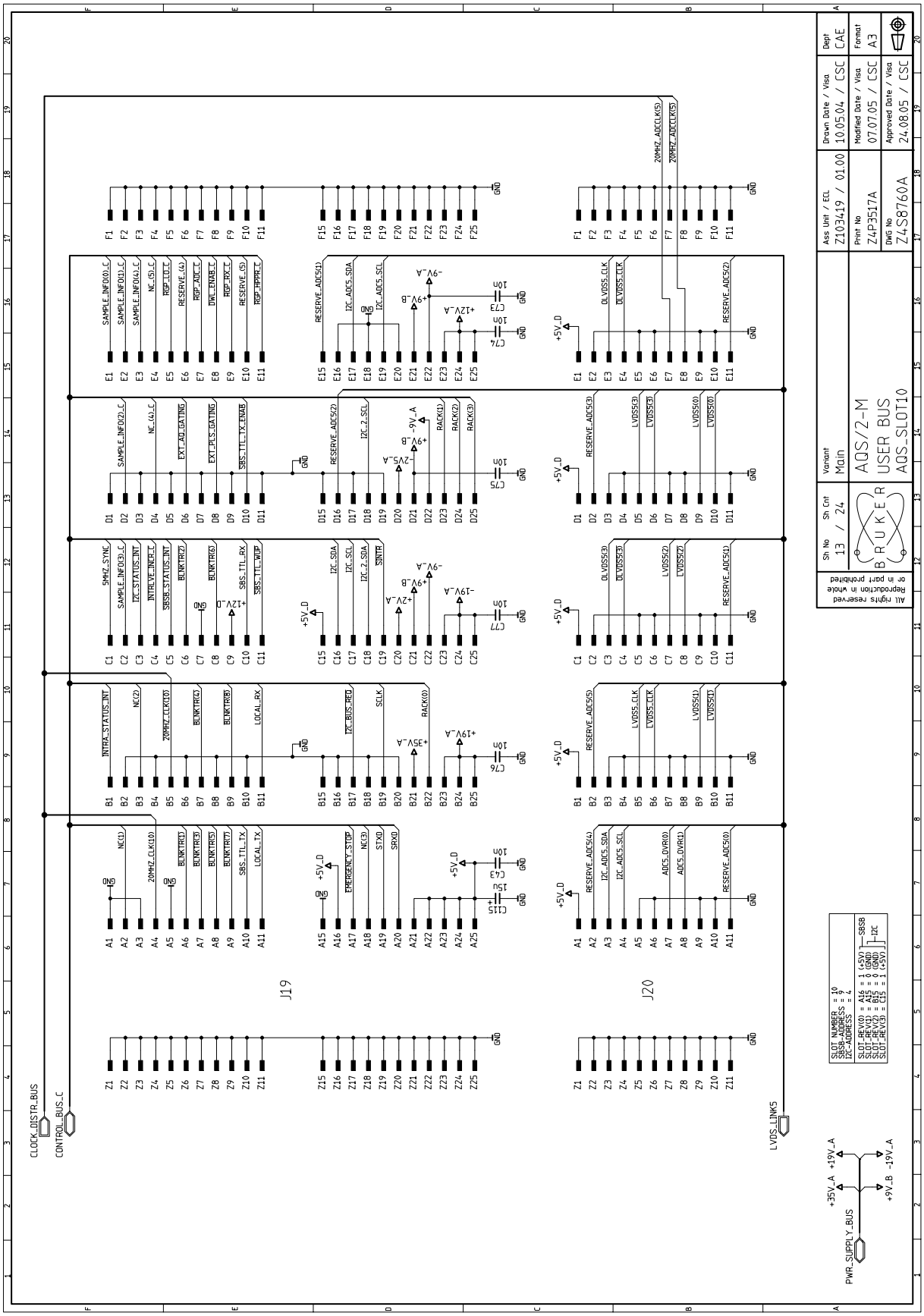


Figure 5.29. User Bus Slot 11

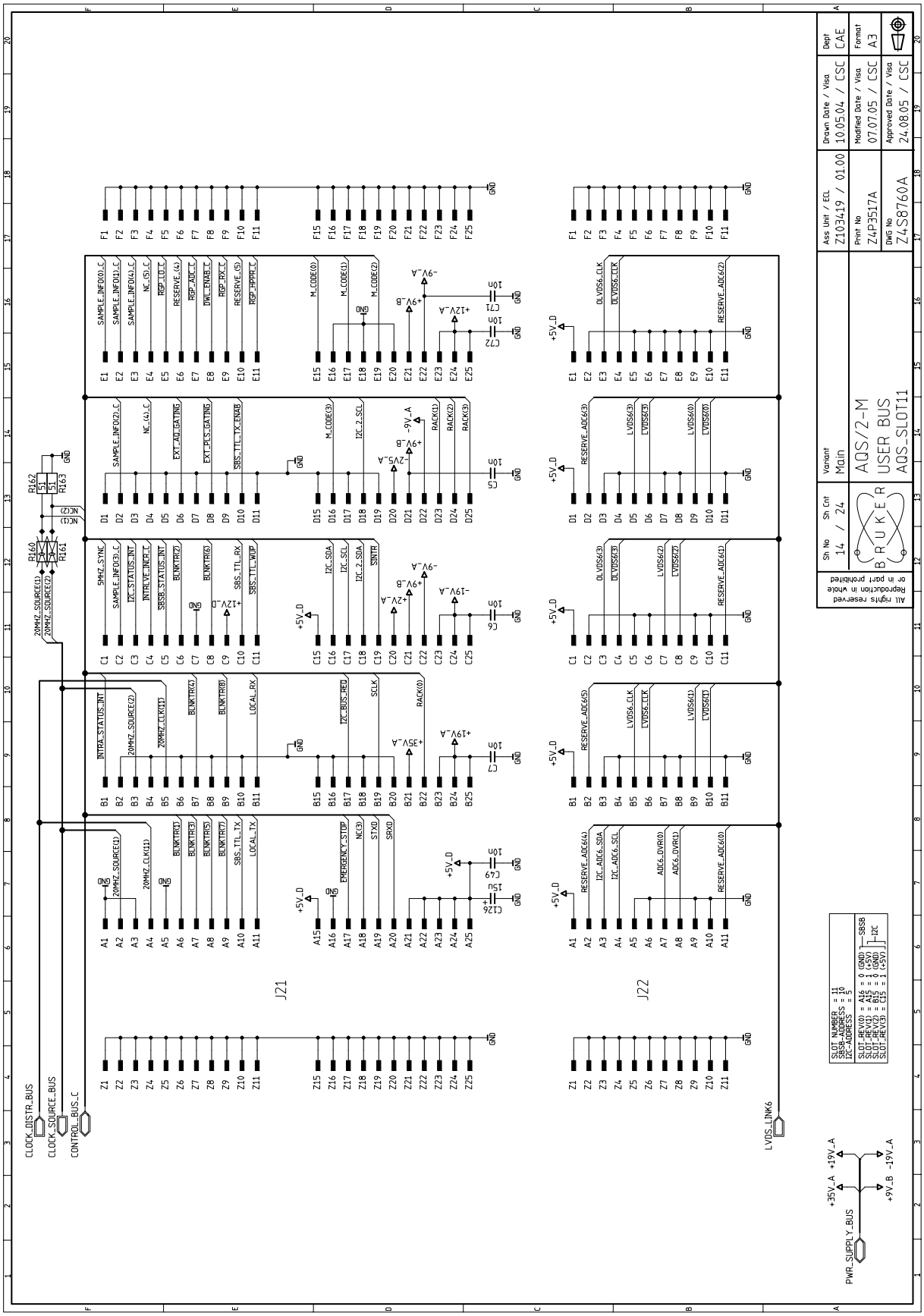


Figure 5.30. User Bus Slot 12

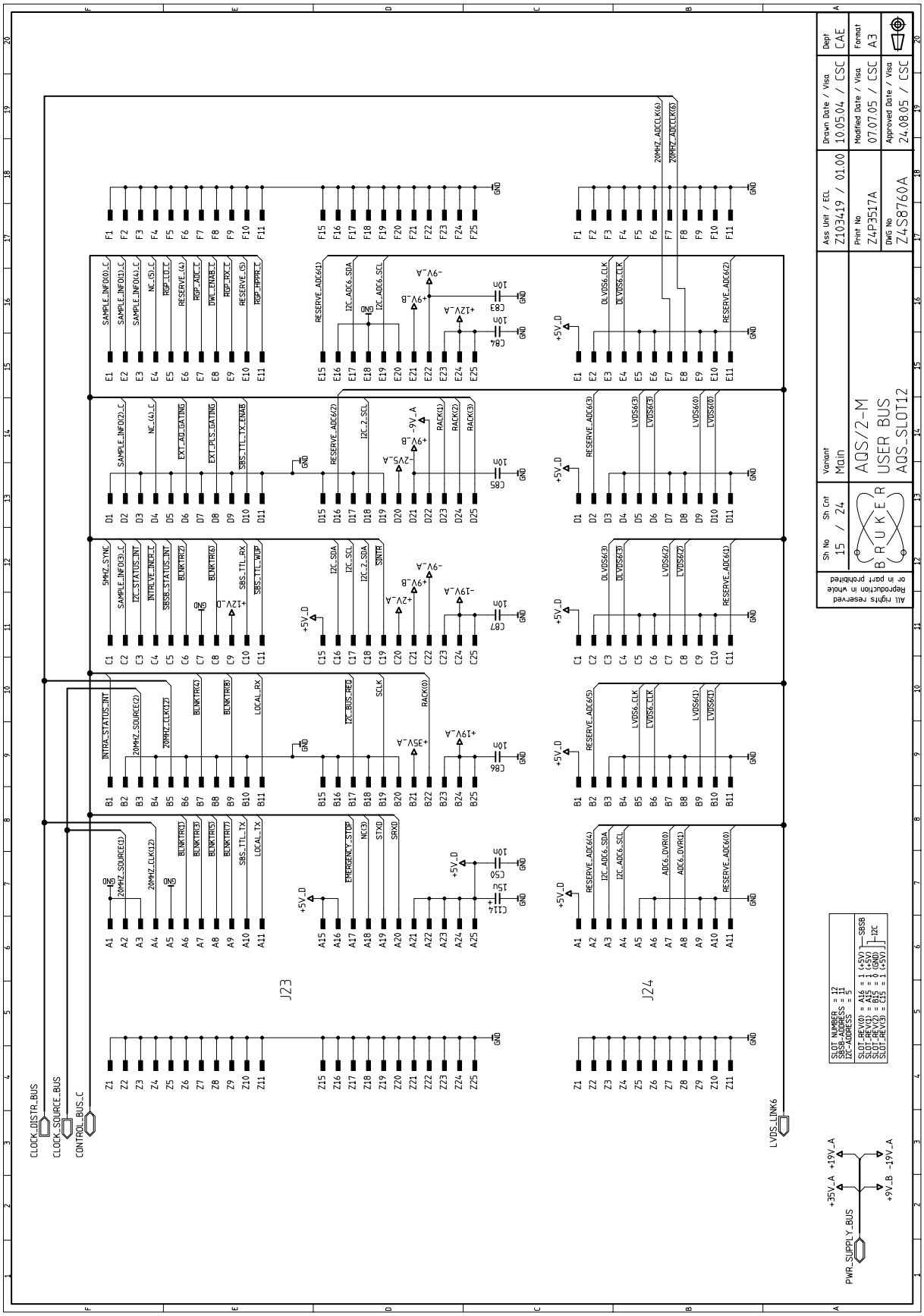


Figure 5.31. User Bus Slot 13

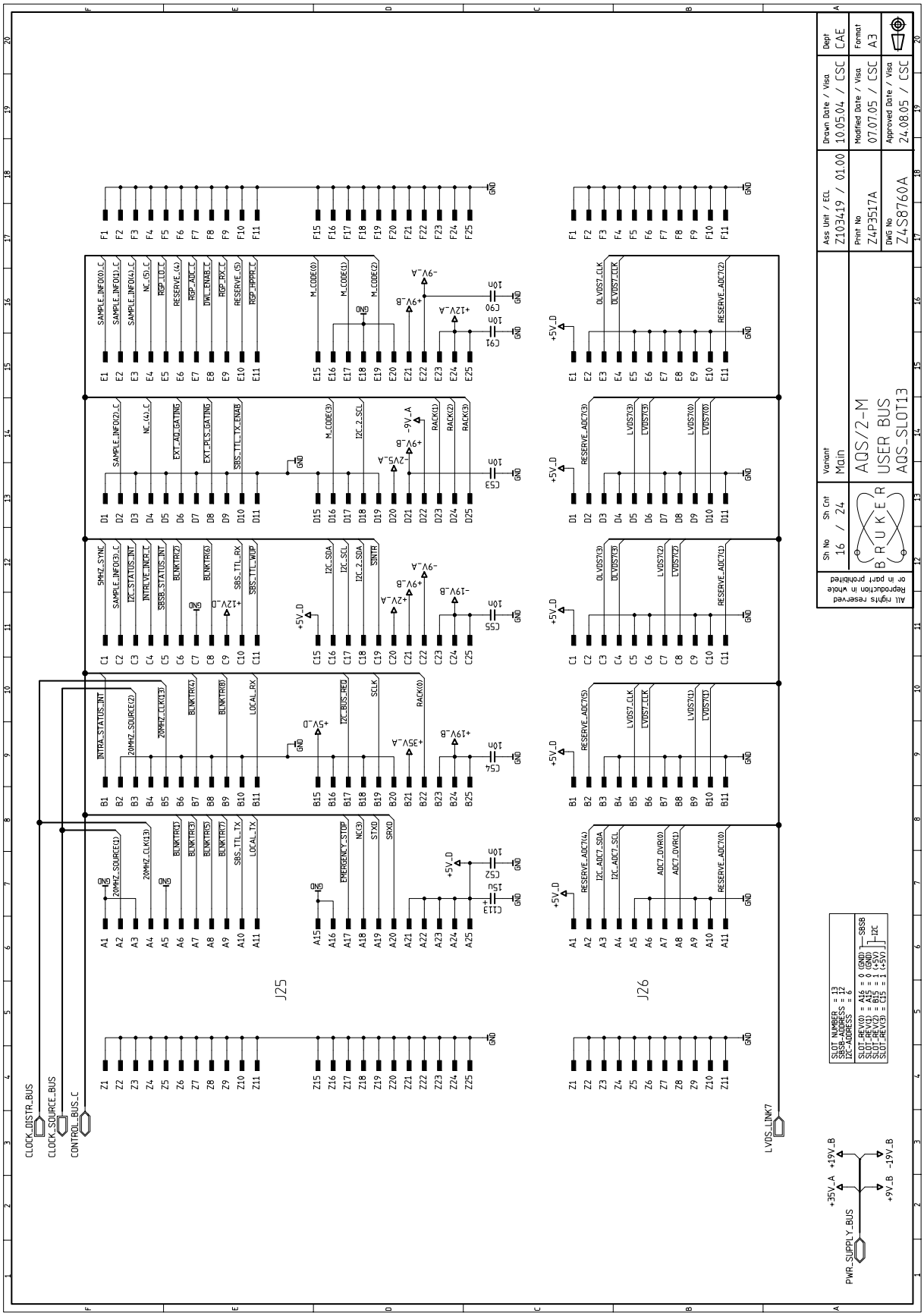


Figure 5.32. User Bus Slot 14

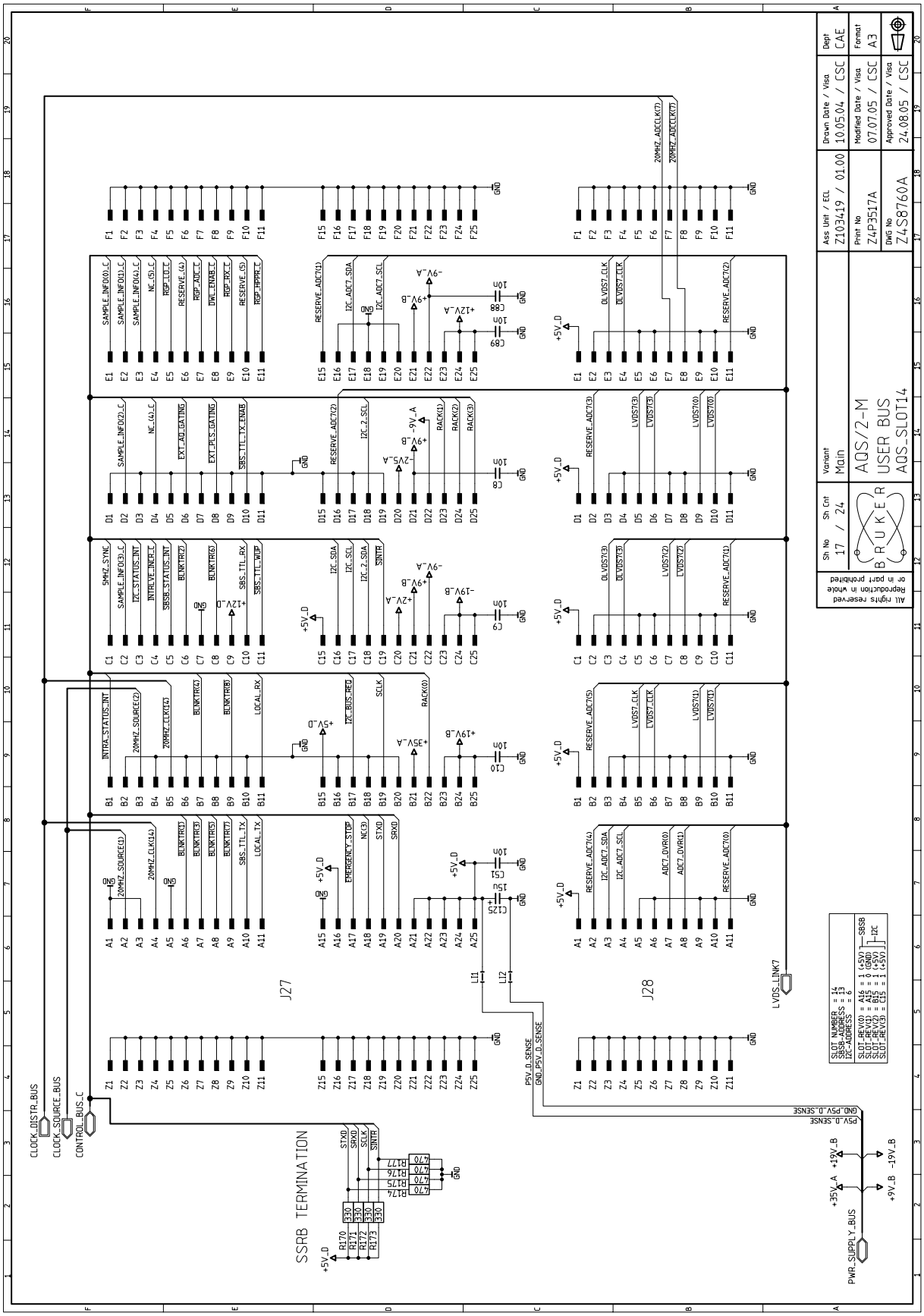


Figure 5.33. PSD Slot

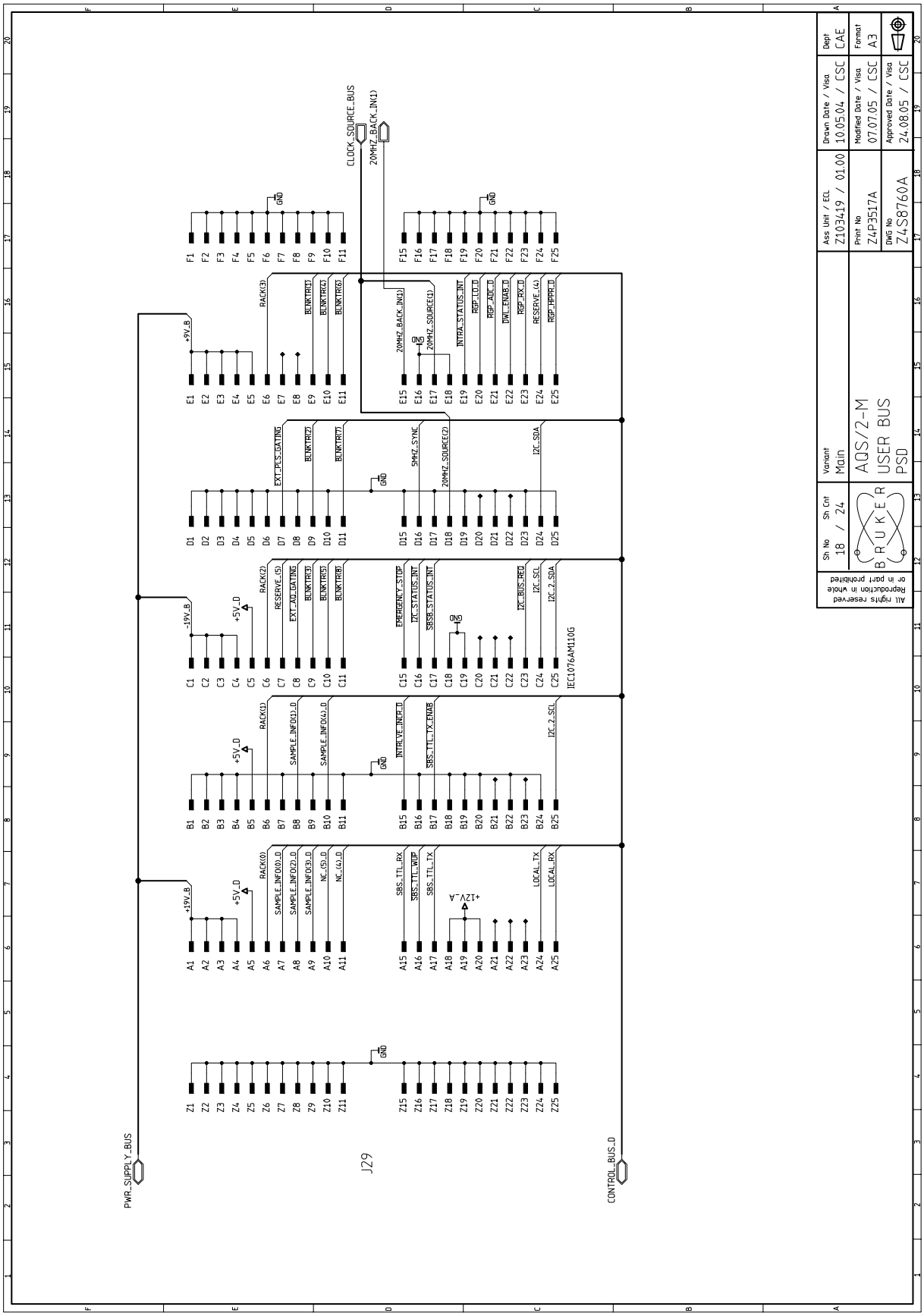


Figure 5.34. Power Supply Slot 1

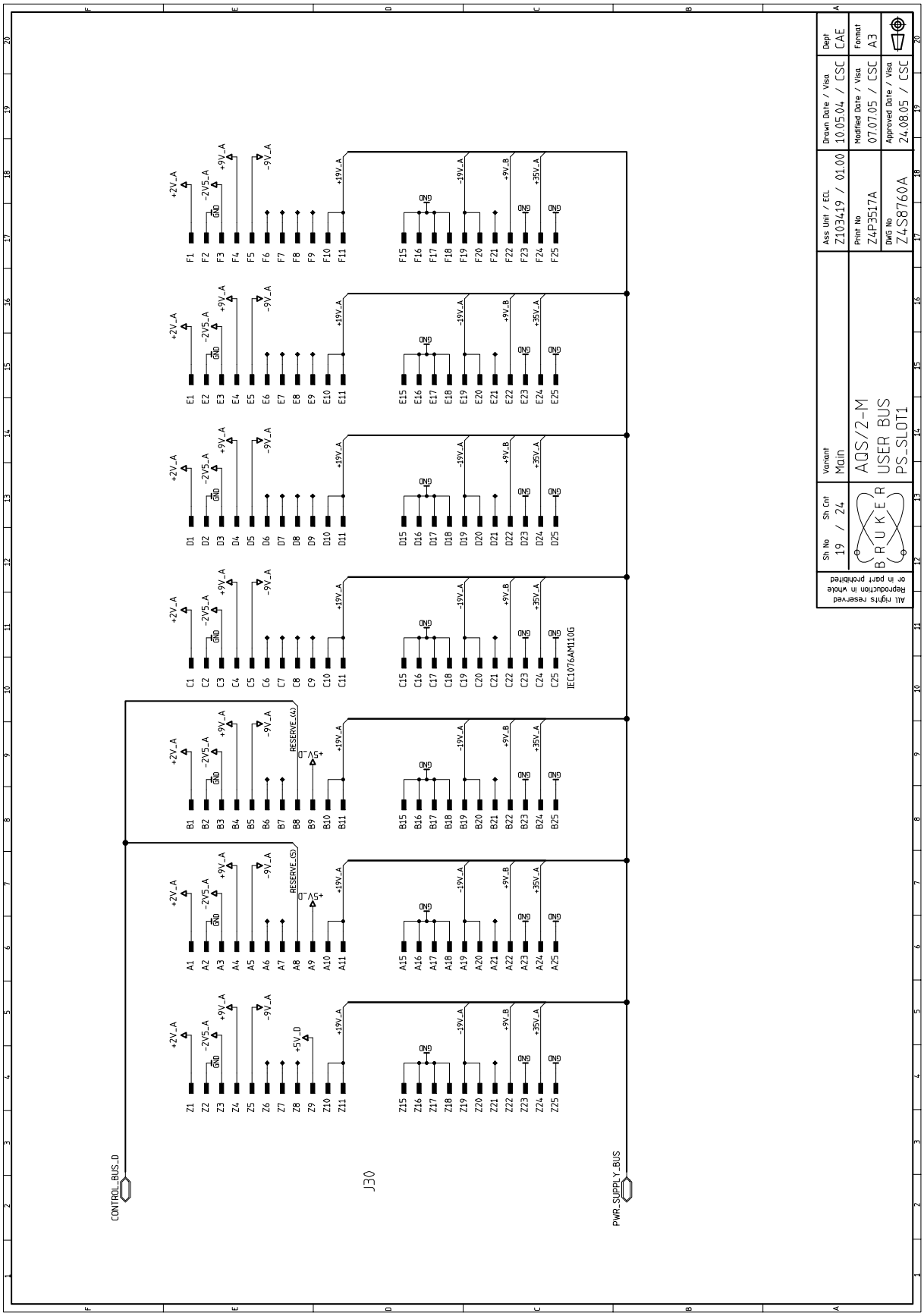


Figure 5.35. Power Supply Slot 2

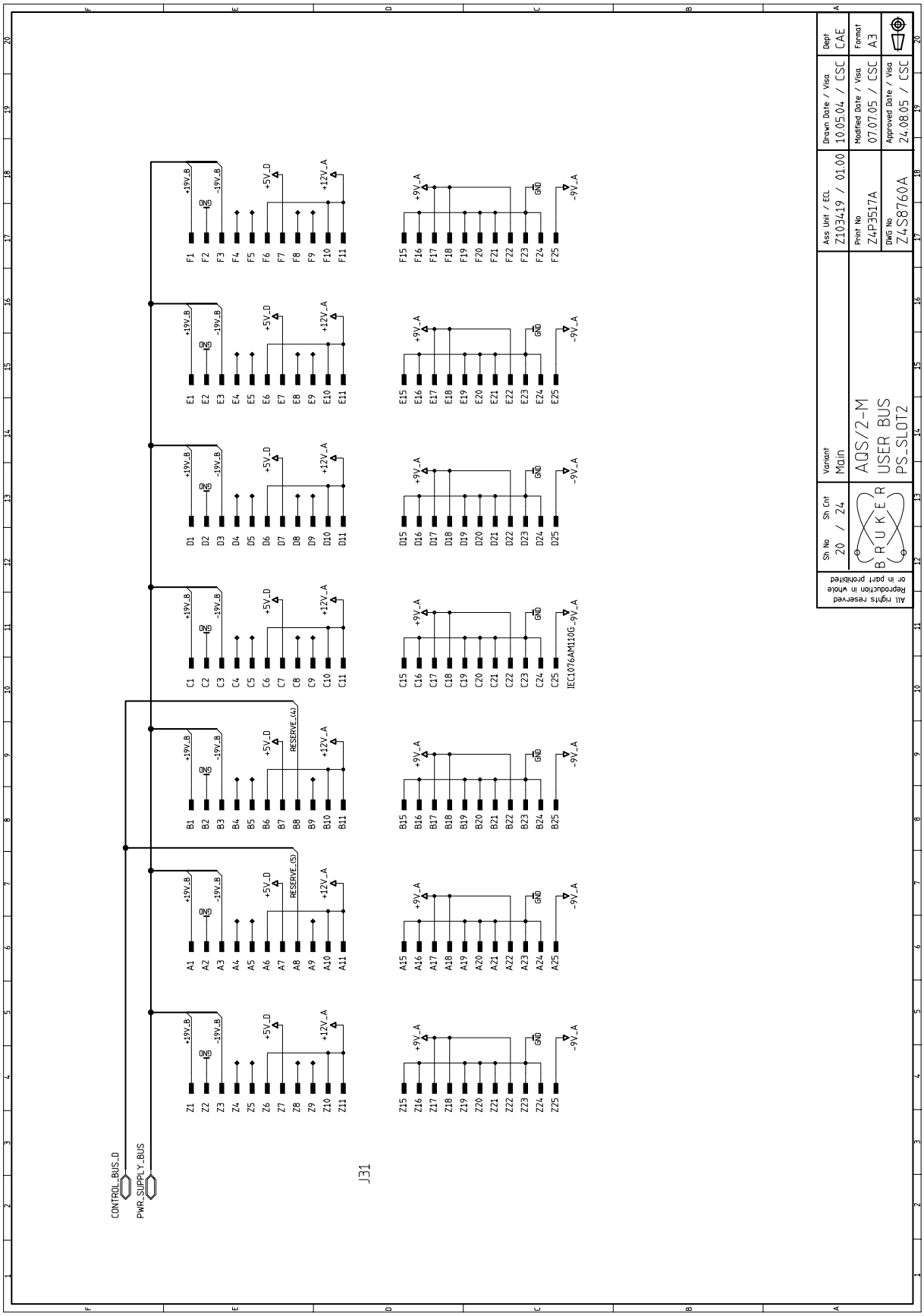


Figure 5.36. Auxilliary Slot 1

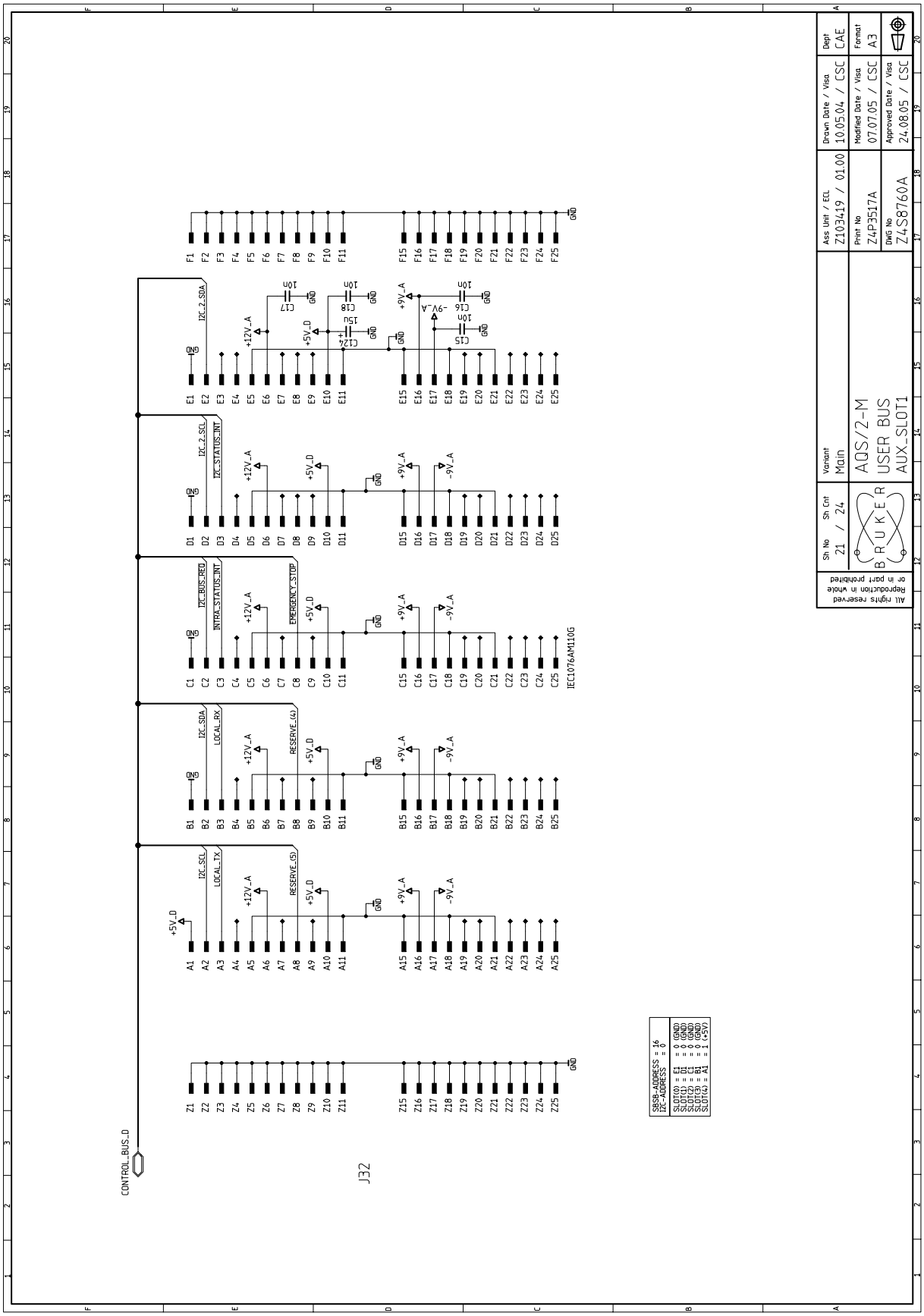


Figure 5.37. Auxilliary Slot 2 (RF-Splitter)

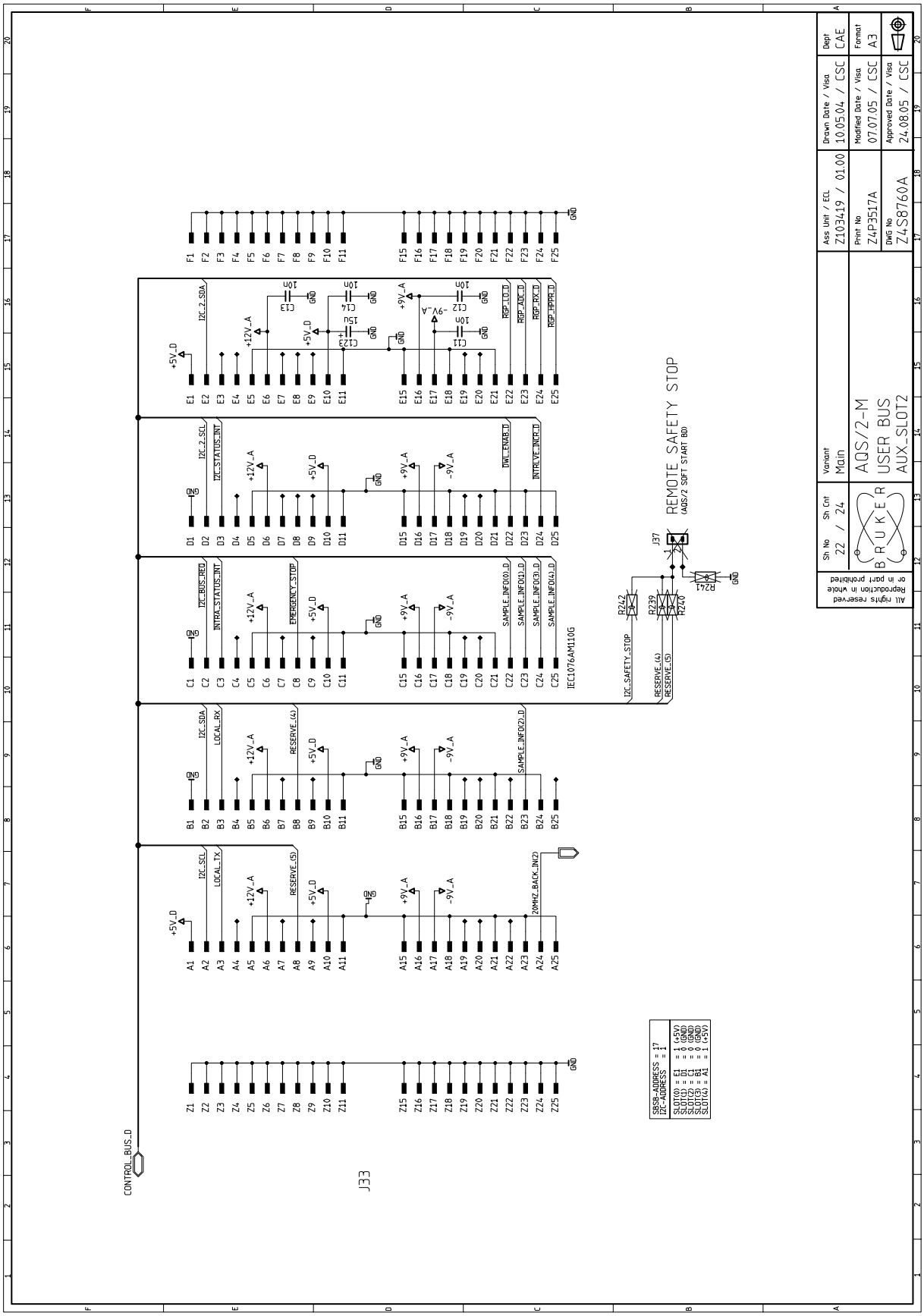
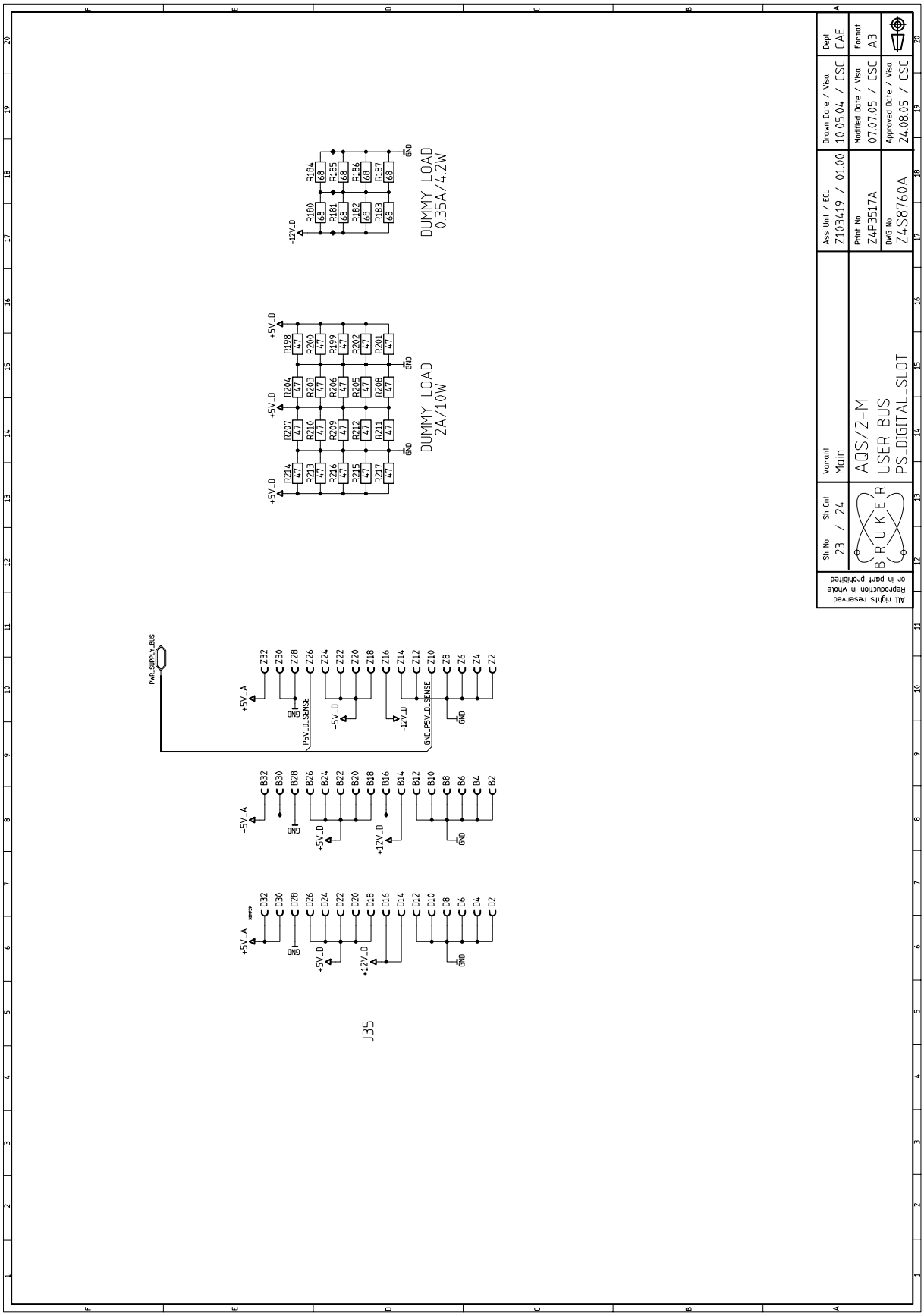


Figure 5.38. PS-Digital Slot



AQS Power Supply 6

Introduction 6.1

The AQS chassis can be equipped with different power supplies, according to the power requirements of the configuration.

Table 6.1. AQS Power Supply Part Numbers

Part Number	Description	Power Supply Type	Chassis Type
87577	IPSO AQS POWER SUPPLY	switched PS	AQS/3
H9489	AQS POWER SUPPLY DIGITAL 350W	switched PS	AQS/2, AQS/2-M
H9520	AQS POWER SUPPLY DIGITAL 450W	switched PS	AQS/2, AQS/2-M
Z003402	AQS PSM1 POWER SUPPLY MODULE	linear PS	all AQS
Z003403	AQS PSM2 POWER SUPPLY MODULE	linear PS	all AQS
Z003404 [a]	*AQS PSM3 POWER SUPPLY MODULE*	linear PS	AQS/2, AQS/2-M
Z102023	AQS PSM5 POWER SUPPLY MODULE	linear and switched PS	all AQS
W1345050	POWER SUPPLY COMPACT 28V 20A	switched PS	AQS/2, AQS/3
Z104783	AQS PSM HPLNA	switched PS	all AQS
Z107413	AQS PSM ADM	switched PS	all AQS

a This unit is obsolete. The replacement power supply is the AQS PSM5.

Table 6.2. AQS Power Supply Comparison Table

Shortname	Supply Output						Power	Load
IPSO AQS PS	+5V 26A	+5V 13A	+12V 9A	-12V 0.1A	+3.3V 11A	+5VSB 2A	350W	IPSO, Fan USER BUS[a]
PS DIGITAL 350W PS DIGITAL 450W	+5V 36A 50A	+5V 10A 14A	+12V 8A 9A	-12V 2A 3A			350W 460W	VME BUS[b], Fan USER BUS
PSM1	+2V 0.5A	-2.5V 0.2A	+19V 6.4A	-19V 2.5A	+9V 5A	+35V 0.2A	220W	USER BUS HPPR
PSM2 PSM5	+19V 1.5A 1.5A	-19V 1.5A 1.5A	+12V 5.8A 17A	+9V 5.6A 7.3A	-9V 2.7A 3.9A		200W 470W	USER BUS HPPR
PS BLA 28V	+28V 20A						560W	internal BLA (pulsed power)
PSM HPLNA	+500V 0.2A	+20V 0.1A	-5V 3A				117W	HPPR/2 HPLNA (max. 2 modules)
PSM ADM	+7.5V 10A	+19V 2A	-19V 1A	-36V 1A	-60V 1A		228W	HPPR/2 ADM

a Supply for all units connected to the USER BUS (SGU, RXAD, DRU, REFERENCE etc.)

b Supply for all units connected to the VME BUS (CCU, FCU, TCU, RCU etc.)

AQS Switched Power Supply Units *6.2*

- IPSO AQS POWER SUPPLY (87577)
- AQS POWER SUPPLY DIGITAL 350W (H9489)
- AQS POWER SUPPLY DIGITAL 450W (H9520)
- POWER SUPPLY COMPACT 28V 20A (W1345050)

These units consist of a compact switched power supply module with multiple outputs. The ac-input cable connects to the line output socket at the rear side of the chassis. The dc-outputs connect to the backplane.

The supply status is indicated with LED‘s on the front panel.

The units have no serviceable parts or fuses.

Figure 6.1. View Switched Power Supply

IPSO AQS POWER SUPPLY
AC-input cable: CABLE RD 3P400
POWER ADAPTER (87938)

AQS POWER SUPPLY
DIGITAL 350W

POWER SUPPLY
COMPACT 28V 20A

AQS PSM HPLNA *6.2.1*

The PSM HPLNA consists of a compact AC/DC power supply module with multiple outputs. The input cable connects directly to the line output socket at the rear side of the chassis. The dc-outputs connect to two D-SUB connectors with high-voltage pins on the front panel.

The supply status is indicated with LED‘s on the front panel.

The unit has no serviceable parts or fuses.

Figure 6.2. View PSM HPLNA

Attention HIGH VOLTAGE:

The D-SUB connectors A and B carry high voltage (+500Vdc).

AQS PSM ADM 6.2.2

The PSM ADM consists of a compact AC/DC power supply module with multiple outputs. The input cable connects directly to the line output socket at the rear side of the chassis. The dc-outputs connect to an UT0 connector with 12 dc pins on the front panel.

The supply status is indicated with LED‘s on the front panel.

Figure 6.3. View PSM ADM

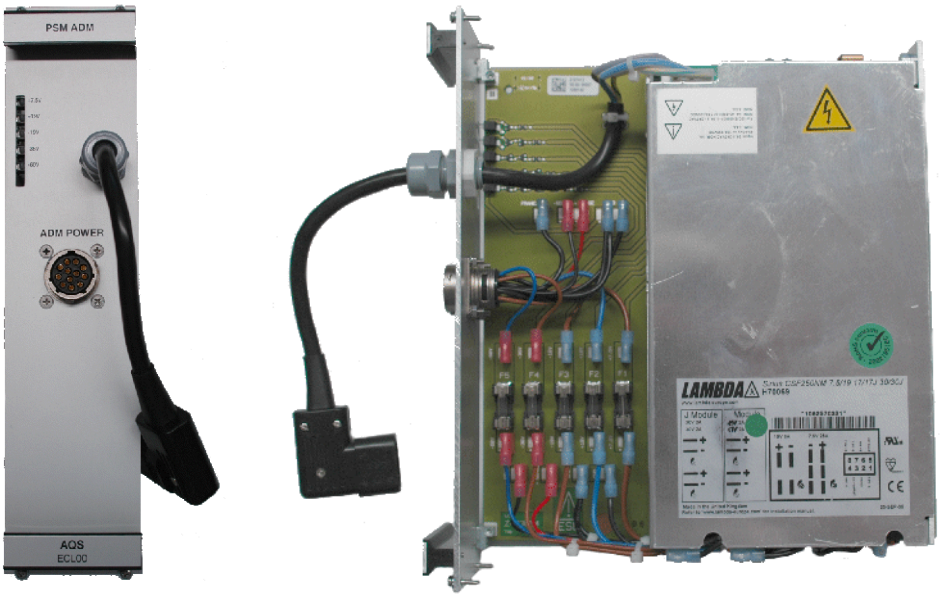
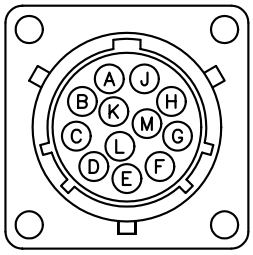


Table 6.3. Pinout ADM POWER Connector



Pin	Signal	Pin	Signal	Pin	Signal
A	GND	E	P19V	J	N60V
B	GND	F	N19V	K	SHIELD (Earth)
C	P7.5V	G	GND	L	PSENSE_P7V
D	P7.5V	H	N36V	M	NSENSE_P7V

Table 6.4. Fuses PSM ADM

SUPPLY	FUSE	CAT_NM	VALUE
+7.5V	F1	2260	10AT
+19V	F2	2254	2AT
-19V	F3	2251	1AT
-36V	F4	2251	1AT
-60V	F5	2251	1AT

Linear Power Supply Modules 6.3

The linear power supply modules consist of rectifiers and linear regulators mounted on an open print. The ac-inputs connects directly to the transformer in the chassis via a front panel connector. The dc-outputs connect to the backplane.

The supply status is indicated with LED‘s on the front panel.

The PSM5 has an additional switched power supply module mounted on the print. It‘s ac-input cable connects directly to the line output socket at the rear side of the chassis.

PSM1 6.3.1

Figure 6.4. Overview PSM1

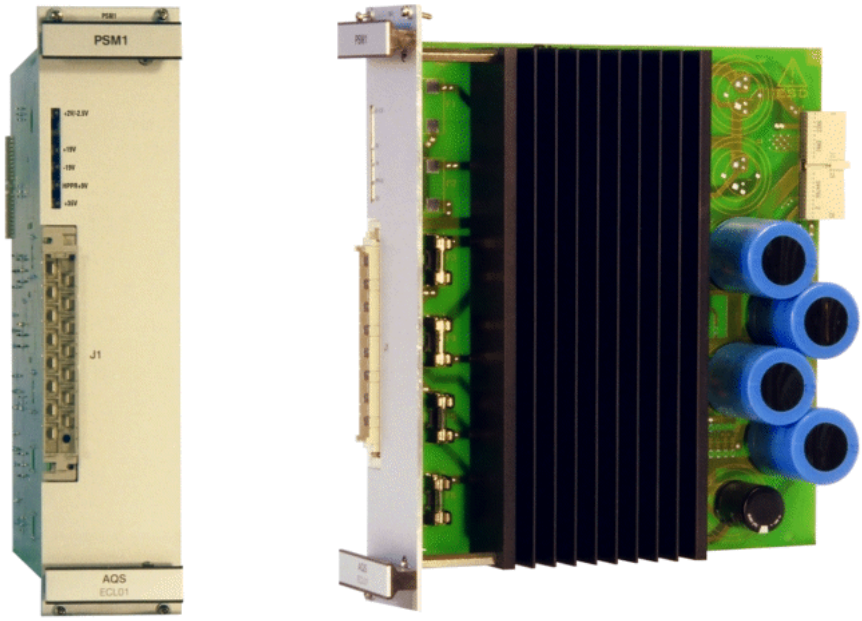


Table 6.5. Fuses PSM1

SUPPLY	FUSE	CAT_NM	VALUE
+19V	F3	2259	8AT
-19V	F4	2256	3.15AT
HPPR +9V	F5	4907	5AT
+35V	F6	2248	0.5AT [a]

a prior fuse was 0.315AT

Figure 6.5. Assembly Drawing PSM1

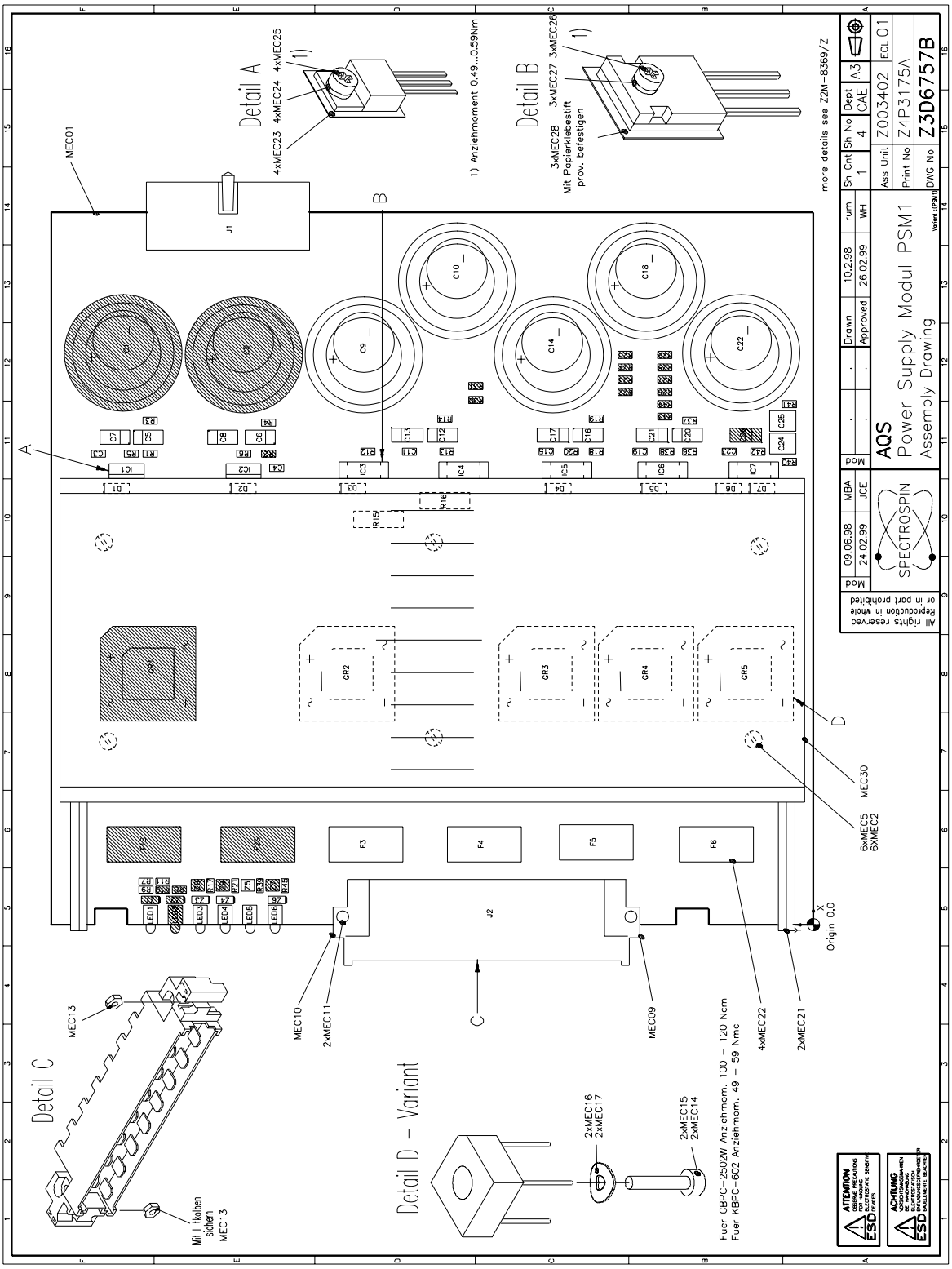


Figure 6.6. Overview PSM2

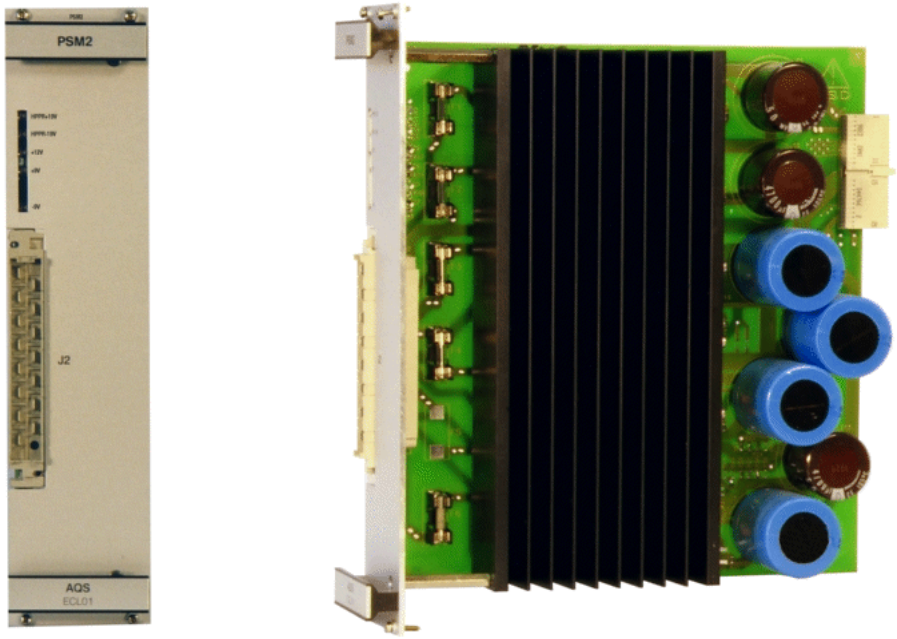
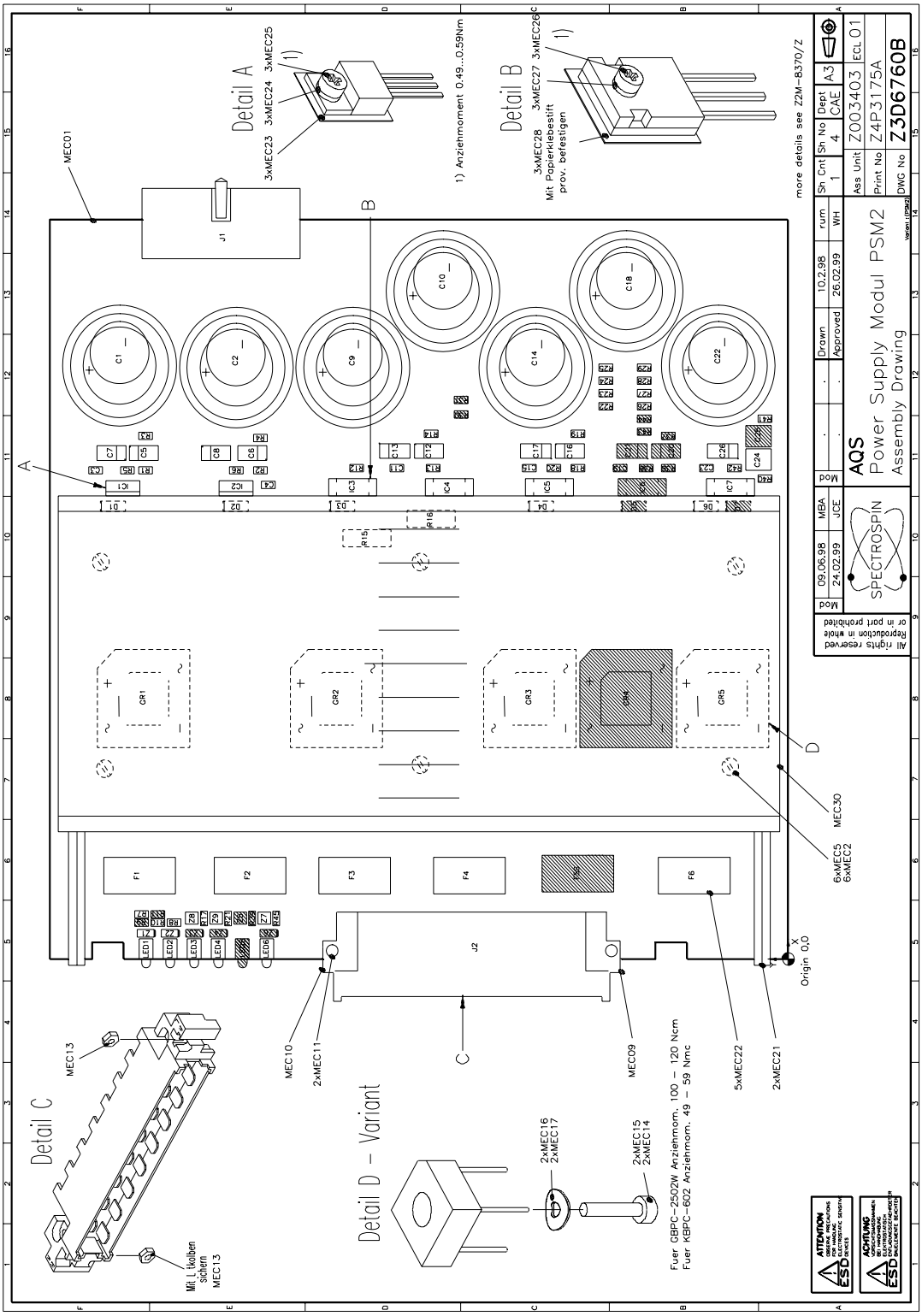


Table 6.6. Fuses PSM2

SUPPLY	FUSE	CAT_NM	VALUE
HPPR +19V	F1	2254	2AT
HPPR -19V	F2	2254	2AT
+12V	F3	2259	8AT
+9V	F4	2258	6.3AT
-9V	F6	2257	4AT

Figure 6.7. Assembly Drawing PSM2



PSM5 6.3.3

The AQS PSM5 is fully compatible to the PSM2 and PSM3. The main difference is the increased output power.

If a PSM5 is used as a replacement of a PSM3, an additional frontplate (Z12170) may be necessary to cover the empty space left behind by the wider unit.

Figure 6.8. Overview PSM5

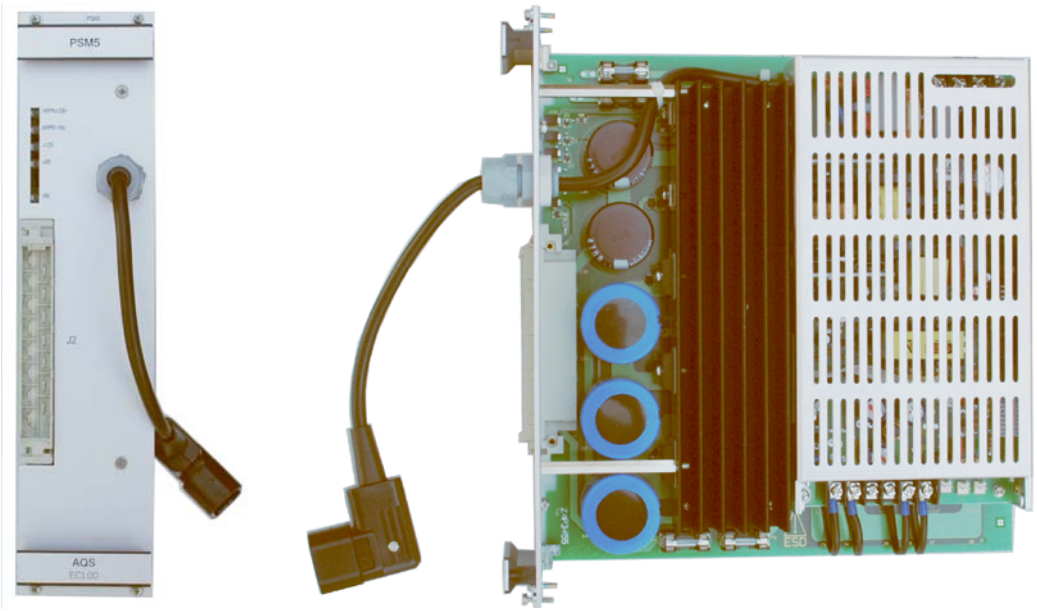


Table 6.7. Fuses PSM5

SUPPLY	FUSE	CAT_NM	VALUE
HPPR +19V	F1	2254	2AT
HPPR -19V	F2	2254	2AT
+9V	F3	2259	8AT
-9V	F4	4907	5AT

The +12V supply from the switched power supply module has no serviceable fuse.

Figure 6.9. Assembly Drawing PSM5

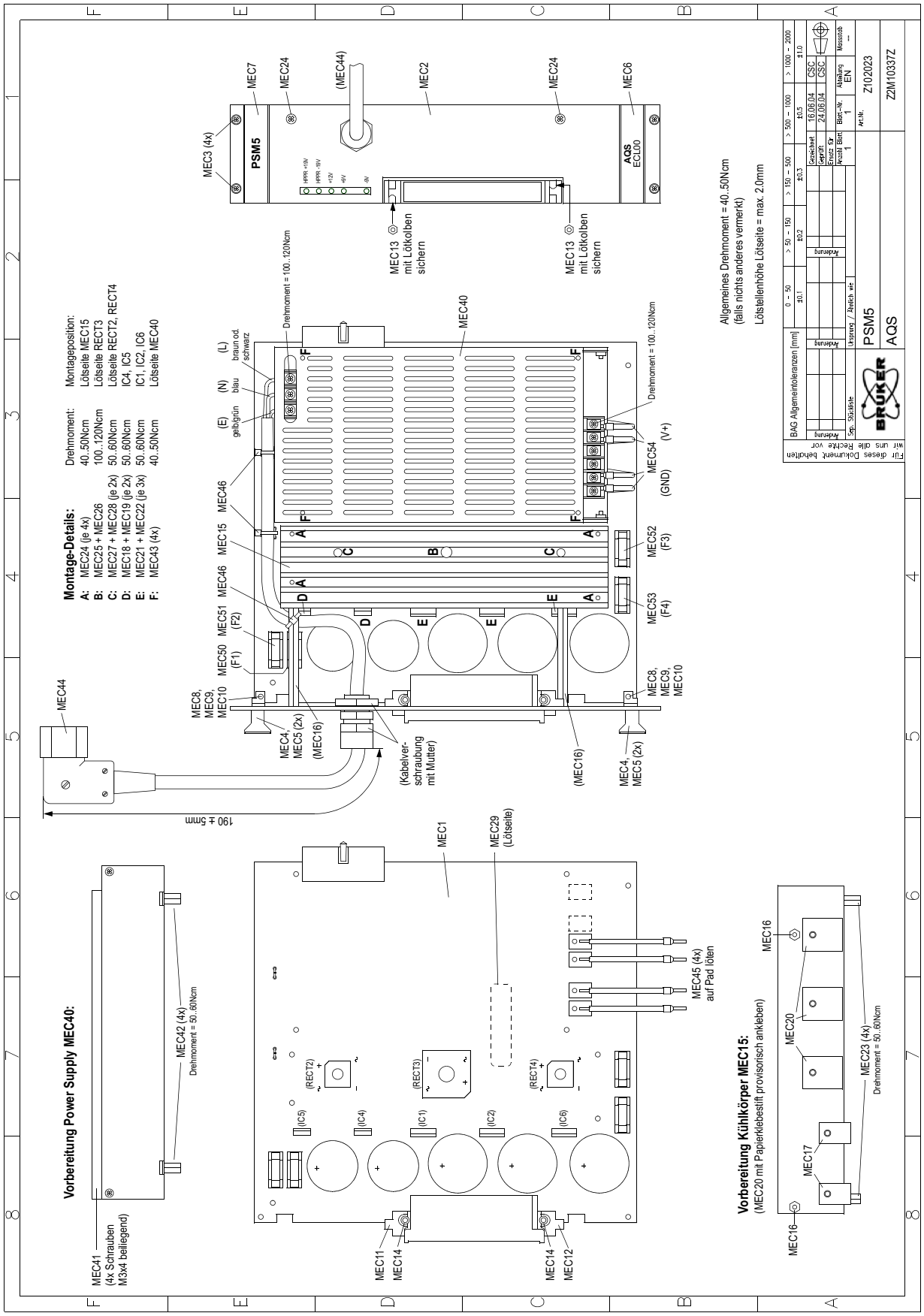


Figure 6.10. Power Supply Module 1-3 Block Diagram

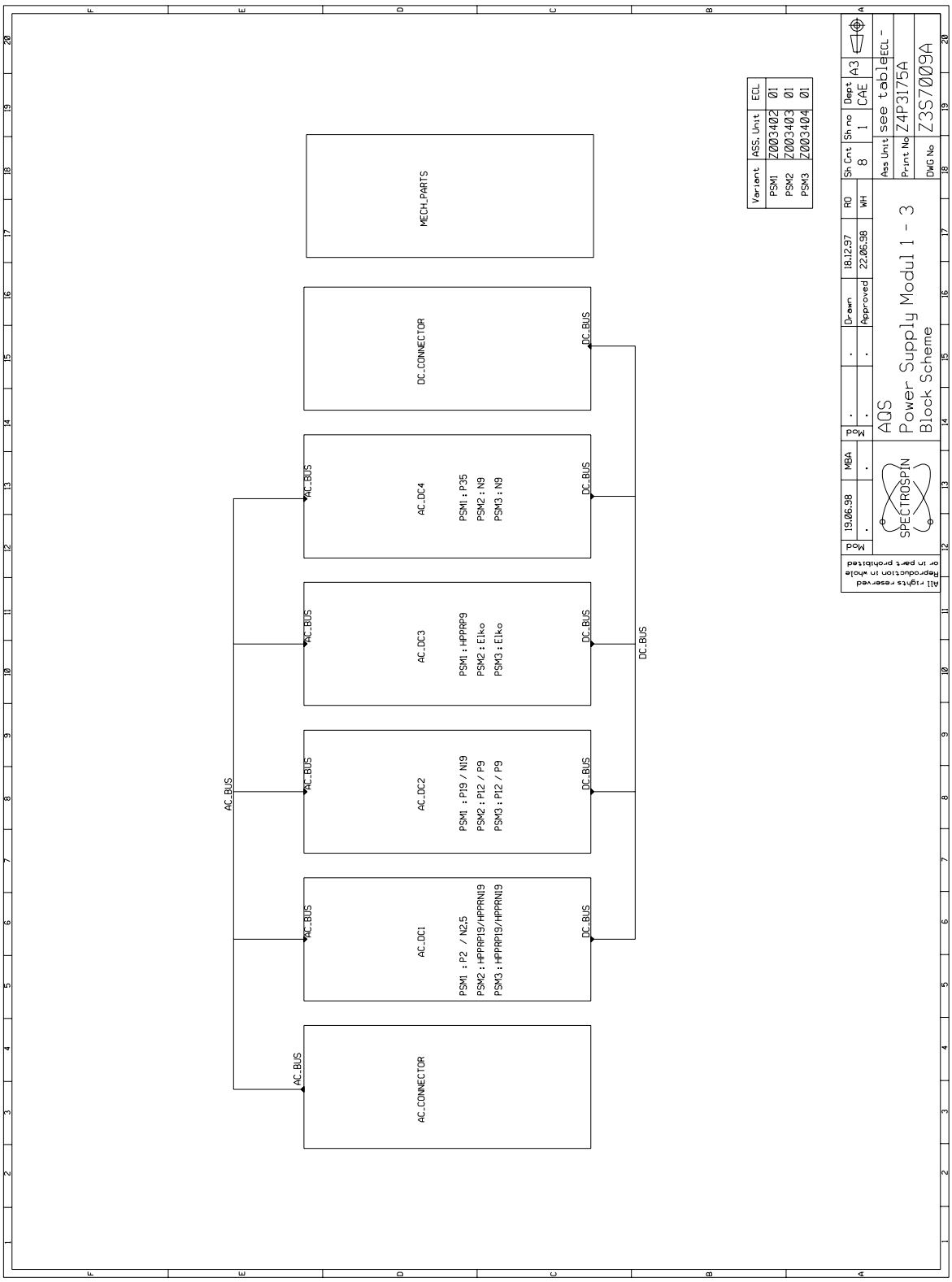


Figure 6.11. AC Connector

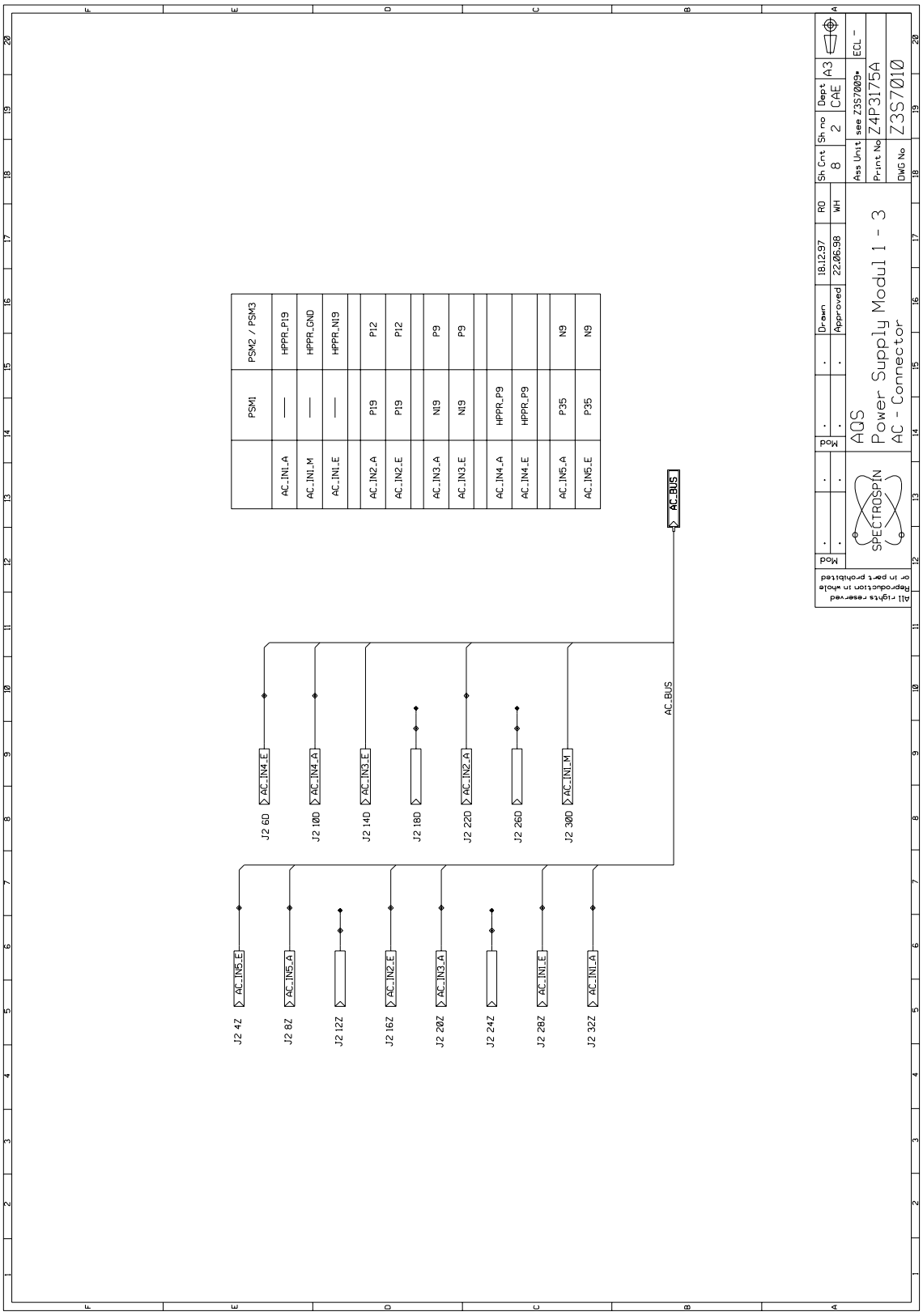


Figure 6.12. Converter AC-DC1

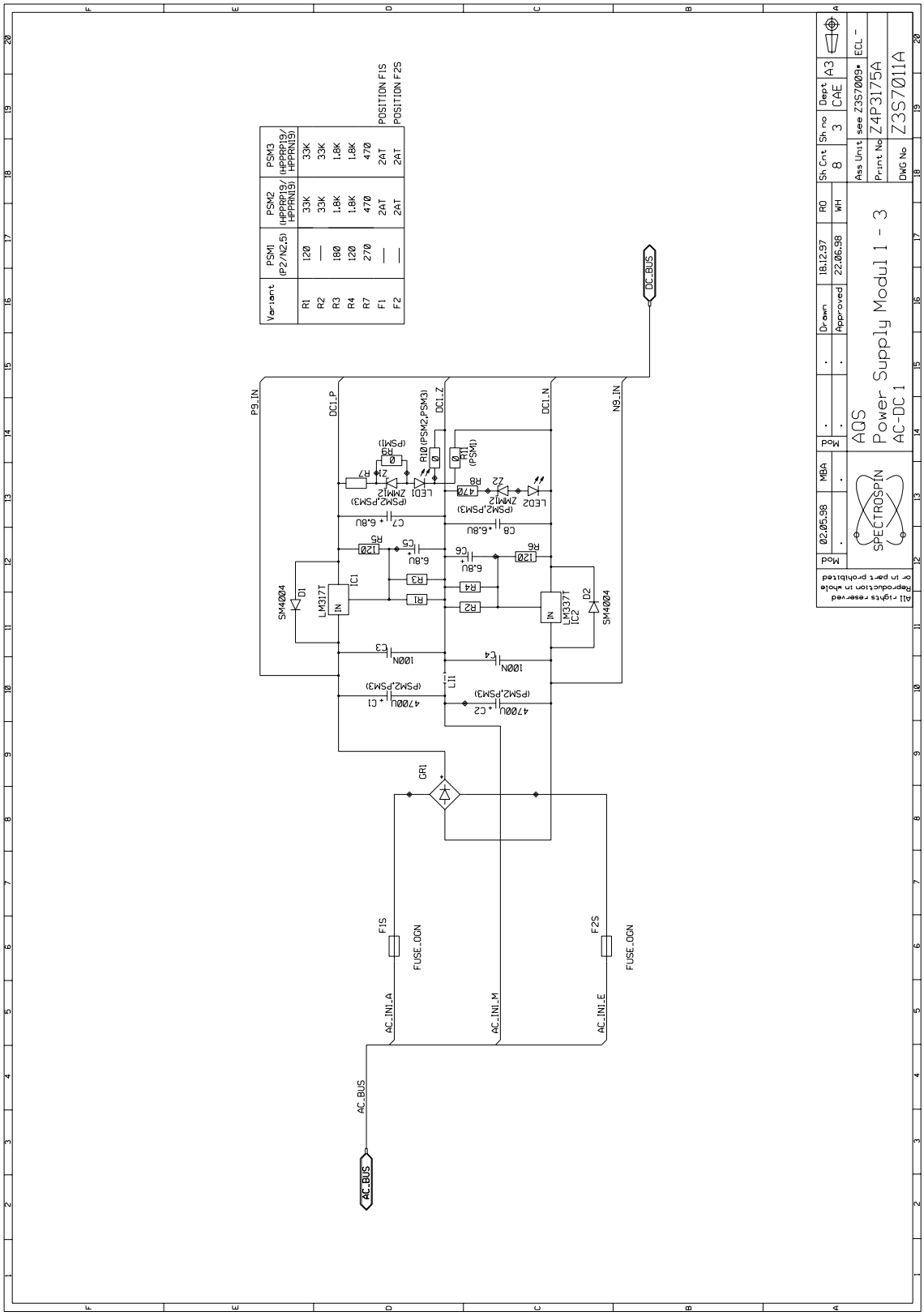


Figure 6.13. Converter AC-DC2

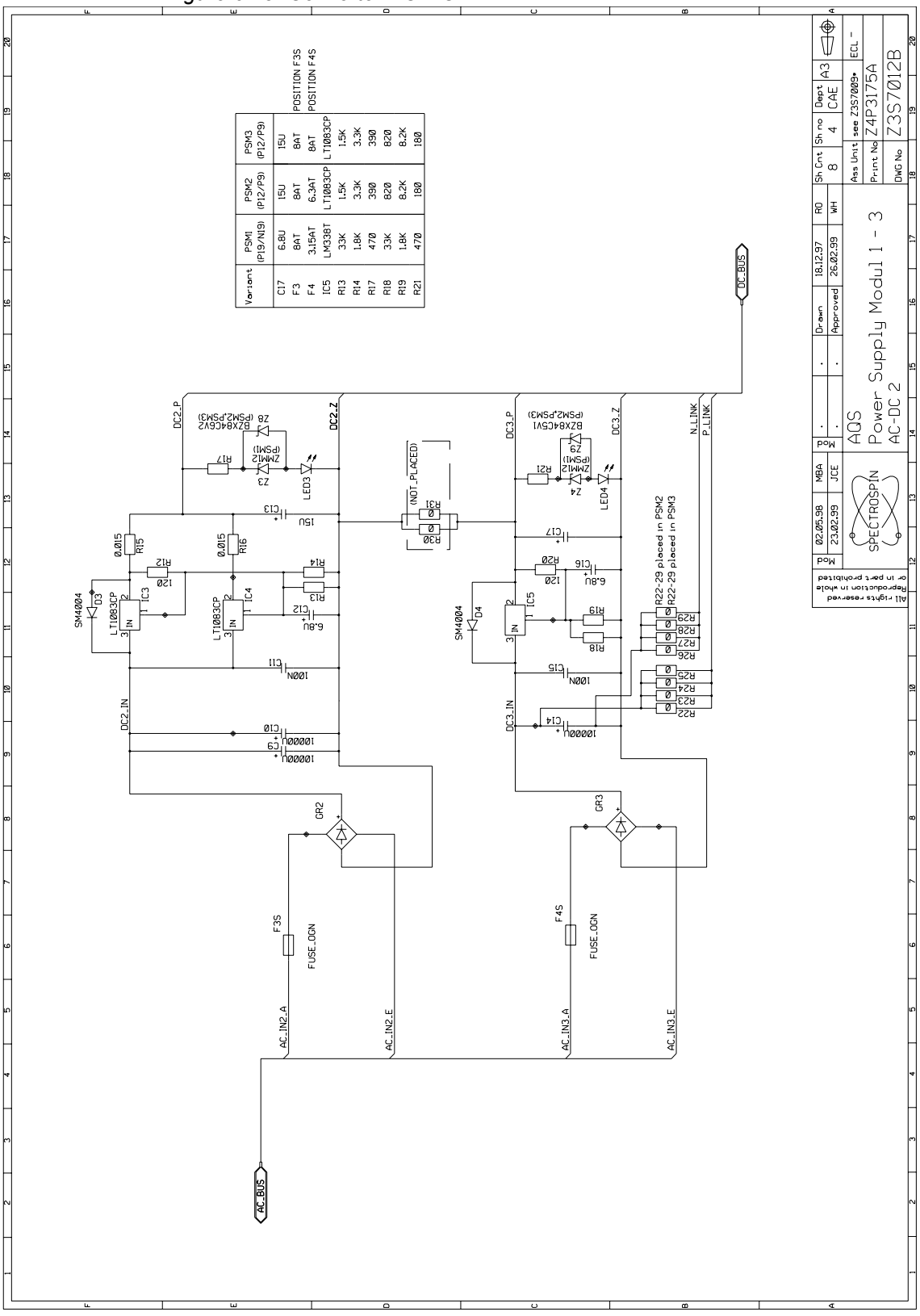


Figure 6.14. Converter AC-DC3

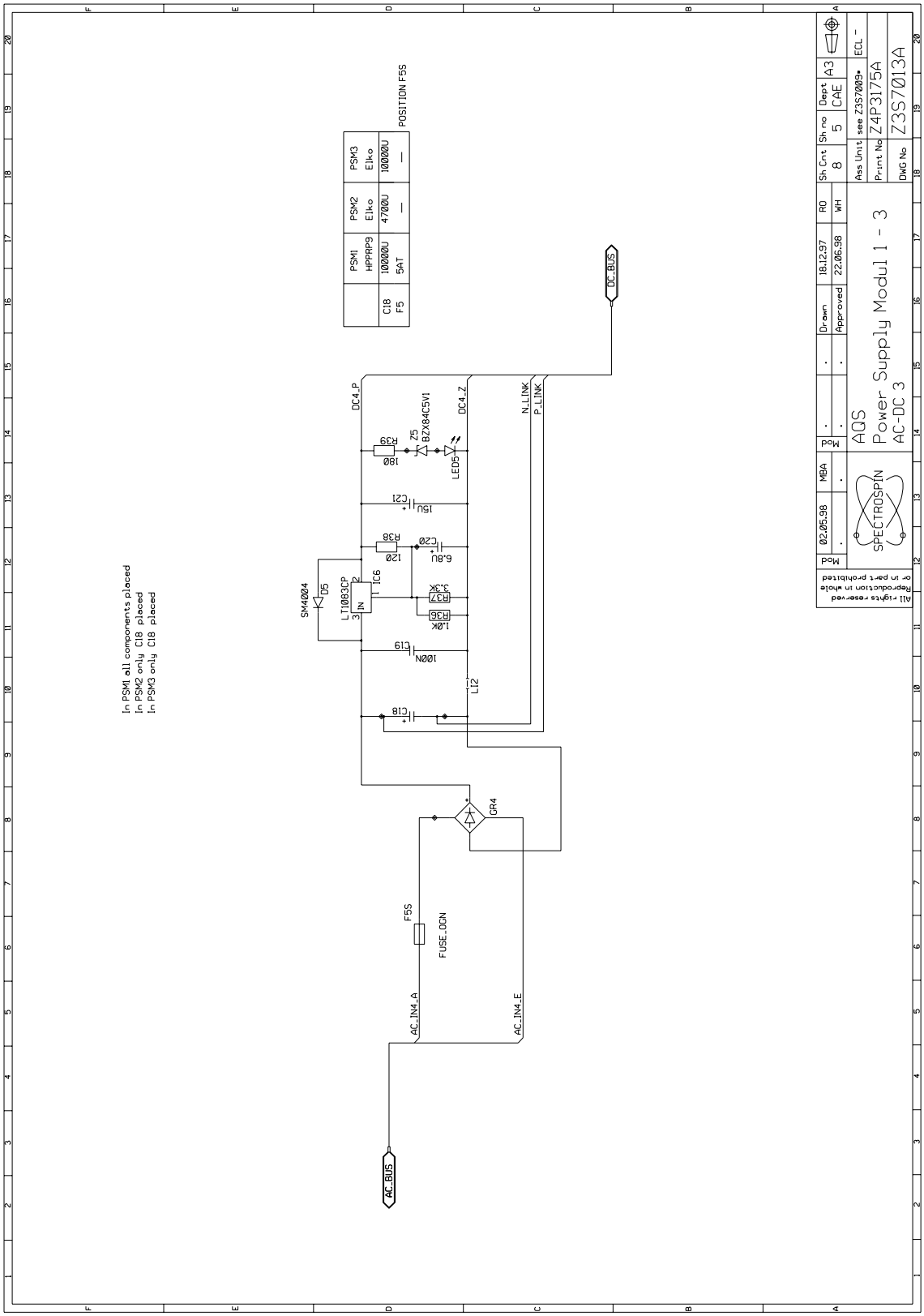


Figure 6.15. Converter AC-DC4

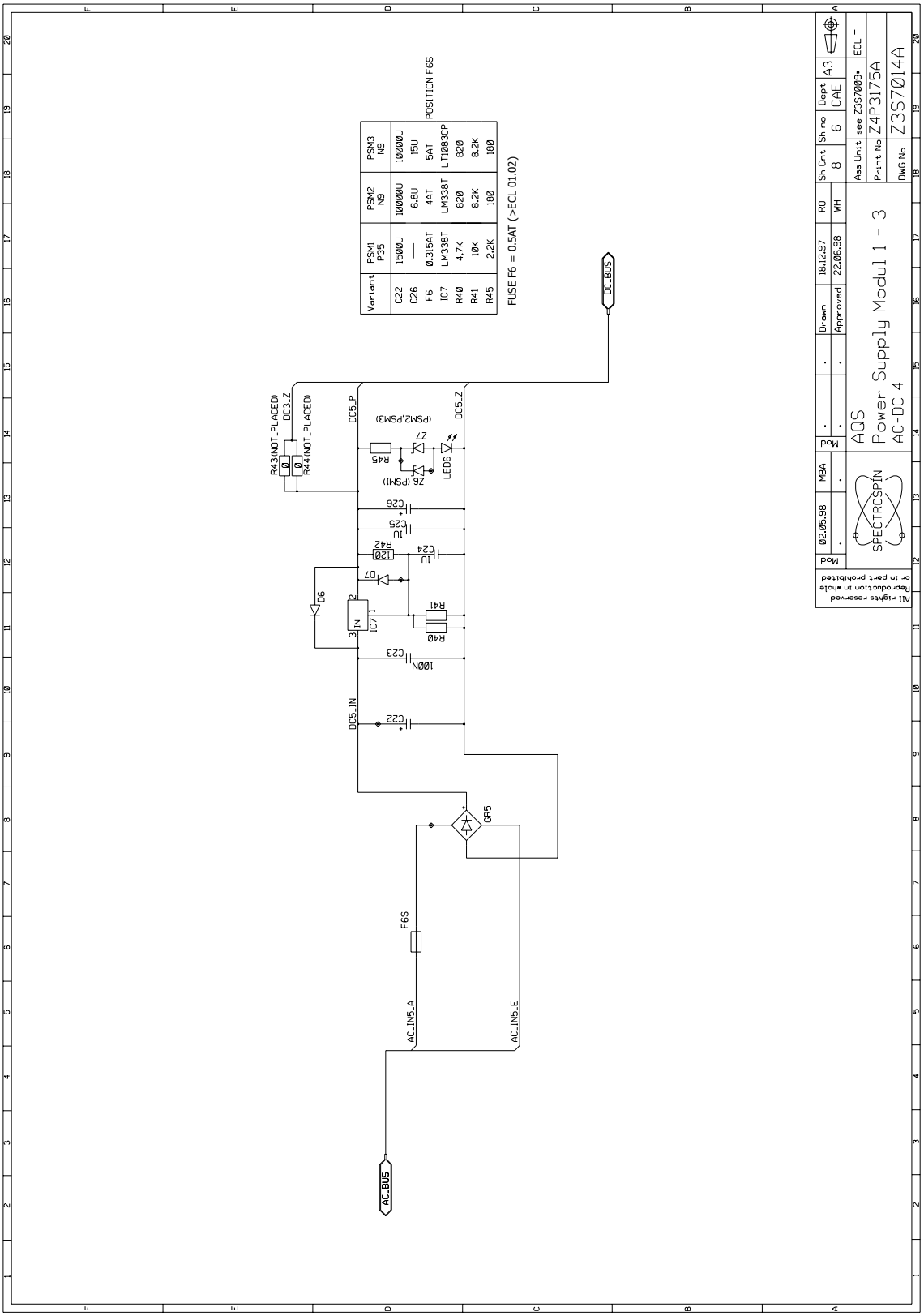


Figure 6.16. DC Connector

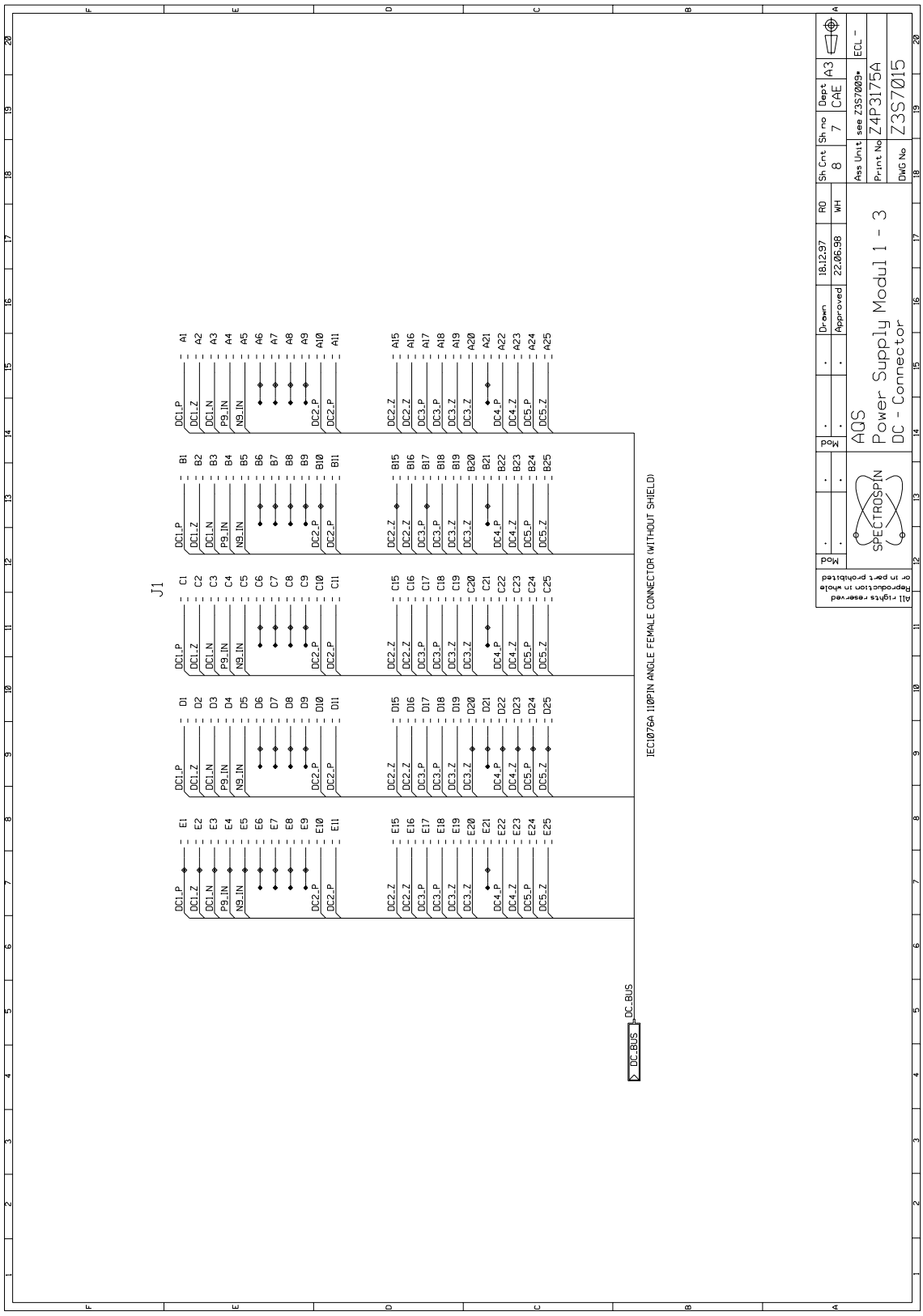


Figure 6.17. Power Supply Module 5 Block Diagram

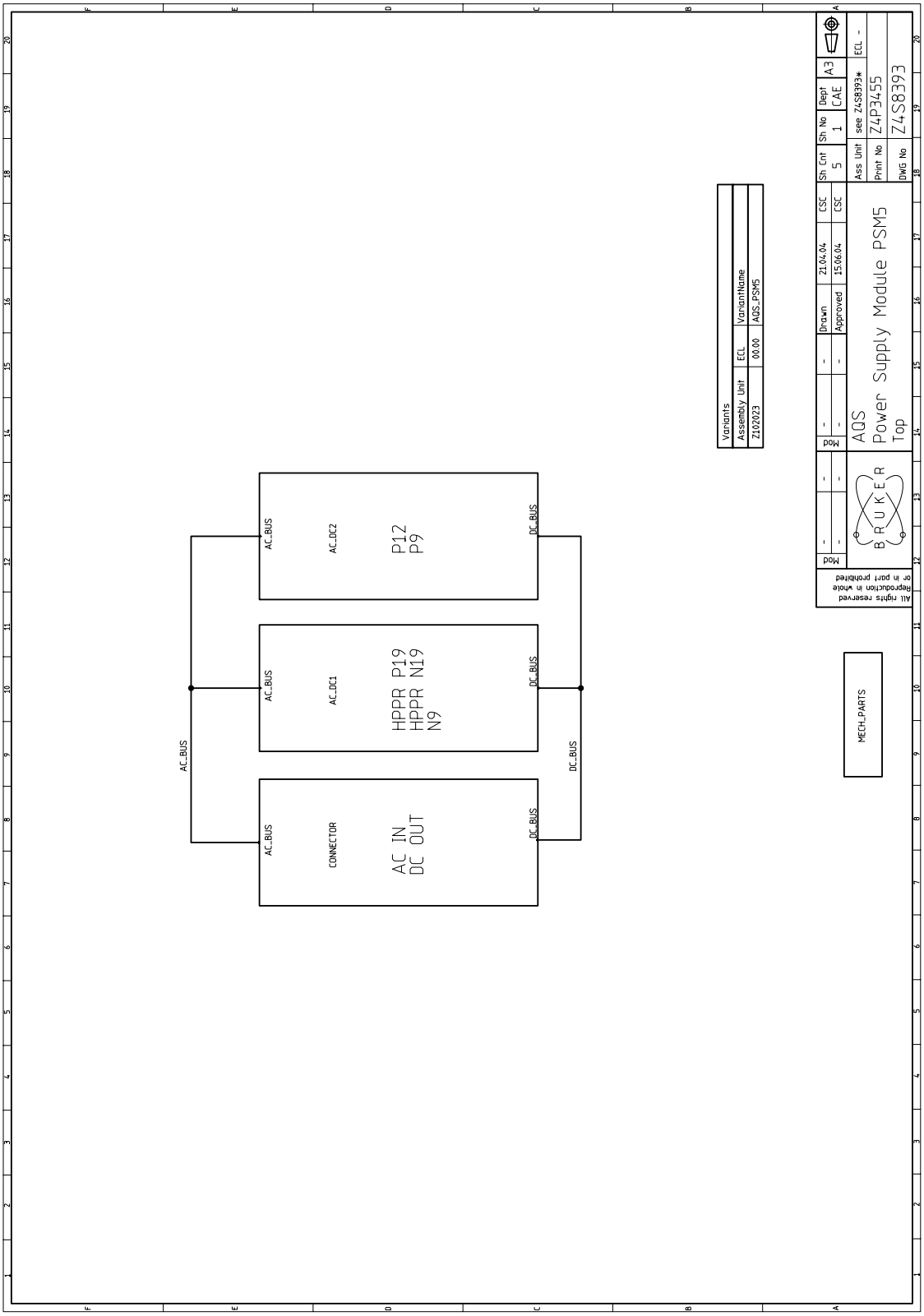


Figure 6.18. Connectors

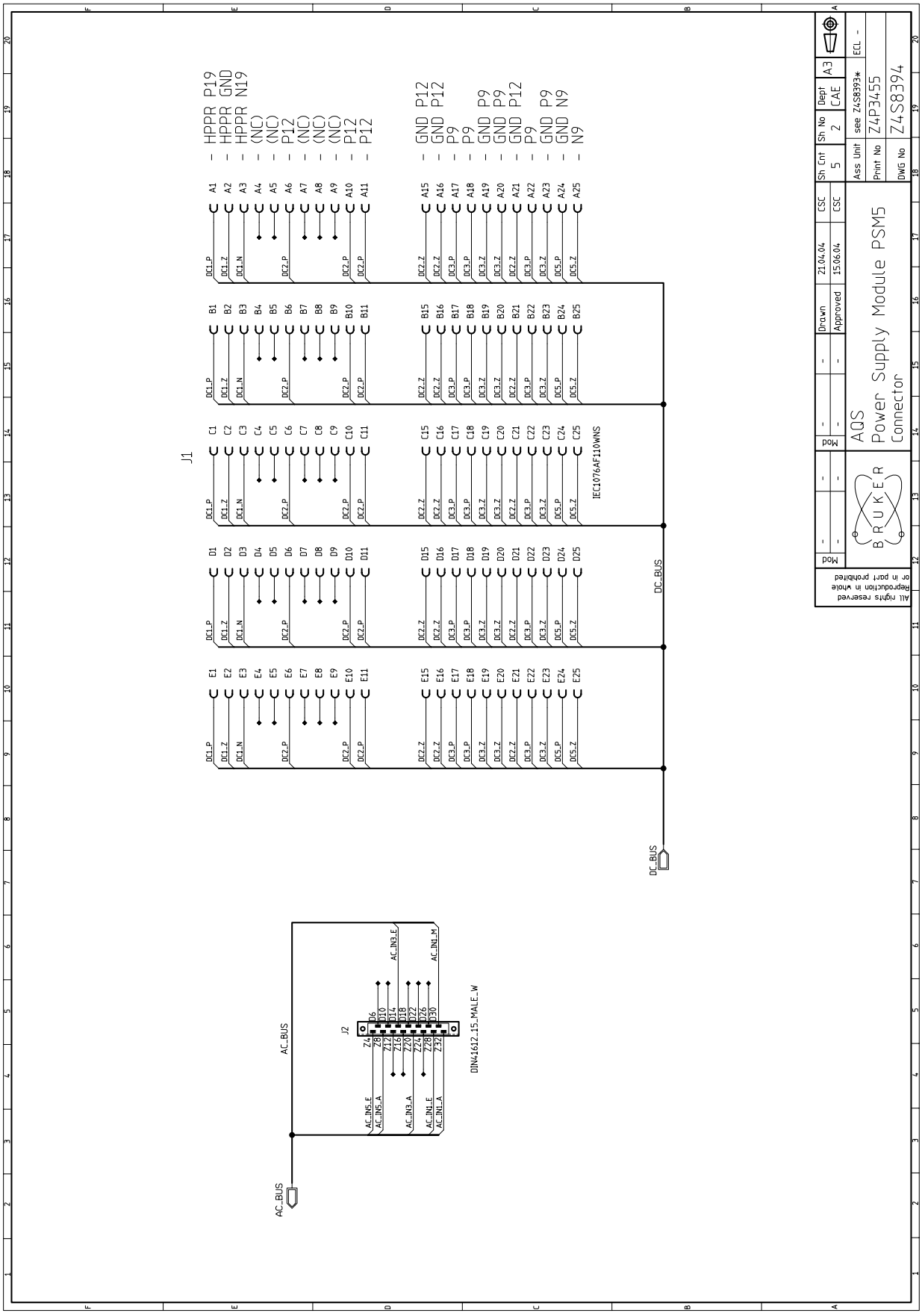


Figure 6.19. Regulators HPPR P19V, HPPR N19V, N9V

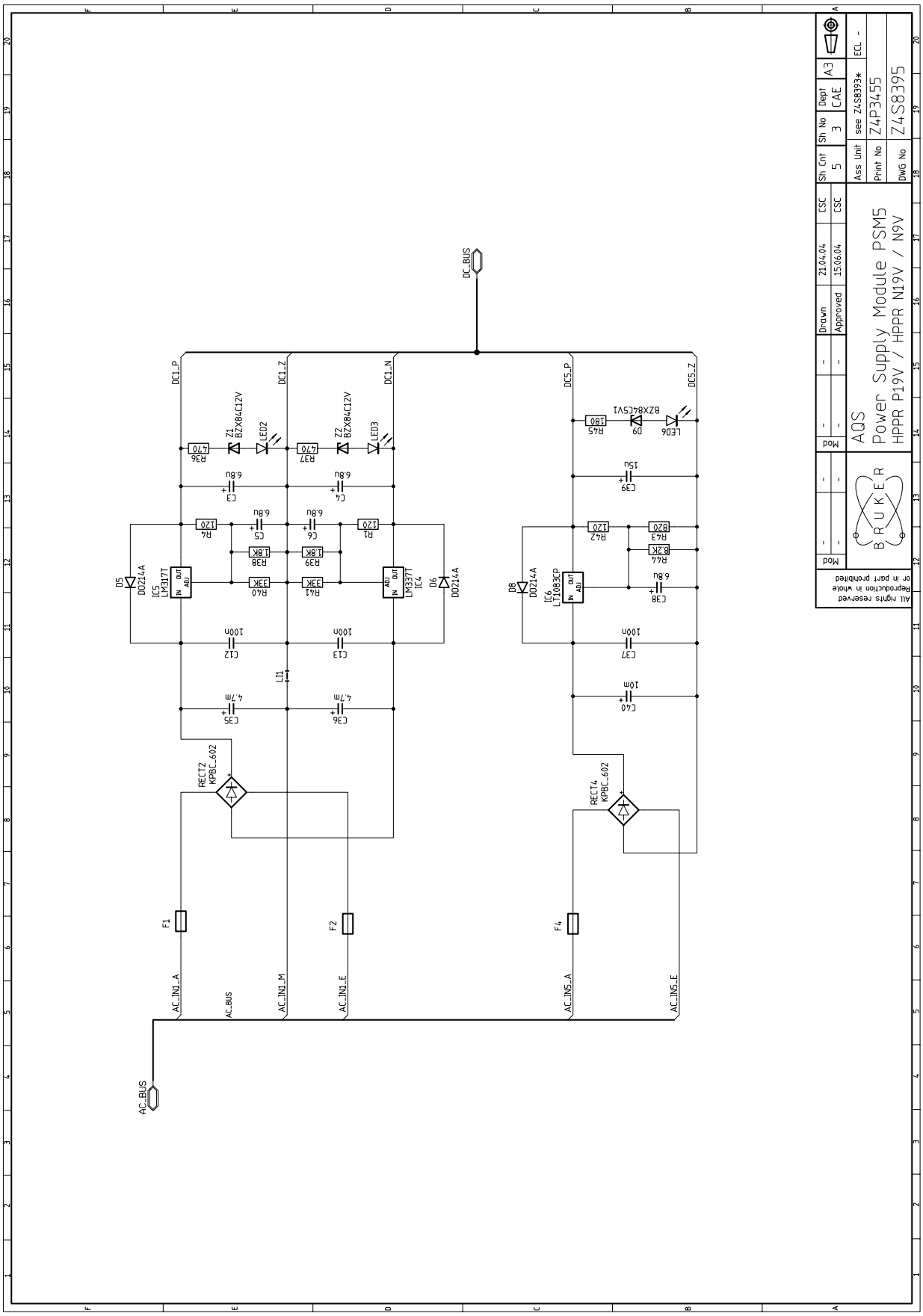
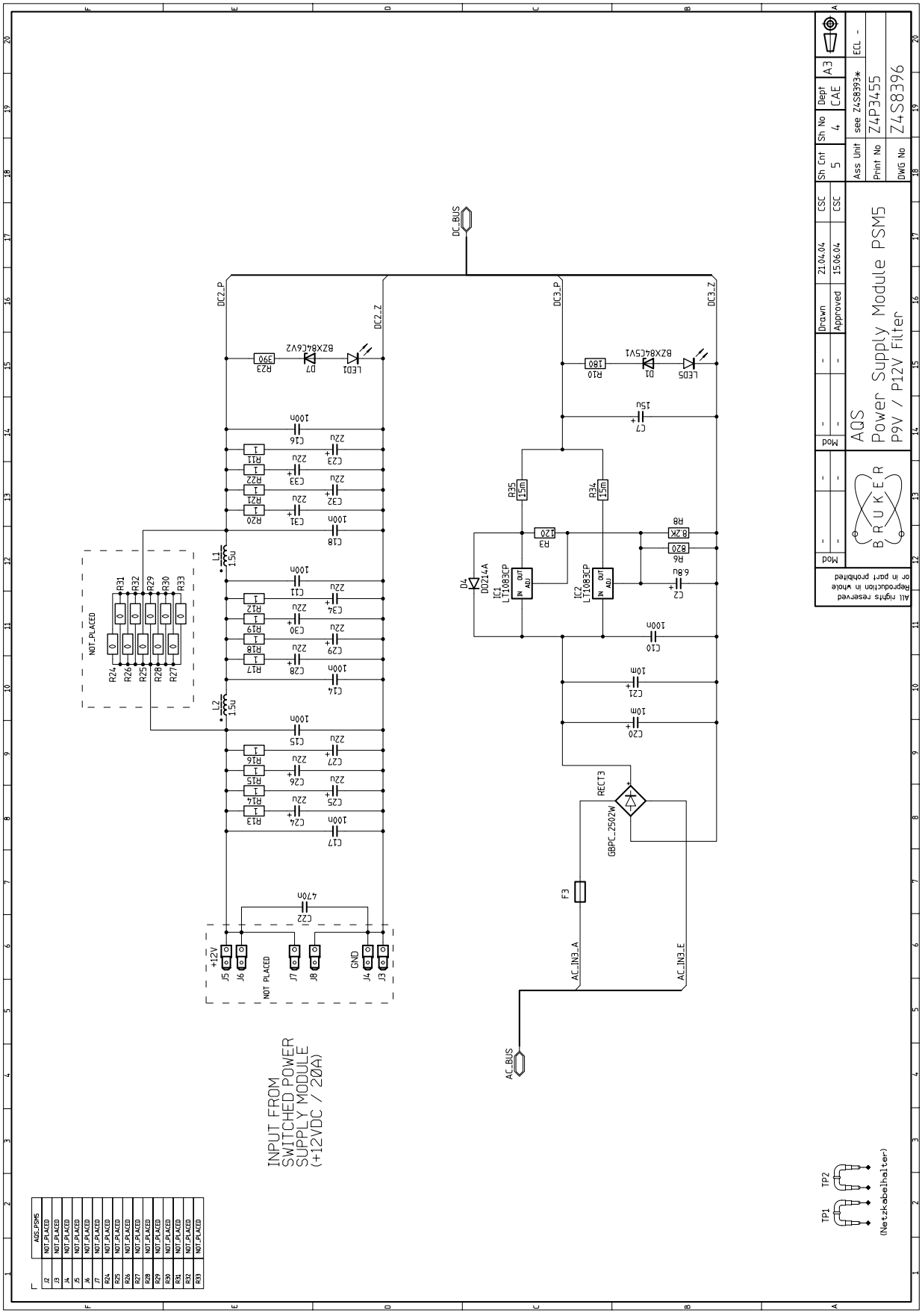


Figure 6.20. Regulator P9V, Switcher Module P12V



AQS Reference Board for RXAD 7

Introduction 7.4

The AQS Reference Board is an exclusive development for the AV spectrometer series. As spectrometers become more sophisticated the importance of coherence and in particular phase coherence between the various channels as well as between the transmission and receiving paths is more and more important. The philosophy of the AV is to ensure that all RF signals as well as all clocks originate from one source. This source is a temperature controlled crystal oscillator (OCXO) at the heart of the AQS Reference Board. Apart from clock signal each AQS Reference Board will provide the necessary RF signals for up to 4 SGU/2. This is to enable the SGU/2 to generate frequencies using a so called up converter. The Reference Board REF/2 unit allows (in addition with two BB-splitters) to supply 6 SGU/2. The location of the AQS Reference Board will depend on the configuration. Technically it can be placed in the slots 3 to 5. Standard configurations have placed it in slot 3 immediately to the right of the RXAD.

Functions/ Description 7.5

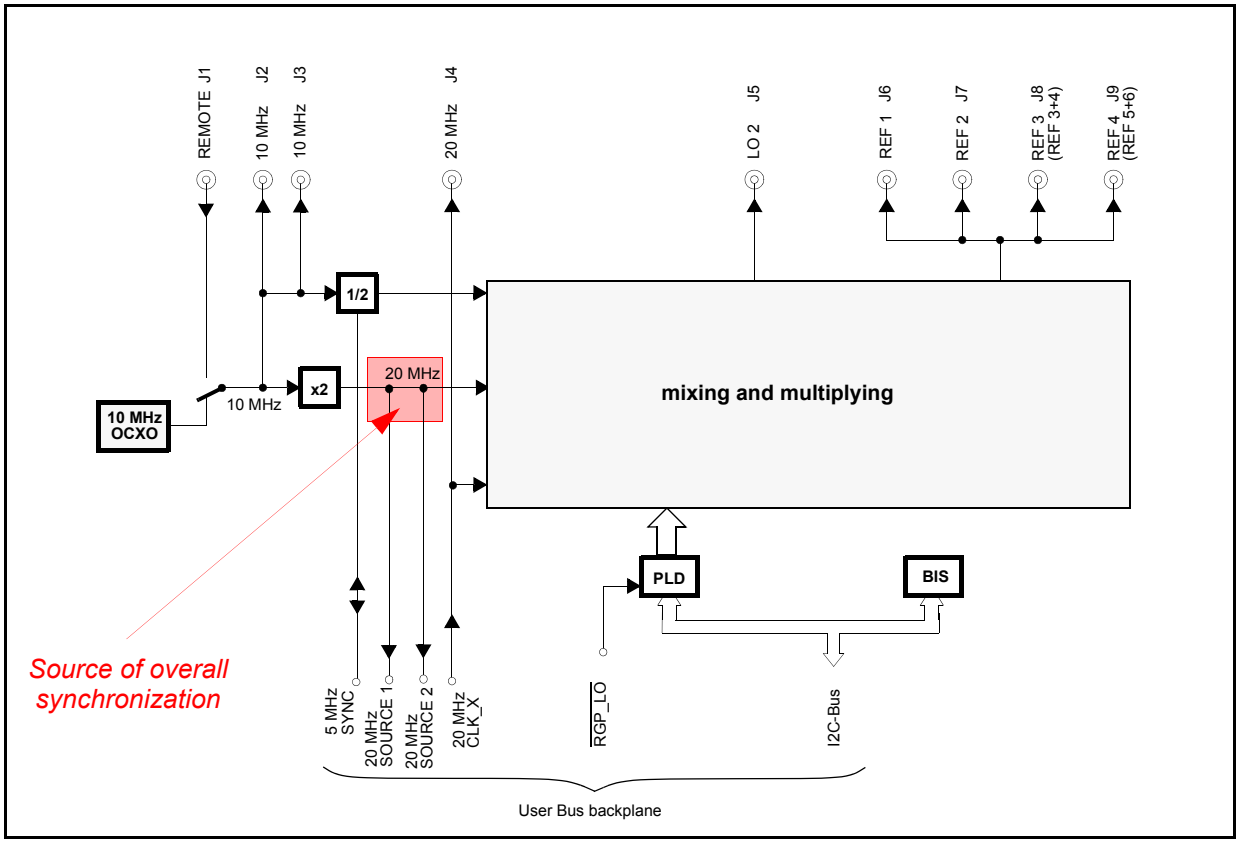
The Reference Board is responsible for the synchronization through the generation of various frequencies. Specifically the generated signals are:

1. Detection reference frequency (LO2 = 720 MHz) for the receiver. There are four versions of the AQS Reference Board that supports the AQS RX-BB or RXAD series (AQS REFERENCE 400, AQS REFERENCE 600, AQS REFERENCE 1000 and AQS REFERENCE/2 1000).
2. 20 MHz synchronization clock for all SGU/2, the IPSO and the user backplane
3. auxiliary signals (frequency mixture) for up to four SGU/2 (six for REF/2)
4. 10 MHz signal for the BSMS LTX

At the heart of the AQS Reference Board is a 10 MHz oven controlled oscillator (OCXO) see ***Figure 7.21.***. This signal is mixed and multiplied and afterwards ported to the four REF outputs (REF1-REF4, J6-J9). The 10 MHz signal for the BSMS LTX is ported directly through connector J2

The detection reference frequency (LO2 = 720 MHz) for the AQS RXAD family of receivers is derived from the 10 MHz OCXO and ported to J5.

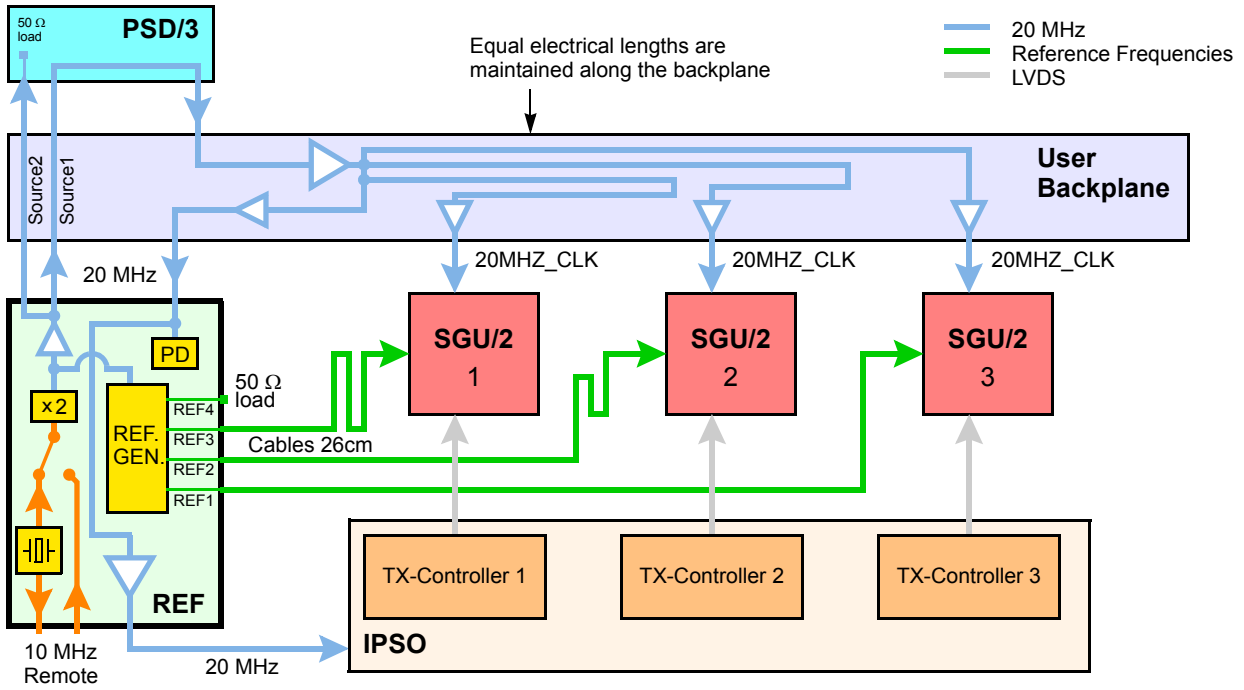
Figure 7.21. Block diagram of AQS Reference Board



Overall synchronization *7.5.1*

The overall synchronization is achieved using the 20 MHz signal generated at the first frequency doubler which is transmitted to the backplane by an ECL signal (20MHZ SOURCE1 and 2). This is transformed into a differential clock signal (20MHZ_CLK_X / 20MHZ_CLK_X) used to clock all slots of the user bus, which will of course include the SGU/2. The same 20 MHz clock is returned and is ported out via J4 and is used to clock the IPSO. Essentially all clocking frequencies in both the analog and digital sections of the AQS are synchronized with the 20 MHz clock of the AQS Reference Board.

Figure 7.22. Overall synchronization of spectrometer for an AQS/3 chassis



Synchronization of a single AQS/3 Chassis:

There is no extra synchronization to be done on a single AQS/3 chassis as long as the cable length are considered carefully (see ***7.5.2 on page 155***).

One 20 MHz signal (Source2) is not required and is terminated on the PSD/3 and the other 20 MHz signal (Source1) is used for the AQS/3 user bus slots.

Cable lengths *7.5.2*

To maintain this synchronization particularly with respect to phase all signals should pass through identical electronic circuitry as well as cables of equal length. The circuitry along the user backplane is designed to ensure equal electrical lengths regardless of the physical slot occupied by an SGU/2.

If cables are to be replaced then the same length cable should be used. For example the cables carrying the mixture of 6 frequencies to the SGU/2 are a standard length of 26cm.

Bus interfaces *7.5.3*

The AQS Reference Board is controlled by the I^2C bus on the backplane. This bus is used to:

1. read the BIS data (Bruker information system, successor to BBIS)
2. allow the AQS controller (DRU in slot 1) to load settings which are stored in an FPGA (field programmable gate array) on-board into DACs to control the REF signal output.

Unit Configuration / Version / Jumpers 7.6

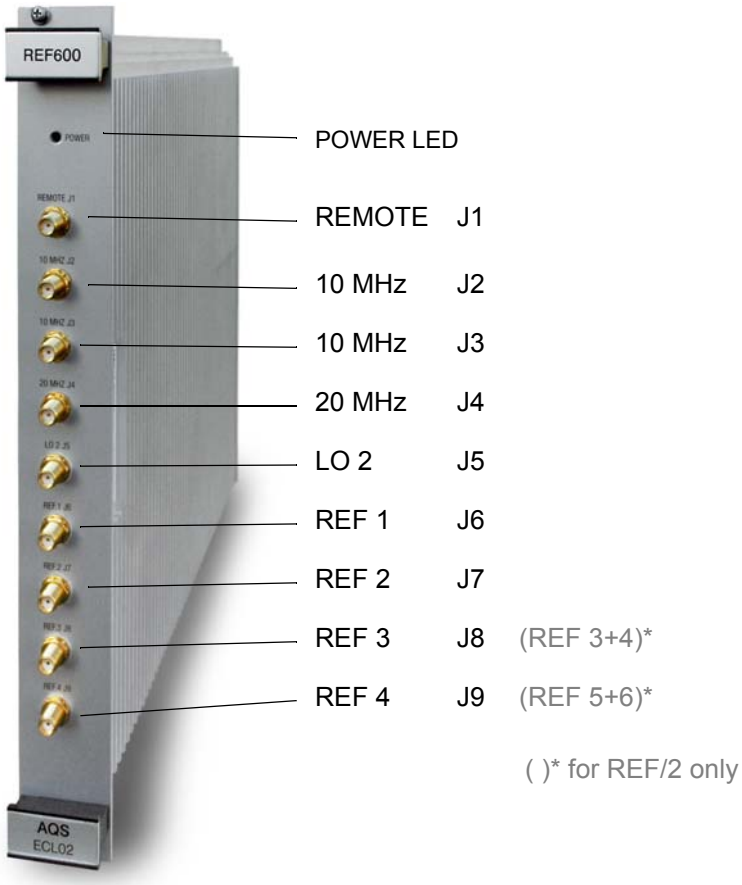
The unit is automatically configured through the ‘cf’ routine. No jumper settings are required.

Differences from previous versions 7.6.4

The AQS Reference Board is developed for the AV series and does not have a counterpart in the AVANCE series.

Front Panel Wiring / Display 7.7

Figure 7.23. AQS Reference Board front panel



J1 REMOTE IN

J1 is an input for external sinusoidal 10 MHz clock and must have a power level in the range 6...13 dBm @ 50 Ω. The presence of this signal will automatically switch off the internal 10 MHz clock generated by the crystal oscillator. This input is nor-

mally not connected except when a second AQS Reference Board is synchronized with the first.

J2 10 MHz OUT

Output to BSMS L-TX J2, used to clock BSMS Lock Transmitter board.
Sinusoidal wave approx. 7 dBm (1.4 Vpp) @ 50 Ω

J3 10 MHz OUT

Output for synchronization with second AQS Reference Board.
Sinusoidal wave approx. 7 dBm (1.4 Vpp) @ 50 Ω

J4 20 MHz OUT

Clock signal to IPSO in ECL logic (emitter coupled logic).
Square wave approx. 1 Vpp @ 50 Ω.
This is the principal synchronization signal for the spectrometer.

J5 LO 2 OUT

Receiver detection reference to AQS RXAD J3.
720 MHz approx. 4 dBm (1 Vpp) @ 50 Ω

J6 - J7 REF 1 and 2 OUT

Frequency mixture to SGU/2: 2.2 Vpp @ 50 Ω at J6 and J7.

J8 - J9 REF 3-4 or 3-6 OUT

At regular REF boards: Frequency mixture to SGU/2.
2.2 Vpp @ 50 Ω at J8 and J9.
At special REF/2 board only: Frequency mixture to BB-SPLITTER.
4.4 Vpp @ 50 Ω at J8 and J9.

POWER LED

See ***"Power Supply / Fuses" on page 158***

Part Numbers and Cables *7.8*

Four versions of AQS Reference Boards are available. They differ for the maximum NMR frequency up to 400, 600 or 1000 MHz and for the number of SGU/2 they can feed.

For 4 SGU/2:

- AQS REFERENCE BOARD 400, P/N Z003265
- AQS REFERENCE BOARD 600, P/N Z003936
- AQS REFERENCE BOARD 1000, P/N Z003937

For 6 SGU/2 with BB SPLITTERs on J8 and J9:

- AQS REFERENCE BOARD/2 1000, P/N Z104236

Troubleshooting / Unit replacement / Tips 'n' Tricks *7.9*

1. Terminate any unused outputs with 50 Ω.
2. If you suspect the OCXO is faulty switch to an external 10 MHz signal (> 4 dBm resp. 1 Vpp @ 50 Ω) by applying it to REMOTE J1.
3. Ensure that any unused REF outputs (J6-J9) are properly terminated with a 50 Ω connector.

Diagnostic Tests *7.10*

Not applicable.

Specifications *7.11*

The principal specification is that of the stability of the crystal oscillator which is specified to:

1 x 10^{-9}/day on REF1000 and REF/2 1000
3 x 10^{-8} total deviation for REF600
2 x 10^{-9}/day on REF400

Power Supply / Fuses *7.12*

The Reference Board uses +5 V, +12 V, ±9 V, +19 V from the backplane see ***"Backplane Connector Ref. unit" on page 159***. The power LED on the front panel indicates that all necessary voltages are present and at the correct level. If the voltage level drops then the LED will go out. Thus once the power LED lights further investigation of the backplane to check the precise voltage is unnecessary.

Backplane Connector *7.12.5*

The table below shows the pin assignment for the rear 110 pin connector. Note the presence of the source and clock signals.

Table 7.8. Backplane Connector Ref. unit

	z	a	b	c	d	e	f
1	GND	GND		5MHZ_SYNC	GND		GND
2	GND	20MHZ_SOURCE1	GND				GND
3	GND	GND	20MHZ_SOURCE2		GND		GND
4	GND	20MHZ_CLK_X	GND				GND
5	GND	GND	20MHz_CLK_X		GND	RGP_LO	GND
6	GND		GND				GND
7	GND				GND		GND
8	GND		GND				GND
9	GND				GND		GND
10	GND		GND				GND
11	GND				GND		GND
						23x GND (21%)	
15	GND	SLOT2	SLOT1	SLOT0	GND		GND
16	GND		GND	I2C_SDA		GND	GND
17	GND			I2C_SCL	GND		GND
18	GND		GND			GND	GND
19	GND				GND		GND
20	GND		GND			GND	GND
21	GND	P5V		P9V	P9V	P9V	GND
22	GND	P5V		N9V	N9V	N9V	GND
23	GND	P5V	P19V	N19V	RACK1	P12V	GND
24	GND	P5V	P19V	N19V	RACK2	P12V	GND
25	GND	P5V	P19V	N19V	RACK3	P12V	GND

AQS RXAD 8

Introduction 8.1

The AQS RXAD is a high dynamic range receiver for NMR with integrated analog-to-digital converter (ADC). The AQS RXAD is available for different nuclei ranges (RXAD400, RXAD600, RXAD1000) and also in a broadband version (RXAD-BB). The AQS RXAD is fully integrated in the AQS concept and runs in conjunction with the AQS SGU, AQS REF and AQS DRU. The AQS RXAD is located in the analog section of the AQS rack. The board is physically as long as the other AQS units (REF/SGU/DRU) and attaches to the user bus (backplane) directly.

As the name suggests the AQS RXAD receiver is concerned with the amplification of the signal 'received' from the sample and therefore uses a intermediate frequency that is generated by the input signal and the local oscillator synthesizer signal. In contrast to former receiver types with analog audio frequency output (RX-22, AQS RX-BB) the output signal from the AQS RX*AD* is in a raw digital format already. The integrated high performance ADC combines wide bandwidth with optimal shielding, shorter signals paths (lower EMI sensitivity) and less wiring.

The AQS RXAD has a sufficient gain range to be set in 1 dB steps. The correct setting of the RF gain will ensure that the receiver output is matched to the ADC range.

The entire receiver function is controlled by a microprocessor. This allows accurate gain setting, phase/amplitude and dc offset adjustment in the quadrature-module via a RS485-Interface which runs over the backplane. Calibration and production data (BIS, Bruker Board Information System) are stored in a EEPROM flash on the board.

A vital element of any RF receiver is the quality of the shielding to maximize the suppression of noise. In the design of this unit special attention has been paid to good clean signal transmission etc. The AQS RXAD is mounted in a 19" RF cassette type case, the quadrature module is temperature stabilized separately.

All communication with the AQS RXAD take place using the SBSB1 link along the backplane. This enables the application of the UniTool which is a software diagnostic tool and is also used for accessing other devices like SGU or HPPR/2.

In contrast to the RX22, the AQS RXAD is also initialized and supervised by the AQS controller (DRU or SGU) using the separate internal RS485 bus on the AQS User Bus.

In multi receiver systems each channel is equipped with a separate AQS RXAD and DRU and its SGU for LO (local oscillator) signal generation.

Functions/Description *8.2*

The AQS RXAD has four main functions, which are to amplify the signal from the sample/HPPR, to down convert it, to match the input range of the ADC and digitize the quadrature signal. The vital elements of this are the linear amplification of all frequencies as well as to guarantee the precise phase relationship of all RF signals.

The RF input is amplified in several stages to increase the dynamic range. The current LO frequency for the first mixer stage is generated in the LO frequency synthesizer.

At the final section the IF signal is split into two channels with phase difference of 90 degrees, a standard method well known as quadrature detection. In order to ensure that the two channels provide identical amplification, slight adjustment to the phase and gain of these channels may be necessary. This can be done via UniTool. Channel A and B are connected directly to the integrated ADC.

The integrated ADC converts the quadrature signal at a very high sampling rate and transmits the data to the AQS DRU over a high speed data link on the backplane.

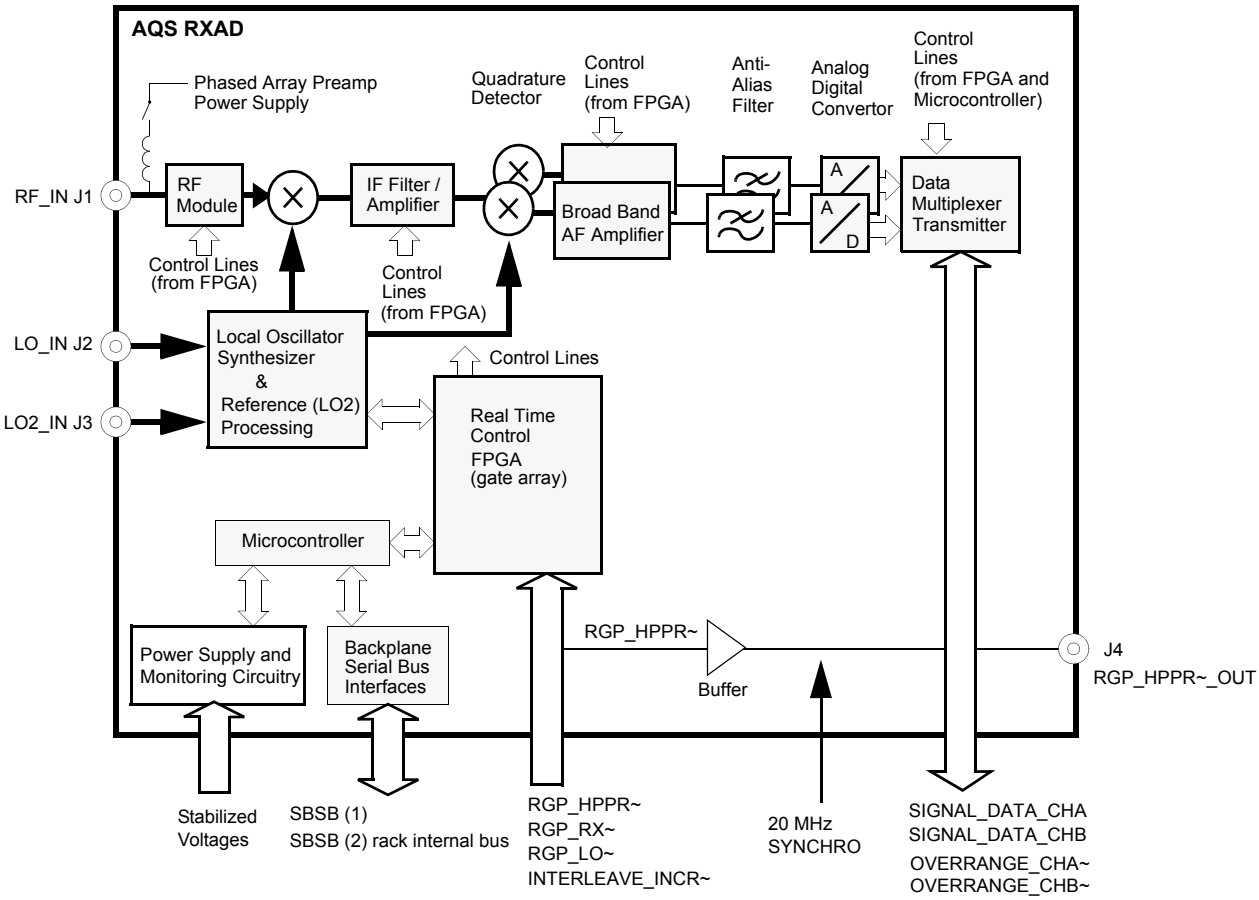
DC offset is pre-adjusted for proper control of the ADC input range and can be fine-adjusted using UniTool. The adjusted values can be saved in the on-board non-volatile memory.

During acquisition full control of the RXAD sections (gain, frequency, sampling etc.) is maintained by two complex FPGA (field programmable gate array) that handles the real-time behavior. The FPGA real-time circuitry is controlled by external gating and pulse signals from the backplane (AQS/2 User Bus). Control information is passed on from the IPSO and the actual Observe-SGU in order to the channel concept.

The on-board microcontroller is used for initialization and RS485 communication.

For multi receiver systems with several preamplifiers, the gating pulse for the HPPR (RGP_HPPR~) from the backplane is buffered and is fed separately to the front panel of the AQS RXAD (RGP_HPPR~_OUT J4).

Figure 8.1. RXAD-Blockdiagram



Power Supply and Monitoring *8.2.1*

All voltages supplied from the backplane are filtered and stabilized on the RXAD. Operation of the *on-board* power stabilization is monitored and indicated by the green LED on the front labeled POWER. If one of the AQS power supply voltages used by the AQS RXAD fails the monitoring circuit will turn the LED off.

Reset *8.2.2*

The AQS RXAD controller is normally in sleep mode (reset state) to prevent disturbance and spikes in the spectra. The 20 MHz microprocessor clocking frequency is also switched off. The controller will be restarted each time a communication via the RS485 is opened (TOPSPIN or UniTool).

The controller will be active during acquisition only in the following cases:

- ‚gs'-mode operation (which is typically used to adjust parameters dynamically) and
- at the beginning of wobble and receiver gain adjustment (rga)

This state is indicated by a ***blinking*** red LED labeled ERROR while the green LED labeled READY ***remains on***.

The AQS RXAD is mainly controlled from the backplane by the following pulses

- RGP_LO~
- RGP_RX~
- INTERLEAVE_INCR~

RGP_LO~

The RGP_LO~ pulse indicates that the LO signal from the SGU is available and so the LO synthesizer of the AQS RXAD can synchronize. If there is a RPG_LO~ pulse and no appropriate LO signal (defective cable, not connected, wrong setting of SGU) an error message will appear.

RGP_RX~

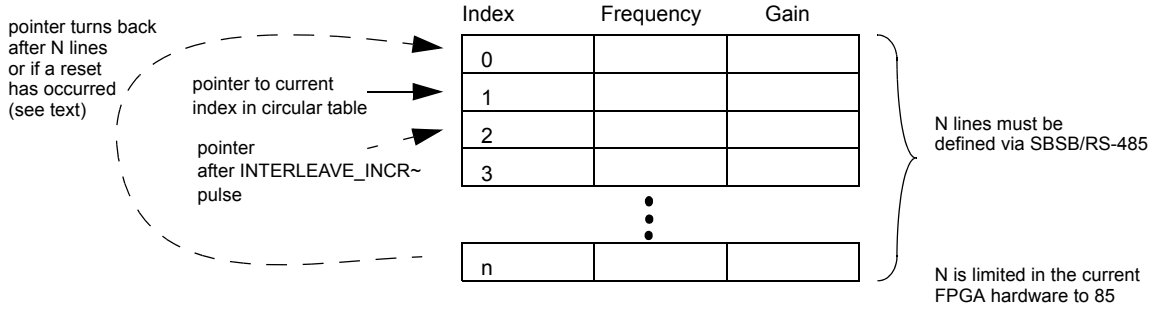
The RGP_RX~ pulse opens the receiver after excitation and prevents saturation of the input stage while transmitters are switched on. An RGP_RX~ pulse occurrence while the on-board microcontroller is running will also lead to an error message (except in ‚gs'-mode operation) because microcontroller circuitry noise might affect the spectral purity of the RF signals.

INTERLEAVE_INCR~

The receiver is prepared for pre-loading a table of different frequency/gain pairs. An INTERLEAVE_INCR~ pulse selects the next line of the table.

This concept is used for wobble, interleaved acquisition experiments and fast receiver gain ('rg') switching.

Figure 8.2. Circular Table: Mode of operation



*For **RXAD1000** ECL02.00 or newer and **RXAD-BB** ECL03.00 or newer:*

The pointer in the circular table resets to index 0 if a long ($\geq$ 4 μs) INTERLEAVE_INCR~ pulse has occurred. A short pulse ($\leq$ 1 μs) selects the next line of the table.

Effective Gain of the AQS RXAD *8.2.4*

Table 8.1. Possible gain steps of the AQS RXAD

Receiver Gain 'RG'	Equivalent RX-BB/RX-22 Voltage Gain [dB] $20*\log([V_{HR\_OUT}/V_{RF\_IN}])$		Receiver Gain 'RG'	Equivalent RX-BB/RX-22 Voltage Gain [dB] $20*\log([V_{HR\_OUT}/V_{RF\_IN}])$	Receiver Gain 'RG'	Equivalent RX-BB/RX-22 Voltage Gain [dB] $20*\log([V_{HR\_OUT}/V_{RF\_IN}])$
2050	78	see footnote a	90.5	51	4.50	25
1820	77		80.6	50	4.00	24
1620	76		71.8	49	3.56	23
1440	75		64.0	48	3.20	22
1150	73		57.0	47	2.80	21
1030	72		50.8	46	2.56	20
912	71		45.2	45	2.25	19
812	70		40.3	44	2.00	18
724	69		36.0	43	1.78	17
645	68		32.0	42	1.60	16
575	67		28.5	41	1.40	15
512	66		25.4	40	1.28	14
456	65		22.6	39	1.12	13
406	64		20.2	38	1.00	12
362	63		18.0	37	0.89	11
322	62		16.0	36	0.80	10
287	61		14.2	35	0.70	9
256	60		12.7	34	0.64	8
228	59		11.3	33	0.56	7
203	58		10.0	32	0.50	6
181	57		9.00	31	0.44	5
161	56		8.00	30	0.40	4
144	55		7.12	29	0.35	3
128	54		6.35	28	0.32	2
114	53		5.60	27	0.28	1
101	52		5.00	26	0.25	0

a Maximum receiver gain value can be set by UniTool to either RG 203 or optional to RG 2050.

Unit Configuration / Version / Jumpers 8.3

There are four versions of RXAD available (see ***"Part Numbers" on page 170***).

Key specifications and digital control behavior remain the same for all versions.

There are no jumpers or manual switches to set.

Through the ‘cf’ routine the number and location of all installed RXADs is determined. In multi receiver systems each RXAD in the AQS chassis has a unique address derived from its physical position.

Differences to previous receiver versions 8.3.1

The AQS RXAD is different from the RX22 in many ways:

- very low dead-time to switch on receiving (RXAD-BB)

- matching AQS reference unit necessary

- broadband suitability (RXAD-BB)

- service access with UniTool instead of RX22 Tool

For solids experiments, the AQS RXAD-BB replaced the SE-451 system:

- now more than 3 channels available

- phase modulation with SGU

- integrated in AQS concept

The difference to AQS RX in AV systems with RCU:

- Integrated ADC and level matching circuits

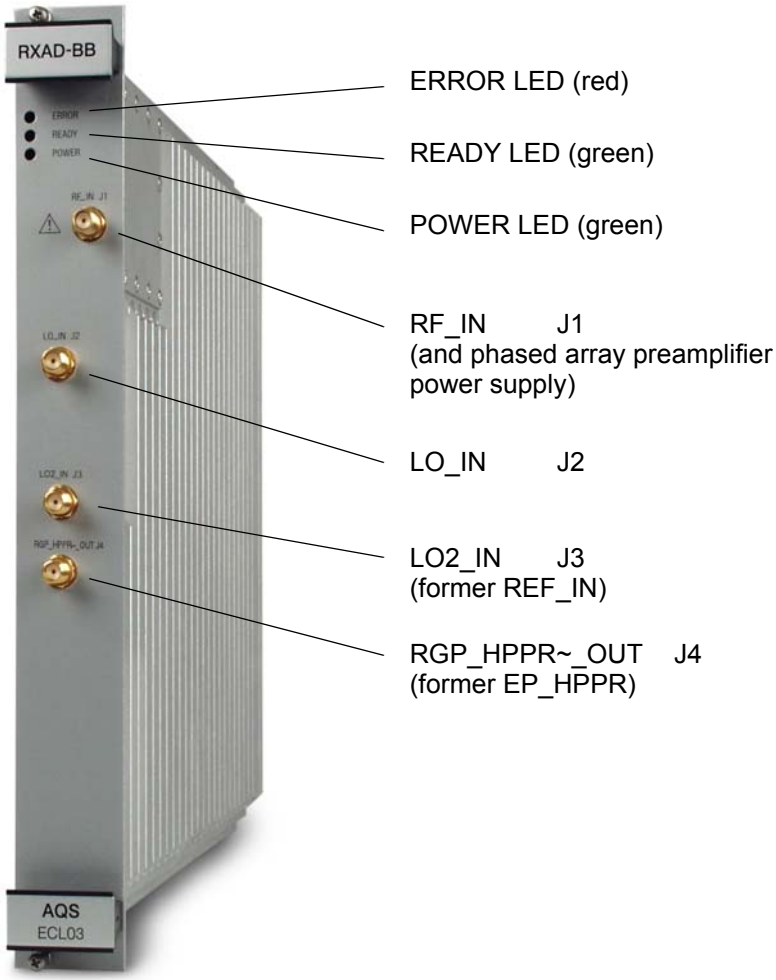
- additional connector for digital output data (on backplane)

Differences to previous ECLs

- RXAD1000 ECL02.00 and RXAD-BB ECL03.00:
  - Phased array preamplifier power supply on RF_IN (J1) → see ***"J1 RF_IN" on page 169***
  - The pulse width of INTERLEAVE_INCR~ affects the changes in the frequency/gain-table. → see ***"INTERLEAVE_INCR~" on page 164***

Front Panel Wiring / Display *8.4*

Figure 8.3. AQS RXAD front panel



LED Display *8.4.1*

The table below summarizes the states of the three front panel LEDs.

Table 8.2. LED States

ERROR (red)	READY (green)	POWER [a] (green)	Description
-	-	off	- Power supply switched off or operating incorrectly
off	on	on	- **Normal sleep mode** - Microcontroller asleep (no spectral spikes due to microcontroller circuitry) - No communication is possible with the RXAD.
off	on resp. short-time flickering [b]	on	- Ready for operation (microcontroller awake) - Communication with the RXAD is possible.
off	blinking (data stream)	on	- Communication LED The unit has received a command from the RS485 bus master. The READY LED switches off and as soon as the RXAD acknowledges the command the READY LED is switched on again.
blinking slowly (approx. 3 Hz)	on [b]	on	- Indicates warning and not error (‘gs’ mode). Caution: Sensitive NMR experiments are not possible in this mode due to disturbances of the controller system.
blinking slowly (approx. 3 Hz)	off	on	- An error has occurred on the RXAD
blinking fast	-	on	- Boot-mode Board not initialized yet or no application firmware found (e.g. because of power failure during firmware update).

a The power LED indicates that **all** necessary voltages are present and at the correct level. If any voltage level drops then the LED will go out. Thus once the power LED lights, further investigations on the backplane to check the precise voltage are unnecessary.

b The flickering LED indicates the active microcontroller (from firmware „rxs_ap.hex“ and later; previous firmware does turn on the LED permanently).

J1 RF_IN

Input (receive signal) from HPPR. This is a RF signal which will only be present when the HPPR is in receive mode. The timing is controlled by the RGP_HPPR signal which is closely linked to the AQS RXAD gating signal (RGP_RX~).

*For **RXAD400/600/1000** ECL02.00 to 03.00 and **RXAD-BB** ECL03.00 to 04.00:*

In addition to the receiving signal, this port supplies also a switchable phased array preamplifier power source. If switched on, a 14 V_{DC} voltage will appear on this connector (if a regulated 10 V_{DC} supply is required use a higher ECL or the ***"MRI Array-Preamp Supply 10V"*** – see ***page 186***). If anything but a suitable phased array preamplifier is connected to it, permanent damage may occur to the connected device.

After system power up the phased array preamp power supply is always turned off. It must be switched on prior to every use by a software command.

The phased array preamp power supply is protected against short circuit and will recover automatically after removing the overload condition. The maximal DC-current of the phased array preamplifier must not exceed 70 mA for proper supply voltage.

*For **RXAD400/600/1000** ECL04.00 or higher and **RXAD-BB** ECL05.00 or higher:*

The phased array preamp power supply voltage has been reduced to 10 V_{DC} to meet the requirements of the new MRI phased array preamps. All other characteristics stay the same as above mentioned.

J2 LO_IN

RF CW signal with frequency of SFO1 + f_{DQD} from SGU. This signal ($1V_{pp}$ at 50 Ω) originates from the observing SGU (LO generating SGU) and is only present when the RXAD is receiving.

The LO signal is routed in a chain through all SGUs and is fed from the most right SGU (connector LO OUT J4) to the RXAD – see also wiring principle.

***J3 LO2_IN** (former REF_IN)*

Detector reference frequency (local oscillator signal 2) from AQS Reference Board (REF) LO2 J5.

***J4 RGP_HPPR~_OUT** (former EP_HPPR)*

Buffered gating pulse (RGP_HPPR~) from backplane, used for preamplifiers in multi receiver systems.

Part Numbers 8.5

- Z102116 RXAD400 (5...432.5 MHz)
- Z102117 RXAD600 (5...647.5 MHz)
- Z102118 RXAD1000 (5...1072.5 MHz)
- Z102119 RXAD-BB (BB option, 5...1072.5 MHz)

Troubleshooting / Unit replacement / Tips 'n' Tricks 8.6

General 8.6.1

1. Do not open the AQS RXAD in the field (calibration void).
2. Ensure the AQS Reference Board unit is **not** labeled with REF22-400, REF22-600 or REF22-1000. The AQS REF must be a REF400, REF600 or REF1000 type.
3. To replace the unit simply switch off the AQS chassis, replace the board and switch the chassis on. Having inserted a new AQS RXAD the spectrometer should be reconfigured ('cf') and the entry in the file `uxmnr.info` checked.
4. RF signals are all AC coupled[1] and the overall input resp. output impedance is 50 Ω. (Please note: The SMA-connector nuts must not be tightened more than to a torque of 45Ncm.)

Download new AQS Receiver (RX) Firmware 8.6.2

1. Check if the directory (/Bruker/<`xwinnmr/topspin release`>/conf/instr/servtool/UniTool/files/birds) exists. Otherwise create it.
2. Copy the new firmware e.g. **rxs**_ap.hex into the directory Bruker/<`xwinnmr/topspin release`>/conf/instr/servtool/UniTool/files/birds
3. Open a shell or the command prompt in the BRUKER Utilities folder when using Windows.
4. Start the UniTool: `xwinnmr -e UniTool or topspin -e UniTool`
5. -> `aqs`, confirm
6. -> decimal address for RX-1 is **`16`**, confirm
7. When the UniTool Menu is loaded, enter `<4> Auto Download` -> download is started. The download takes about 22 minutes
8. If you have more than one RX, do the same as above with address **`17, 18,`** and so on.

1 Except RF_IN (J1) → see ***"J1 RF_IN" on page 169***

Error Messages *8.6.1*

Description of possible error messages:

Table 8.3. AQS RXAD error messages (Release AR)

Error No.	Error Message	Description	Possible cause
Error No. 1	Serial RS485 time-out	slave device did not answer in expected time	slave device probably not initialized, check connections
Error No. 4	Serial RS485 command, checksum error	RS485 protocol violation	spectrometer control software failure
Error No. 8	checksum error on INTRA bus		
Error No. 10	RAM Selftest Error	RAM test failed	hardware failure
Error No. 11	No application firmware found	no application firmware found	hardware failure or firmware download failed
Error No. 13	**Power failed**	**indicate that a power up has occurred and the system is not initialized**	**ordinary power up or a power breakdown during an experiment**
Error No. 15	Parameter exceeds valid range	value out of range	spectrometer control software failure or faulty input using Unitool
Error No. 16	Unknown board hardware version	this hardware version has never been delivered	firmware or hardware error on RXAD
Error No. 17	Function not supported by board hardware version		RXAD with newer ECL required
Error No. 18	Unknown version index in configuration page	internal validation of calibration data failed	hardware error
Error No. 19	BIS checksum error		
Error No. 20	Syntax error	selected feature not supported by actual firmware, board does not understand command	spectrometer control software failure, wrong board selected, hardware feature not supported by actual version
Error No. 21	Command not availabe for this HW version		RXAD with newer ECL required
Error No. 22	RTX create error	operating system error	firmware or hardware error on RXAD
Error No. 23	RTX memory allocation error		
Error No. 24	RTX memory free error		
Error No. 25	RTX communication pool exhausted		
Error No. 26	RTX send signal error		
Error No. 27	RTX interrupt handling error		
Error No. 28	RTX semaphore waiting list full		
Error No. 29	RTX pool create error		

Table 8.3. AQS RXAD error messages (Release AR)

Error No.	Error Message	Description	Possible cause
Error No. 35	Download done correctly, but board not initialized, restart AQS when downloading has finished		
Error No. 36	Flash Byte Program Error	failure during FLASH memory programming	hardware error
Error No. 37	Flash Erase Error		
Error No. 40	Flash Erase Timer expired		
Error No. 41	Error in Flash Command Sequence		
Error No. 42	Flash Page mismatch, storing terminated		
Error No. 43	calibration data invalid		
Error No. 50	RAM selftest error	RAM test failed	hardware failure
Error No. 51	no app firmware found (wrong FW checksum)	RAM test failed	hardware failure
Error No. 52	no app firmware found (wrong FW name)	RAM test failed	hardware failure
Error No. 53	no app firmware found (wrong FW id)	RAM test failed	hardware failure
Error No. 56	boot can't be forced to sleep, please download application firmware first		no application firmware is loaded
Error No. 57 (54)	Wrong filename, expected '.. rxs_ ...'		
Error No. 58	Corrupt BIS on board	BIS (Board Information System) test failed	hardware failure
Error No. 59	BIS checksum error	BIS (Board Information System) test failed	hardware failure
Error No. 60	Unknown rack code		
Error No. 61	Board Number exceeds valid range		
Error No. 100	Serial DAC bus (SPI, 8420) error		
Error No. 101	Serial ASIC bus (JTAG) error		
Error No. 102	Missing valid configuration page	configuration data (calibration data) not available	hardware failure
Error No. 105	Flash table does not exist, using default table	configuration data (calibration data) not available	hardware failure
Error No. 107	Table address or identifier out of range		
Error No. 128	input value out of range	entered input value out of range	spectrometer control software failure or faulty input using Unitool

Table 8.3. AQS RXAD error messages (Release AR)

Error No.	Error Message	Description	Possible cause
Error No. 129	Error in LO generation (coarse tuning)	LO synthesizer was not able to set its frequency correctly	hardware failure
Error No. 130	Error in LO generation (VCO gradient fail)		
Error No. 131	**Error in LO generation (PLL lock lost)**	**LO synthesizer was not able to set its frequency correctly**	**LO IN cable from SGU not connected REF IN cable from REF not connected spectrometer control software failure**
Error No. 133	Wrong RF-switch value	faulty input using Unitool	faulty input using Unitool
Error No. 134	Wrong IF-switch value		
Error No. 135	Wrong AF-switch value		
Error No. 136	Wrong PLL-gain-adjust value		
Error No. 137	Wrong PLL-level value		
Error No. 138	Enable/Disable expected		spectrometer control software failure or faulty input using Unitool
Error No. 139	No oscillator selected	faulty input using Unitool	faulty input using Unitool
Error No. 140	**Power Diagnostic failed**	**on-board diagnostic detected faulty power supply voltages**	**check power LED on AQS RXAD and other AQS boards to determine if AQS RXAD hardware failed or fuses on the power supplies need to be exchanged**
Error No. 141	**RGP_RX-Error occurred**	**receiver has been gated while the on-board microcontroller was running – spectra may show spikes**	**spectrometer control software failure**
Error No. 142	Frequency invalid		spectrometer control software failure or faulty input using Unitool
Error No. 143	Gain invalid		
Error No. 144	Gain distribution scheme not found		hardware failure
Error No. 145	Gain table not found		
Error No. 146	PLL table not found		
Error No. 147	VCO gradient too low		
Error No. 148	VCO gradient too high		
Error No. 149	I2C bus fail		
Error No. 150	wrong IF-gain-adjust value		faulty input using Unitool
Error No. 151	wrong gain distribution table-index		faulty input using Unitool
Error No. 152	invalid row number in loop-table		spectrometer control software failure or faulty input using Unitool
Error No. 153	invalid amount of rows in loop table		

Table 8.3. AQS RXAD error messages (Release AR)

Error No.	Error Message	Description	Possible cause
Error No. 154	Wrong PLL-tune value		faulty input using Unitool
Error No. 155	On/Off expected		spectrometer control software failure or faulty input using Unitool
Error No. 156	Frequency too high for this type of RX		
Error No. 157	DC offset correction table full, offset setting is stored temporally only		too many entries in the dc offset correction table
Error No. 158	DC offset correction table can't be deleted - delete DC offset correction table in RAM then save config		faulty input using Unitool
Error No. 159	No ADC board available		
Error No. 160	Command not accepted while RF input is disabled, init RX/RXAD first		RF input was disabled via Disable-RF-Input-Command

Diagnostic Tests *8.7*

The AQS RXAD has no special written diagnostic program. The AQS RXAD can be accessed with the UniTool that is accessible from BRUKER Utilities:

With UniTool you can

1. read and write the AQS RXAD receiver gain
2. adjust the gain, phase and baseline for the quad module
3. adjust DC offset
4. measure the quad module temperature
5. read actual firmware version, ECL and hardware version
6. download new firmware

Be aware that UniTool is a hardware level tool and improper operation may void the calibration data. UniTool should be used by service personnel only.

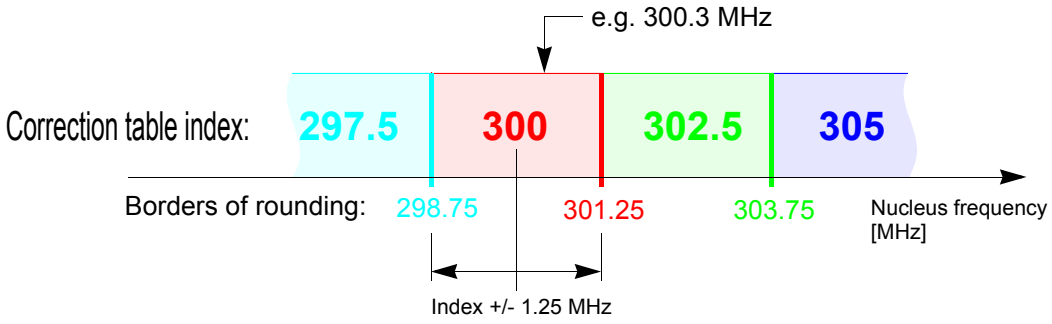
DC Offset and Quadrature Correction Table *8.8*

The DC offset of the AQS RXAD variants running with TOPSPIN can be adjusted by software and stored in the on-board FLASH non-volatile memory. The offset values are handled for each frequency/gain pair and will automatically be adjusted each time the receiver gain (rg) or the observe frequency (the nucleus) is changed.

! ***NOTE: The frequency value in the correction table is rounded to the next 2.5 MHz index-step (see Figure 8.4.). As a consequence of this rounding, a drifting magnet can cause a nucleus frequency to fall into another 2.5 MHz***

index-step where the RXAD is not adjusted. In this case a readjustment is necessary.
(This difficulty can occur in unlocked magnet systems only. In locked magnet systems the nucleus frequency does not drift away.)

Figure 8.4. Rounding of the frequency in the Correction Table



If quad image gain/phase adjustment is necessary (initial quad image in qsim mode is factory preadjusted), do that ***before adjusting DC offset***. See chapter ***8.9 "Quadrature Phase/Gain Adjust / Useful Pulse Programs"***

To fill a DC offset correction table you have to do a ‘gs’-experiment with TOPSPIN. Be sure TOPSPIN has selected the nucleus/frequency you want to adjust the DC offset correction for.

! ***Set the following environment variable (in TOPSPIN command line):***

```
env set TOPSPIN_DC_CORRECTION=no
```

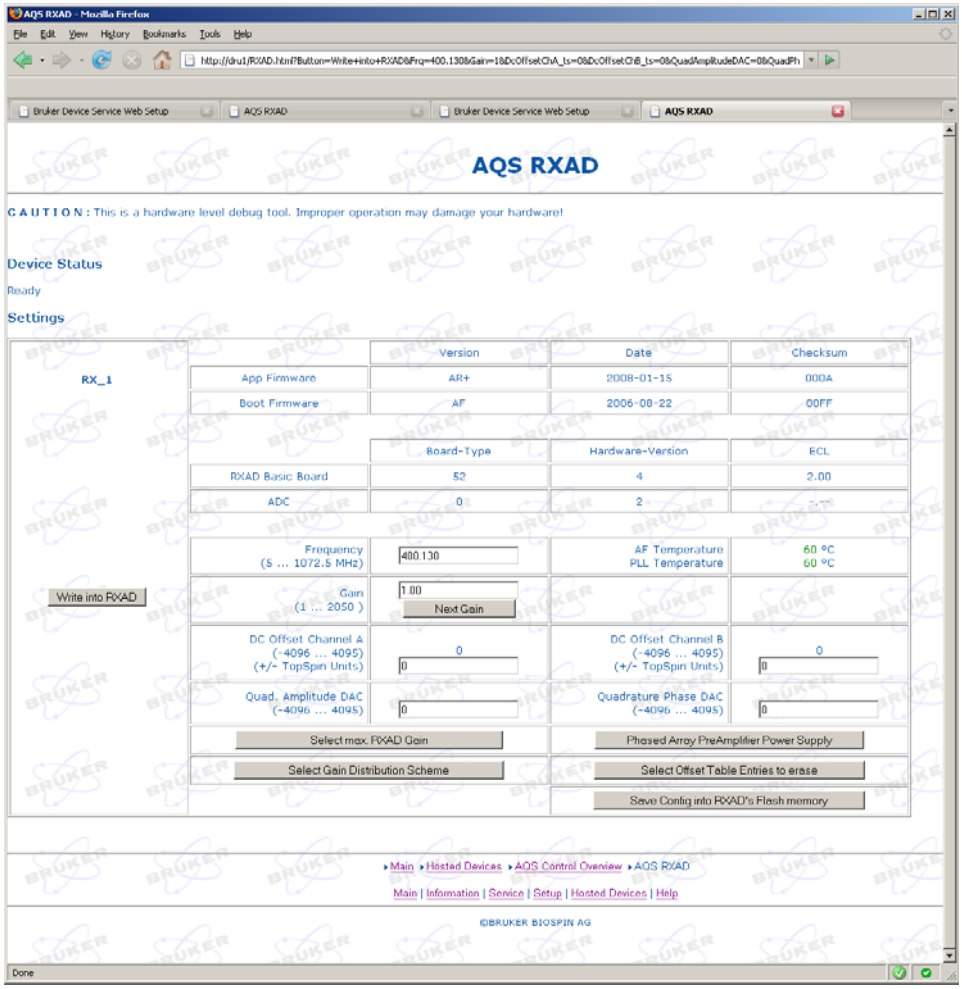
(or run the following au-program: `dccorr off`)

After selecting an experiment choose TOPSPIN‘s acquisition window (fid) to see the time domain signal and select `Unsh` (`Unshuffle` Symbol) to see both channels.

Set the AQ_mod (Acquisition mode) in the acquisition parameters (eda, AcquPars) to **qsim**.

Start your web browser (Internet Explorer, Mozilla Firefox, ...), type ‘dru1‘ (respectively 149.236.99.89) into the URL field and hit <Enter>. Branch into --> ‘Hosted Devices‘ --> ‘AQS Overview‘ --> ‘AQS RXAD 1‘

Figure 8.5. AQS RXAD website



The AQS rack must be powered on at least for 30 minutes to guarantee a stable temperature of the RXAD before adjusting any quad image or DC offset.

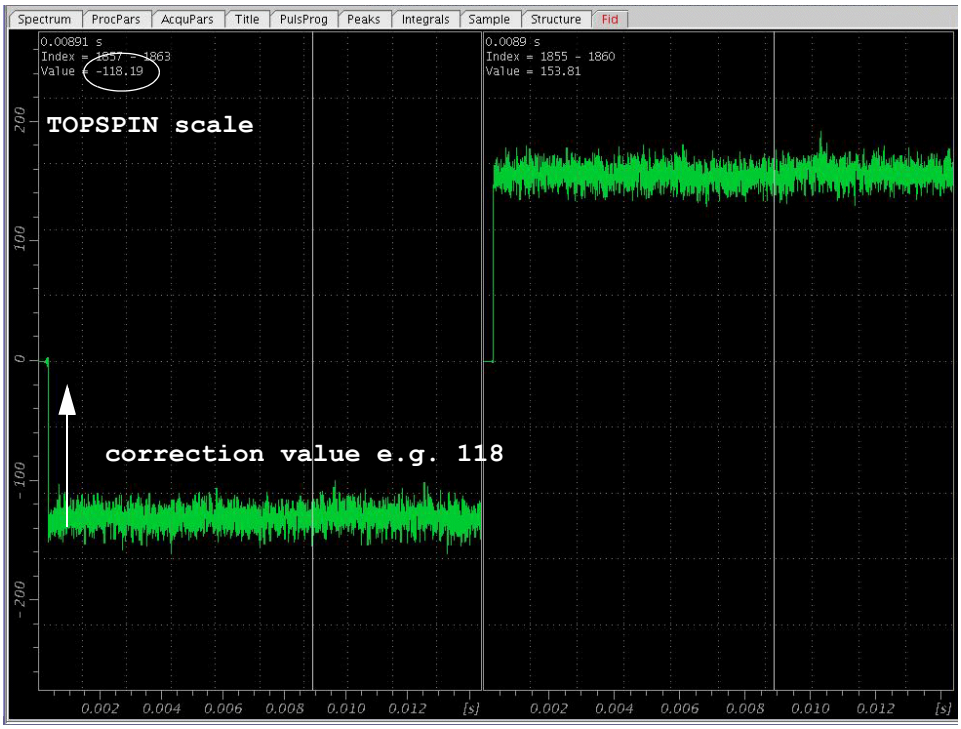
You can check the RXAD-temperature (AF and PLL). The temperature values should be written in green color (not red). The nominal temperature is 54 °C or 59 °C dependant on the internal hardware-version.

The ‘offset and quad image‘ table handles entries (max. 900 entries) which are stored according to the selected nucleus/frequency (in steps of 2.5 MHz) and the selected gain (in steps of 1 dB).

To adjust the table for the actual nuclid/frequency you must start with the lowest gain. Check the frequency to be correct (press F5 to refresh/reload if necessary) then fill in ‘`1`‘ into the Gain input field and press the ‘Write into RXAD‘-button.

To be sure the actual DC offset correction table in the random-access-memory (RAM) is empty for this nucleus/frequency start UniTool with the appropriate address, choose `[T] RX erase all OfsTableEntries of actual Frequency` in the main menu and `<y> yes`.

Figure 8.6. Example figure 1



The graph's left half of the TOPSPIN's y-axis shows the offset correction of channel A. If the graph's y-value is negative you have to enter that value positively to converge to zero offset. If the graph's y-value is positive enter the value negatively.

Fill in the 'DC Offset Channel A' input field (in this example 118) and press the button 'Write into RXAD'.

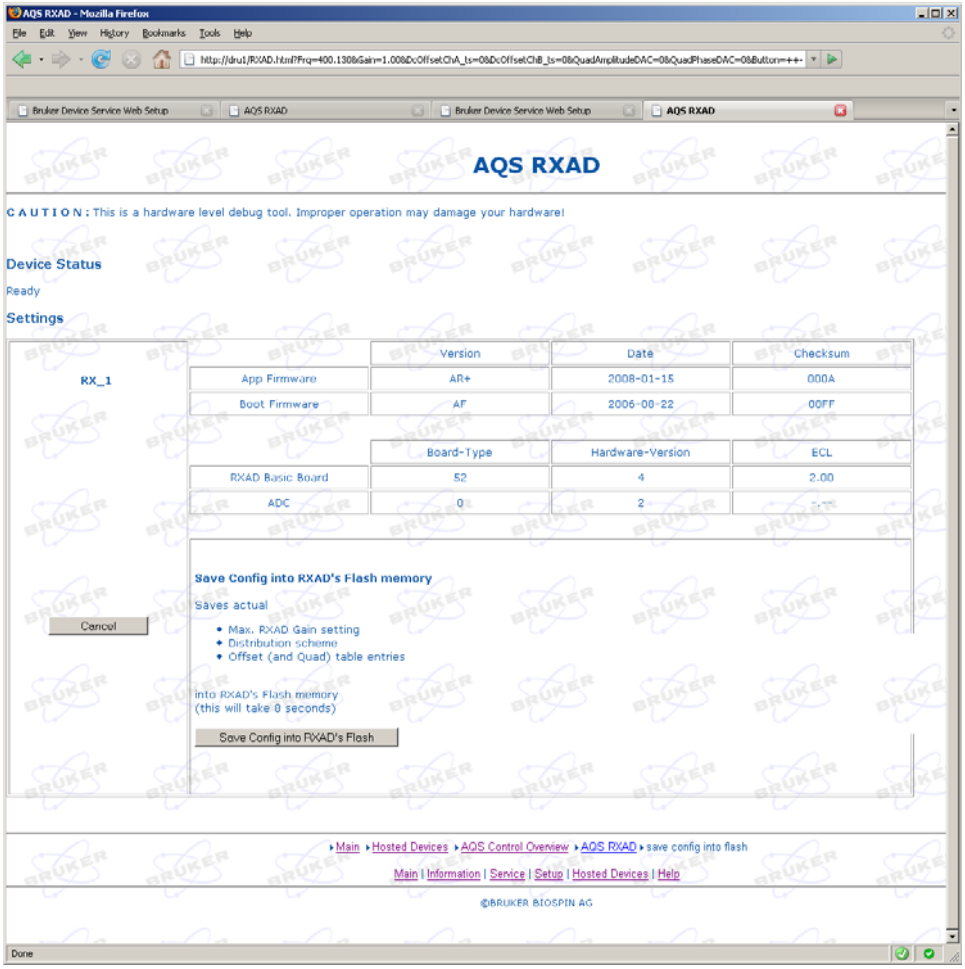
The controller on the RXAD will calculate the internal correction values needed. Repeat this once or twice and you will be within one percent of the uncorrected offset.

! ***There may be an inaccuracy between entered value and actually set correction due to scaling variation by chosen digital filter and SWH.***

The graph's right half of the TOPSPIN's y-axis shows you the offset correction of channel B. In this example fill in -153 into the 'DC Offset Channel B' input field and press the 'Write into RXAD'-button.

Repeat the whole procedure for the next gain by pressing the 'Next Gain'-button. Repeat 'Next Gain' until all gains are adjusted including the highest gain (= 203 respectively 2050).

If you don't want your table entries to be lost after a power down of the AQS-rack you need to save the RXAD configuration by pressing the 'Save Config into RXAD's Flash memory' button. You have to confirm in the following window. Confirming will take a few seconds.



Stop the TOPSPIN experiment, select the next nucleus/frequency you want to adjust and start another ‘gs’-experiment. Adjust in the same way as above...

! ***If you have finished DC offset correction reset the following environment variable (in TOPSPIN command line):***

```
env set TOPSPIN_DC_CORRECTION=yes
```

(or run the following au-program: `dccorr on`)

This will set the AQ_mod as it was before the adjustment.

Quadrature Phase/Gain Adjust / Useful Pulse Programs 8.9

For quadrature phase/gain adjustment the following pulse program is useful:

```
;zgcw.mod
;avance-version (04/02/08)
;1D sequence with CW decoupling
```

```
#include <Avance.incl>
"d11=30m"
1 ze
2 d11 reset:f1 reset:f2
  d11 pl26:f2
  d11 cw:f2 ph30
  d1
  p1 ph1
  go=2 ph31
  wr #0
  d11 do:f2
  exit
  ph1=0 2 2 0 1 3 3 1
  ph31=0 2 2 0 1 3 3 1
  ph30=0
  ;pl1 : f1 channel - power level for pulse (default)
  ;pl26: f2 channel - power level for cw decoupling
  ;p1 : f1 channel -  high power pulse
  ;d1 : relaxation delay; 1-5 * T1
  ;d11: delay for disk I/O [30 msec]
```

In `edasp` select two identical nucleus for F1 and F2 and set the offset frequency OFS2 of the second one to e.g. 1000.0 Hz

Figure 8.7. Example of eda for RXAD Quadrature Adjustment

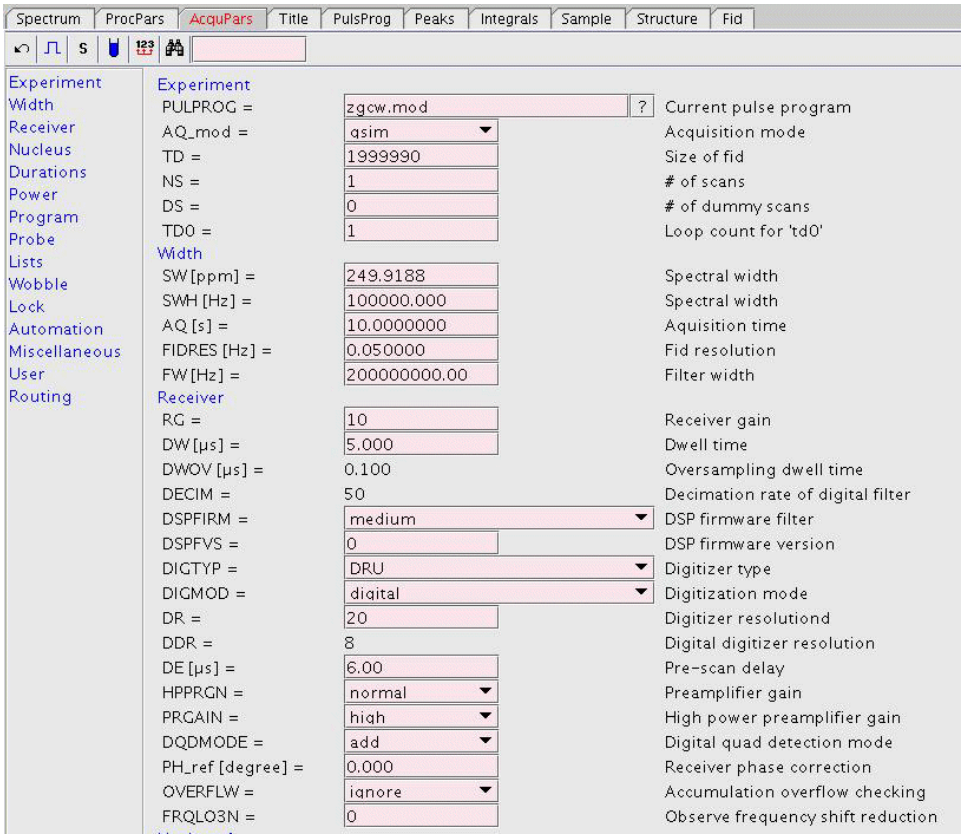
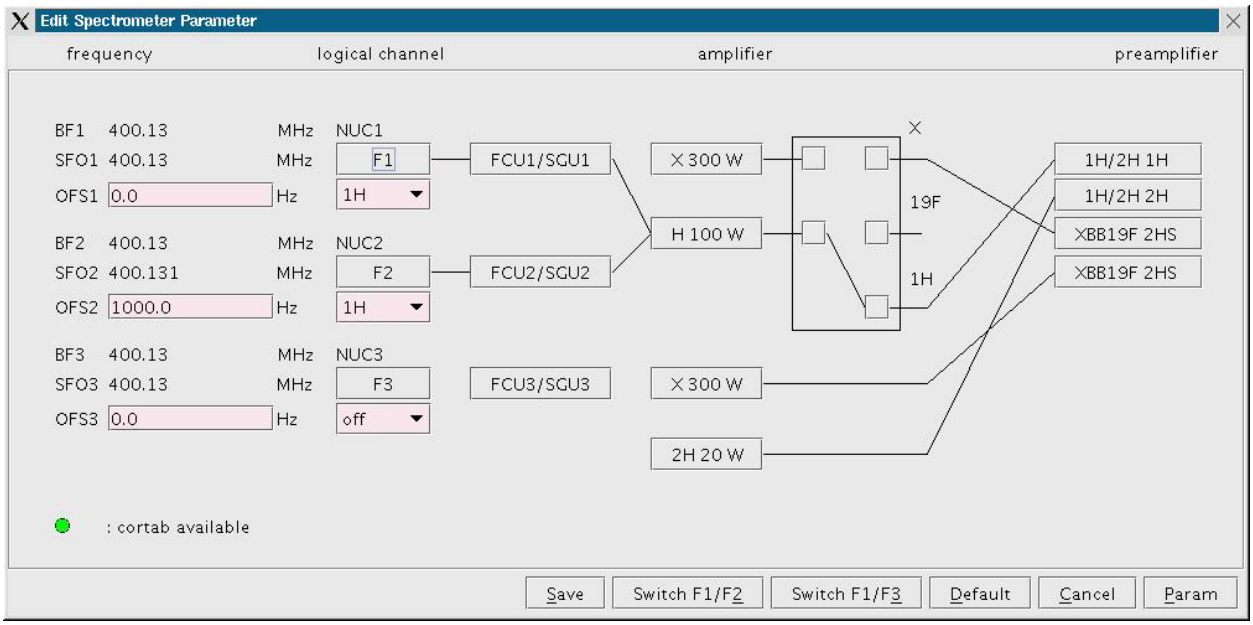


Figure 8.8. Proposed setup for quad image adjustment



Set `phmod` to `mc`.

Connect now the RF OUT of SGU2 with the RF IN of the RXAD directly and start acquisition in ‘gs’ mode (pl26 ≈ 40 dB).

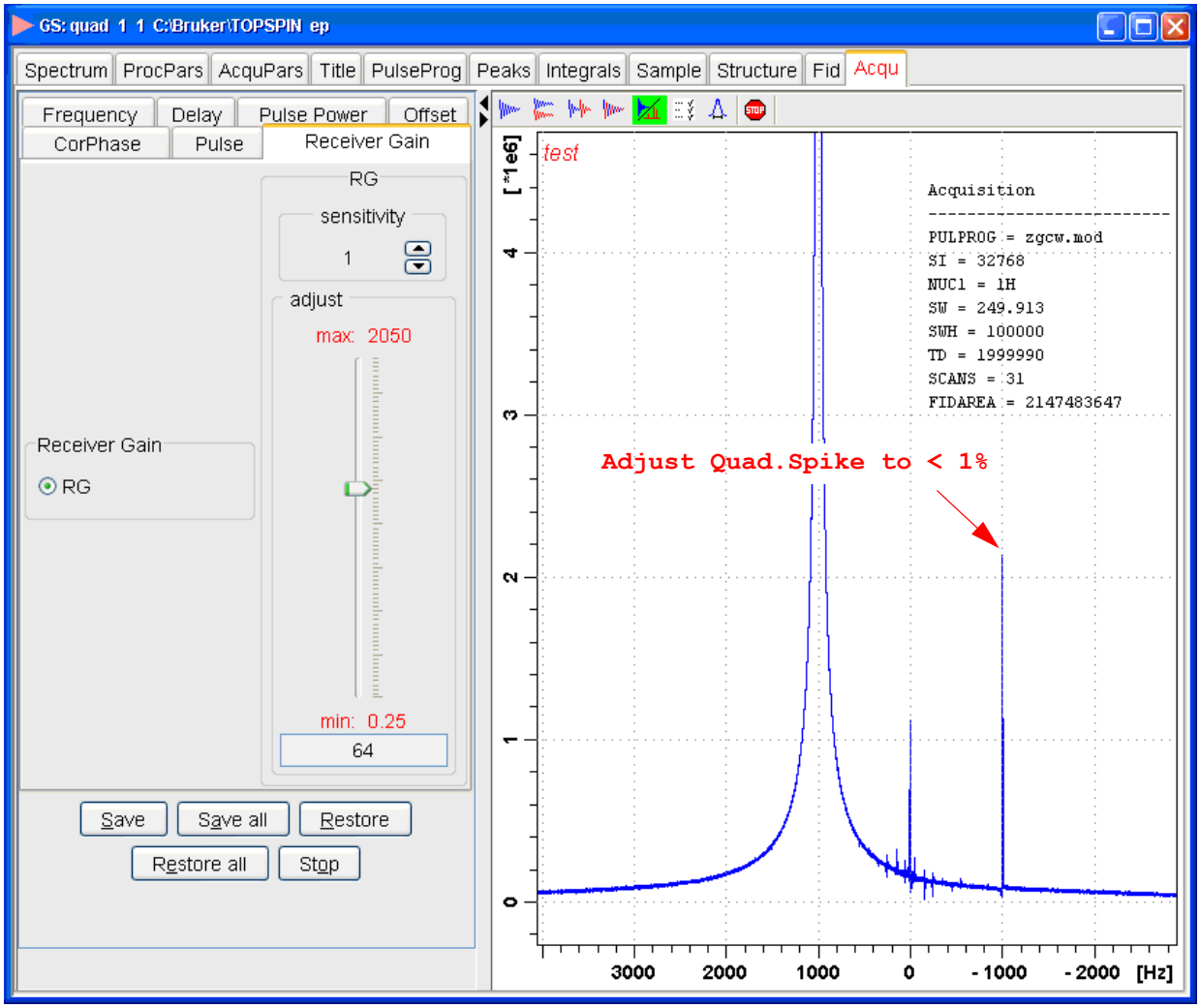
Check the input signal level in the acquisition window. Check for appropriate amplitude of the ADC and do not overdrive it.

Press in TOPSPIN the button „Execute realtime ft and show spectrum“ (Symbol) and adjust the quadrature image signal with the RXAD website.

The adjustment procedure is similar to that one for dc offset correction.

For phase/amplitude adjustments modify the ‘Quad. Amplitude DAC‘ and/respectively the ‘Quadrature Phase DAC‘ input field(s) and press the ‘Write into RXAD‘ button.

Figure 8.9. Example of Quadrature Adjustment



Specifications *8.10*

Frequency Range:

5...432.5 MHz (RXAD400)

5...647.5 MHz (RXAD600)

5...1072.5 MHz (RXAD-BB, RXAD1000)

Frequency Stability: This is governed by the stability of the crystal oscillator on the REF unit which is specified to 3 $x10^{-9}$/day and 1 $x10^{-8}$/year

Frequency Resolution: The local oscillator synthesizer in the AQS RXAD follows the SGU LO signal with its resolution of <0.005 Hz.

LO Phase Settling Time: 2 μs max. (RXAD-BB)

Audio Signal Settling Time: < 2 μs (RXAD-BB)

Gain:

Gain Range: 0...58 dB (linear 0.25...203), resolution 1 dB

ADC Resolution:

depends on oversampling rate on AQS DRU:

- up to 200 kHz bandwidth 20 bit
- up to 5 MHz bandwidth 16 bit

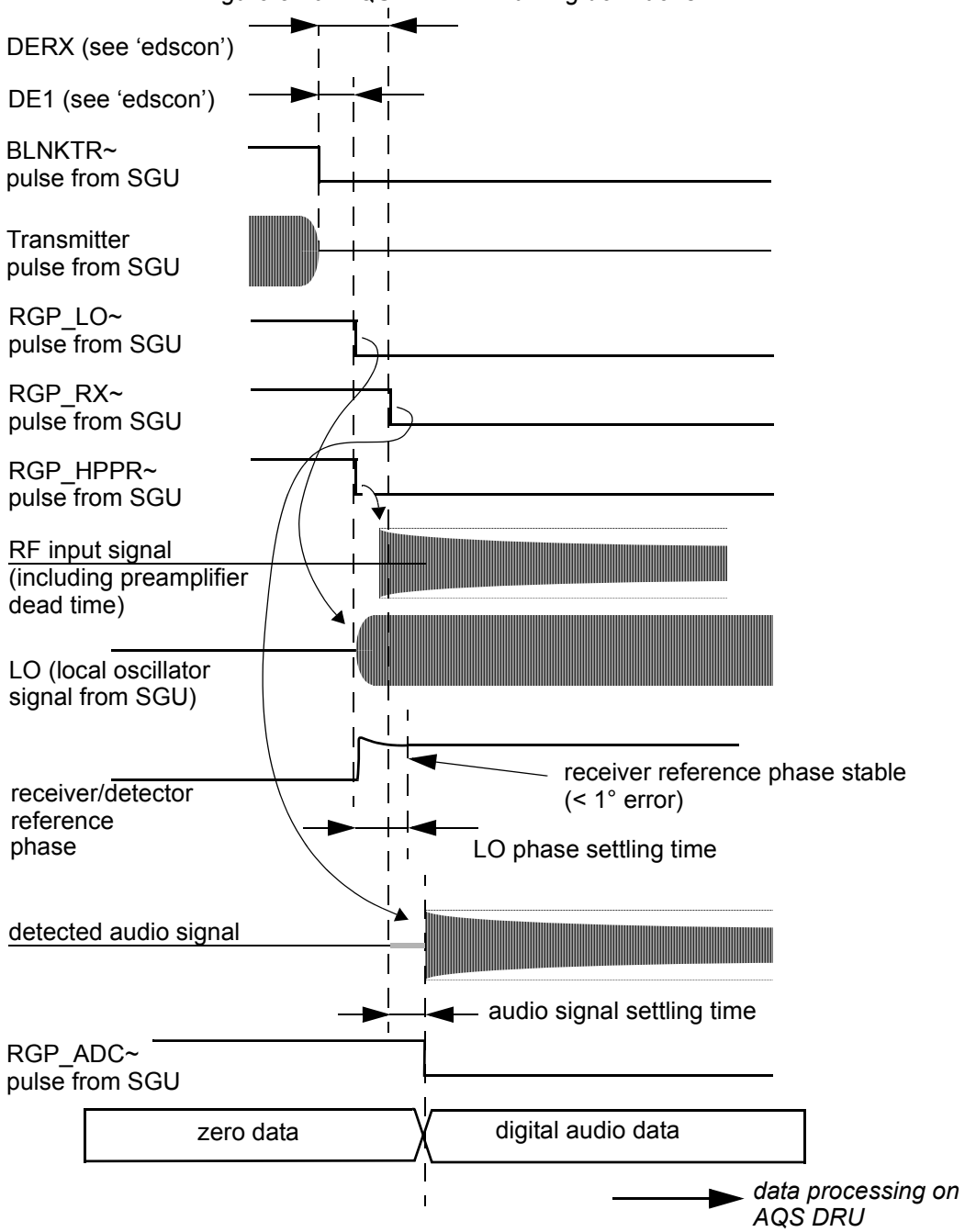
ADC Output Data Rate

28 bit / 20 Mwords per second (560 Mbit/s)

Timing Definitions *8.10.1*

Turn on or settling time of the AQS RXAD-BB are defined as follows:

Figure 8.10. AQS RXAD-BB timing definitions



Power Supply / Fuses *8.11*

See ***8.4.1***

Backplane Connector *8.11.2*

	z	a	b	c	d	e	f
1	GND	GND	RESERVE_1	NC	GND	SAMPLE_INFO0	GND
2	GND	NC	GND	SAMPLE_INFO3	SAMPLE_INFO2	SAMPLE_INFO1	GND
3	GND	GND	NC	RESERVE_2	GND	SAMPLE_INFO4	GND
4	GND	20MHZ_CLK_X	GND	INTERLEAVE_INCR~	ADC_SEL1	ADC_SEL0	GND
5	GND	GND	20MHz_CLK_X~	RESERVE_3	GND	RGP_LO~	GND
6	GND	BLNKTR1~	GND	BLNKTR2	RESERVE_6	RESERVE_4	GND
7	GND	BLNKTR3~	BLNKTR4~	NC	GND	RGP_ADC	GND
8	GND	BLNKTR5~	GND	BLNKTR6~	RESERVE_7	DWL_CLK	GND
9	GND	BLNKTR7~	BLNKTR8~	NC	GND	RGP_RX~	GND
10	GND	SBS_TTL_TX	GND	SBS_TTL_RX	SBS_TTL_TX_ENAB~	RESERVE_5	GND
11	GND	LOCAL_TX	LOCAL_RX	SBS_TTL_WUP~	GND	RGP_HPPR~	GND

red = CCU bus galvanically isolated
blue = Intra Rack Bus

Key Area

15	GND	SLOT2	SLOT1	SLOT0	GND	RESERVE_ADC_1	GND
16	GND	SLOT3	GND	I2C_SDA	RESERVE_ADC_2	GND	GND
17	GND	EMERGENCY_STOP	I2C_BUS_REQ	I2C_SCL	GND	ADC_I2C_SDA	GND
18	GND	NC	GND	I2C_2_SDA	I2C_2_SCL	GND	GND
19	GND	NC	NC	NC	GND	ADC_I2C_SCL	GND
20	GND	NC	GND	P2V	N2.5V	GND	GND
21	GND	P5V	P35V	P9V	P9V	P9V	GND
22	GND	P5V	RACK0	N9V	N9V	N9V	GND
23	GND	P5V	P19V	N19V	RACK1	P12V	GND
24	GND	P5V	P19V	N19V	RACK2	P12V	GND
25	GND	P5V	P19V	N19V	RACK3	P12V	GND

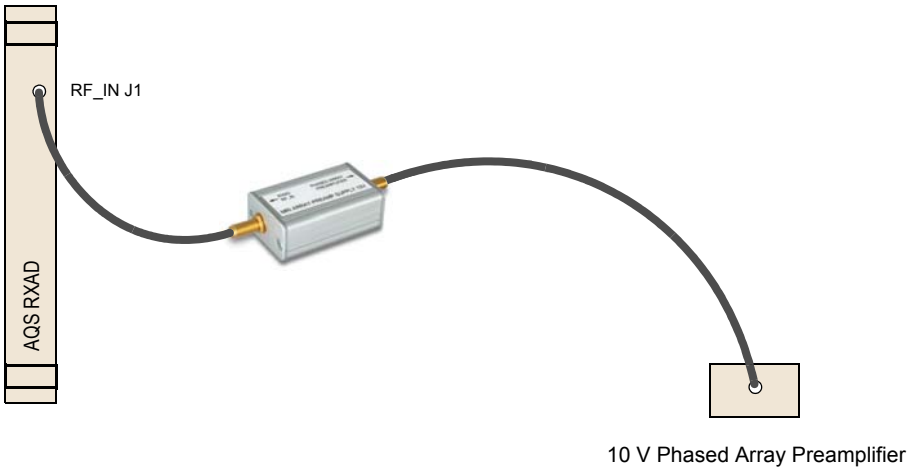
Table 8.4. RXAD extension connector

	z	a	b	c	d	e	f
1	GND	P5V	P5V	P5V	P5V	P5V	GND
2	GND	RESERVE_4	RESERVE_5	GND	RESERVE_3	GND	GND
3	GND	ADC_I2C_SDA	GND	L3_OPT	GND	LCLK_OPT	GND
4	GND	ADC_I2C_SCL	GND	L3_OPT~	GND	LCLK_OPT~	GND
5	GND	GND	L_CLK	GND	L_DATA_3	GND	GND
6	GND	GND	L_CLK~	GND	L_DATA_3~	GND	GND
7	GND	L_OVR0	GND	L_DATA_2	GND		GND
8	GND	L_OVR1	GND	L_DATA_2~	GND		GND
9	GND	GND	L_DATA_1	GND	L_DATA_0	GND	GND
10	GND	GND	L_DATA_1~	GND	L_DATA_0~	GND	GND
11	GND	RESERVE_0	GND	RESERVE_1	GND	RESERVE_2	GND

To run a 10 V MRI phased array preamplifier with a older **RXAD400/600/1000** ECL02.00 to 03.00 or **RXAD-BB** ECL03.00 to 04.00 it is essential to use a „MRI Array-Preamp Supply 10V“ converter box (P/N Z110658). The box transforms the 14 V_{DC} input voltage to a regulated 10 V_{DC} supply for the MRI preamplifier.

Do not use such a converter box for newer RXAD‘s (RXAD400/600/1000 ECL04.00 or higher or RXAD-BB ECL05.00 or higher). Those RXAD‘s already have the appropriate 10 V_{DC} supply voltage.

Figure 8.11. Wiring



AQS DRU 9

Introduction 9.1

The AQS DRU (Digital Receiver Unit) is a digital signal processing board implementing an enhanced digital receiver in comparison to the RCU introduced in 1994. It incorporates the digital mixing (LO3) stage for DQD and the ‚on the fly' digital signal processing block for a variety of digital filters within the AQS/2 receiver system.

To achieve a more flexible spectrometer integration (especially with extended multiple receiver systems), accumulation and data buffering is done on board. This allows for data transfer to the workstation to run across a commercial local area network (Fast Ethernet LAN). The omnipresent transfer control protocol / internet protocol (TCP/IP) is used to build the loosely coupled, standardized spectrometer environment, thus allowing flexible extensions in the future.

Distributed communication between the workstation and one or more DRU runs on common object remote broker architecture (CORBA). CORBA is a modern and reliable distributed object middle ware. By implementing a hardware- and operating system independent software interface, it allows in future to communicate with the DRU by any workstation topology (Intel architecture, SGI, etc.) and operating system (JAVA, .NET, etc.)

Diagnosis and servicing access to the DRU relies on hypertext transfer protocol (HTTP) and hypertext markup language (HTML), enabling service access just by any web browser (e.g. Netscape), without the need for special training of service people like the former UniTool.

The AQS DRU is enclosed in an aluminum metal case allowing seamless integration in the AQS chassis - concerning minimized RF interference and design.

The AQS DRU comes in two versions, the DRU and the DRU-E:

AQS DRU, P/N Z100977

This version includes interfaces for automatic tuning and matching (ATMA), probe identification and control system (PICS) and AQS integrated preamplifier modules. It will be mainly used for low field NMR systems.

This version does not include the very high speed interface (digital data output) and has not an expandable ADC word width facility for future RXAD.

A real-time pulse (RCP) input is used to switch the 2H preamplifier module transmit and receive switch according to the lock operation (TP_F0).

AQS DRU-E, P/N Z102520

This version includes a very high speed interface to stream the received data to further signal processing systems for applications requiring more than the 50MBit/s, e.g. for real time decision capability or just for user oriented dedicated solutions.

The protocol has not been defined yet but may be fixed later by downloading new firmware. Such protocols could be CameraLink™ or similar.

It also offers wider ADC data paths to the RXAD. This interface is prepared for the increased dynamic range of future AD converters.

This version does not include interfaces for ATMA, PICS or preamplifier modules. The HPPR/2 system is required for these purposes instead.

A real-time pulse (RCP) output is available to trigger future experiments upon acquiring NMR data (to be defined).

General Functions and Description *9.2*

The basic digital receiver concept of the DRU is designed to fulfill the following tasks:

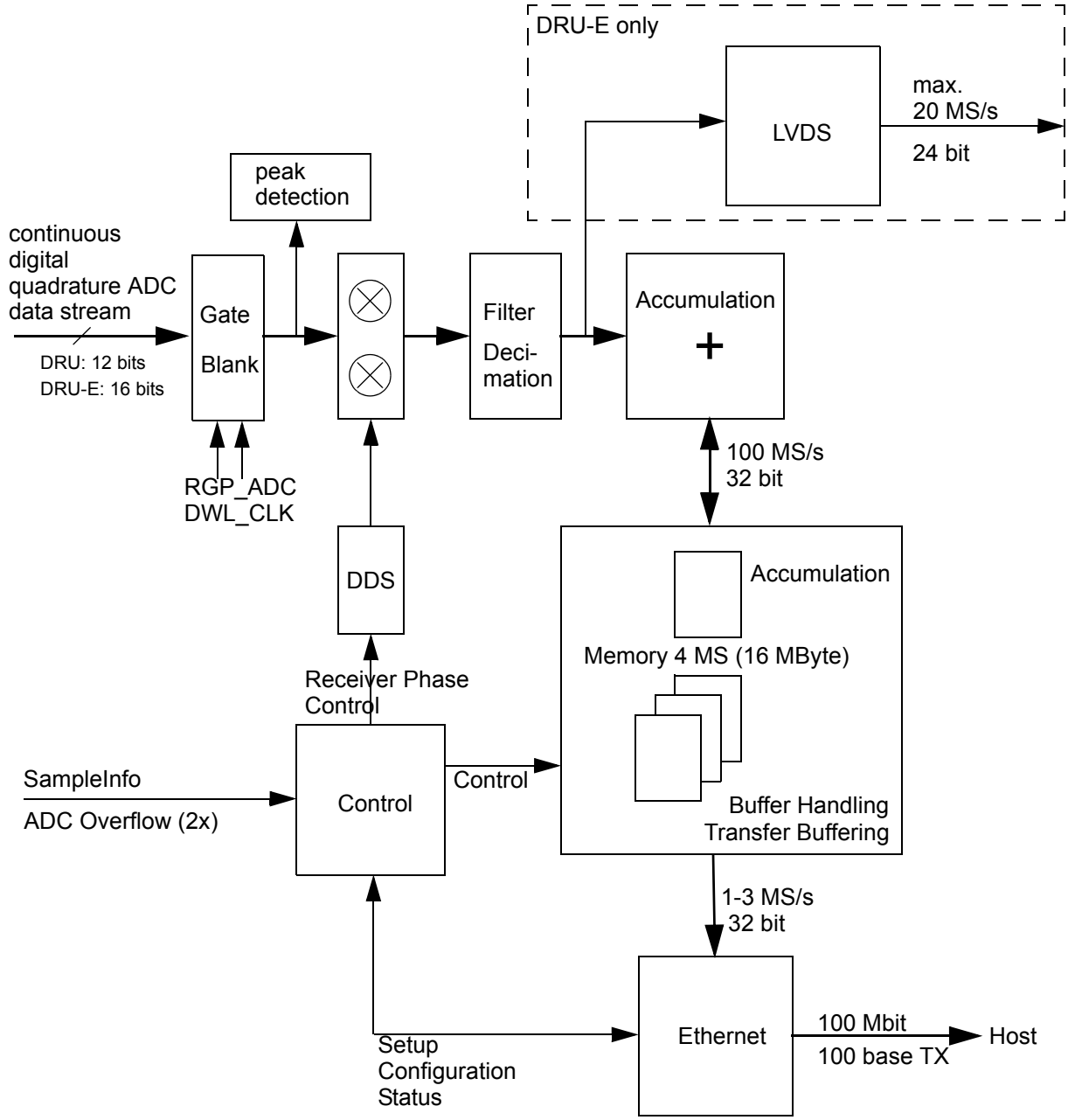
1. Interface to different types of AD converters (for future)
2. Propagate a digitizer overflow condition
3. Capture digitizer peak values (i.e. used for receiver gain adjust)
4. Automatic DC offset calibration (used for AutoZeroCompensation)
5. Digital receiver phase control
6. Digital quadrature detection (LO3)
7. Digital filtering of NMR signals
8. Decimation of NMR signals
9. Accumulation and acquisition, multi buffer handling
10. Data transfer to workstation via ethernet (write to disk, online display)
11. Special fast functions (i.e wobble display, RGA, AutoZeroCompensation)

Most of these operations (scan control) are under real time control by the pulse program via the so called ‚SampleInfo' bus. With this it is possible to handle the ADC data, in the extreme cases each sample, by the information given via this acquisition synchronous system bus. The scan control runs in parallel with the DWELL clock and the RGP_ADC of the digitizer.

Depending on type of DRU, following functional modules are incorporated:

12. Integration of AQS preamplifier controller (DRU only)
13. Real Time Trigger output (to be defined, DRU-E only)
14. High Speed LVDS data output (DRU-E only)

Figure 9.1. DRU Blockdiagram ‚digital receiver‘



Power Supply and Monitoring LED‘s ***9.2.1***

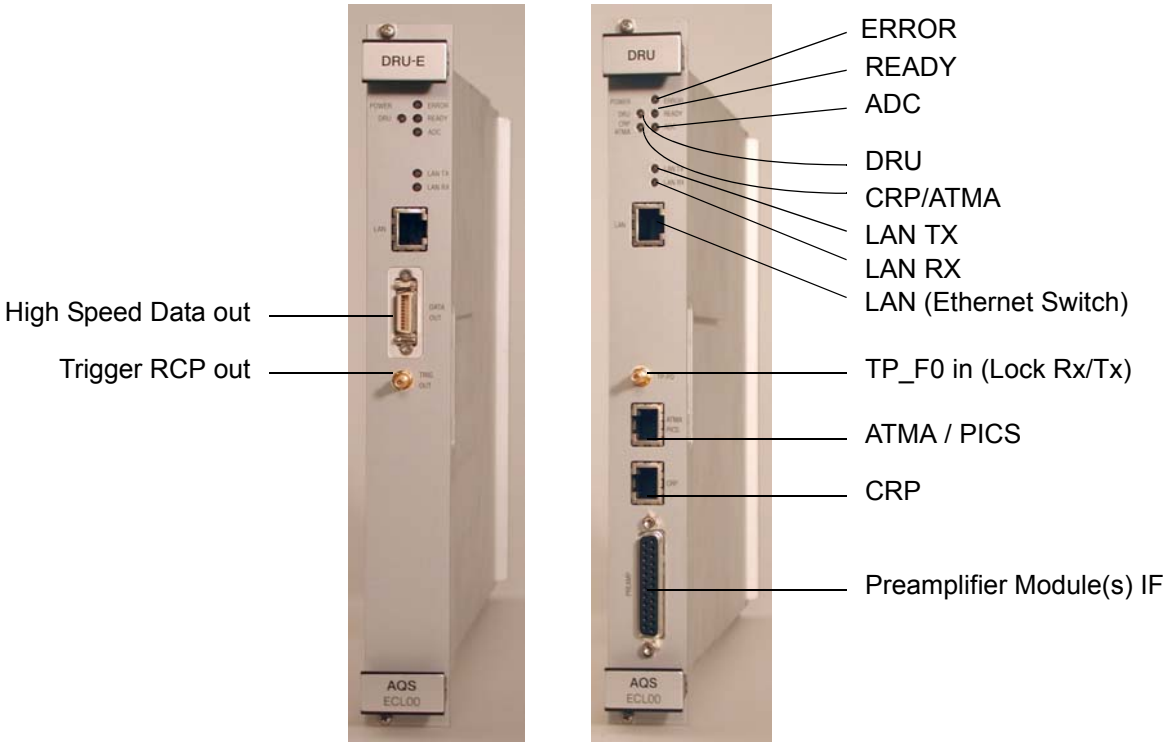
Operation of the *on-board* power stabilization is monitored by the two green LED on the front labeled ‚POWER‘.

The LED labeled ‚DRU' monitors the internal DRU supplies (3.3V, 2.5V, 1.5V). These are all derived from a single 5V AQS backplane supply.

The LED labeled ‚CRP/ATMA' monitors the +/-15V CRP and +9V ATMA voltages. These are derived from the +/-HPPR_19V and HPPR_9V AQS backplane supplies.

Front Panel Wiring / Display *9.2.2*

Figure 9.2. AQS DRU-E and AQS DRU frontside view



Reset and Operation LED Display *9.2.1*

ERROR LED:

The red ‚ERROR' LED indicates a pending ERROR.

READY LED:

Normal operation is indicated by the green ‚READY' LED.

Every 500ms this LED is turned off for 20ms, resulting in a faint flicker. If this flicker is missing, the DRU is not running properly and must be reset by switching off the AQS chassis for about 10 seconds.

ADC LED:

This green ‚ADC' LED indicates a running Acquisition.

LAN TX LED:

This green ‚LAN TX' LED indicates outgoing LAN traffic.

LAN RX LED:

This green ‚LAN RX' LED indicates incoming LAN traffic.

Servicing the DRU *9.3*

Diagnosis and servicing access to the DRU relies on HTTP, enabling service access just by any web browser. This is possible because only basic HTTP V1.1 protocol elements have been used.

Accessing the DRU *9.3.1*

Depending on the slot and the rack code, the DRU adopts one of the following IP addresses. Any illegal or unknown configuration is mapped to DRU1 and the message „Illegal Rack/Slot configuration. Fallback to DRU1 address." is written to the DRU Log.

Table 9.1. IP Addresses for DRU

IP Address	DRU Name
149.236.99.89	dru1
149.236.99.88	dru2
149.236.99.87	dru3
149.236.99.86	dru4
149.236.99.85	dru5
149.236.99.84	dru6
149.236.99.83	dru7
149.236.99.82	dru8

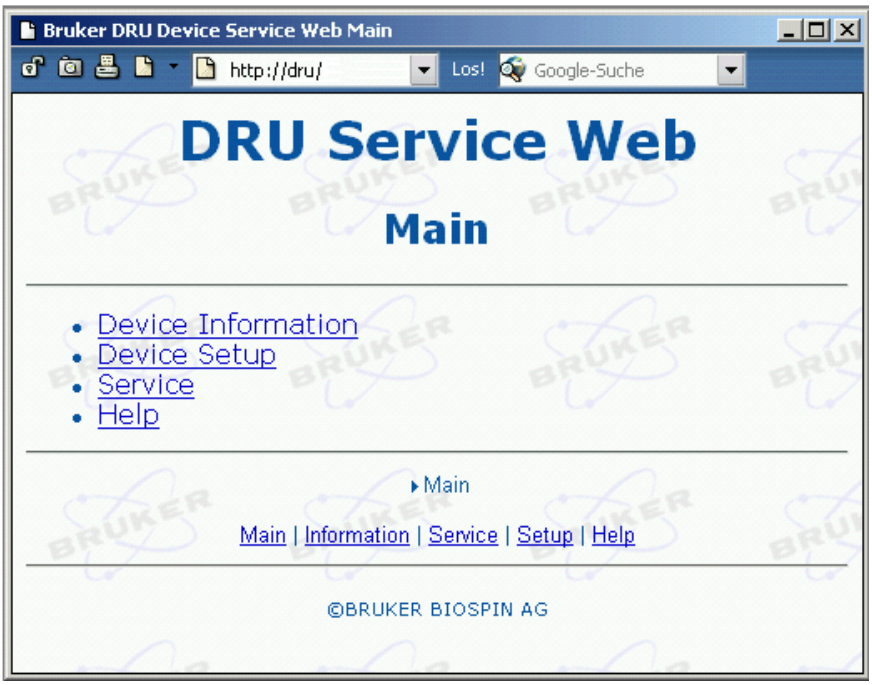
It might be useful to edit the hosts file.

In case of problems:

- check the RJ45 cabling between DRU, Ethernet switch and the workstation
- check the ethernet switch power if appropriate
- check the DRU heart beat (flicker of ‚READY LED)

- ping DRU1 (DRU2...)
- check LAN ‚RX/TX' LED while pinging

To access the DRU, start your favorite web browser and type „dru1" or „149.236.99.89" as URL. You should get the following start screen:



Downloading new firmware *9.3.2*

Main -> Device Information -> DRU Firmware

leads you to a page giving information about the current firmware.

! ***Note: The document caching of the browsers can be tricky - make sure your browser doesn't fool you with old data. Most browsers have some „Reload" button for this purpose.***

Main -> Device Setup -> Load new DRU firmware

leads you to a page allowing to download new firmware. The current firmware file name is displayed together with a prompt for the new firmware file.

The following example explains the naming convention:

```
DRU_firmware_040325.hex
```

040325 is a date code for March 25, 2004. Alphabetically sorted, the newest file is found at the bottom line.

! ***Do not download an older firmware than the currently installed one, except you want to roll back in time.***

Main -> Service -> Display logged messages

shows a page containing the main log. If you are in the situation to report a software bug, it‘s a good idea to include this log. You can copy the text part into an explaining mail or you can save the whole HTML page and attach it.

Technical data 9.4

ADC Data Input:

Data Rate	2*20	MS/s
Data Format DRU	2 x 12	bits
Data Format DRU-E	2 x 16	bits

NMR Data Output (Ethernet):

Data Rate	0.3 - 10‘000	kS/s[1]
Data Word Width	32	bits

Acquisition Modes:

Quadrature off acquisition (only channel A, analog and digital modes)	QF
Quadrature simultaneous acquisition (analog and digital modes)	QSIM
Acquisition with Digital Quadrature Detection (digital mode only)	DQD

Digital Quadrature Detection (digital down conversion):

DDS frequency range (LO3)	+/-(0...5)	MHz
Digital Mixer Operation	SSB	

Digital Filter type ‚smooth‘:

Passband Error	0.01 %	max
Transition Region	15 %	SWH
Stoppband Attenuation	86 dB	min
Group Delay	20	samples
Bandwidth (SWH)	5 MHz	max

Digital Filter type ‚medium‘:

Passband Error	0.001 %	max
Transition Region	10 %	SWH
Stoppband Attenuation	103 dB	min
Group Delay	36	samples
Bandwidth (SWH)	2.222 MHz	max

Digital Filter type ‚sharp‘:

Passband Error	0.001 %	max
Transition Region	5 %	SWH
Stoppband Attenuation	104 dB	min
Group Delay	68	samples
Bandwidth (SWH)	1.25 MHz	max

1 complex data points

Miscellaneous:

Direct accessible Scan Memory Size	4M	samples
Banked Scan Memory Size	16M	samples
Sustained LAN data rate (depending on Workstation)	45	Mbit/s

Trigger output:

Voltage Level	5	V
Impedance	50	Ohm
max Frequency	1	MHz

Backplane Connectors *9.5*

The DRU accesses the AQS backplane by 2 high density backplane connectors. The common interface is similar to the one used on SGU. The ADC data interface to the RXAD is done by a private additional backplane connector (dedicated DRU slots within the AQS chassis family).

Table 9.2. Common AQS backplane connector

	z	a	b	c	d	e	f
1	GND	GND	INTRA_STATUS		GND	SAMPLE_INFO0	GND
2	GND		GND	SAMPLE_INFO3	SAMPLE_INFO2	SAMPLE_INFO1	GND
3	GND	GND	NC	I2C_STATUS	GND	SAMPLE_INFO4	GND
4	GND	20MHZ_CLK_X	GND	INTERLEAVE_INCR~	ADC_SEL1	ADC_SEL0	GND
5	GND	GND	20MHz_CLK_X~	RESERVE_3	GND		GND
6	GND		GND			INTRA_WUP	GND
7	GND		BLNKTR4~		GND	RGP_ADC	GND
8	GND		GND			DWL_CLK	GND
9	GND		BLNKTR8~		GND		GND
10	GND	SBS_TTL_TX	GND	SBS_TTL_RX	SBS_TTL_TX_ENAB~		GND
11	GND	LOCAL_TX	LOCAL_RX	SBS_TTL_WUP~	GND	RGP_HPPR~	GND

red = CCU-Bus galvanically isolated
blue = Intra Rack Bus

Key Area

15	GND	SLOT2	SLOT1	SLOT0	GND	MCODE0	GND
16	GND	SLOT3	GND	I2C_SDA	MCODE3	GND	GND
17	GND	EMERGENCY_STOP		I2C_SCL	GND	MCODE1	GND
18	GND		GND	I2C_2_SDA	I2C_2_SCL	GND	GND
19	GND				GND	MCODE2	GND
20	GND		GND			GND	GND
21	GND	P5V		P9V	P9V	P9V	GND
22	GND	P5V	RACK0				GND
23	GND	P5V	P19V	N19V	RACK1		GND
24	GND	P5V	P19V	N19V	RACK2		GND
25	GND	P5V	P19V	N19V	RACK3		GND

Table 9.3. private DRU - RXAD backplane connector

	z	a	b	c	d	e	f
1	GND	P5V	P5V	P5V	P5V	P5V	GND
2	GND			GND		GND	GND
3	GND	ADC_I2C_SDA	GND	L3_OPT	GND	LCLK_OPT	GND
4	GND	ADC_I2C_SCL	GND	L3_OPT~	GND	LCLK_OPT~	GND
5	GND	GND	L_CLK	GND	L_DATA_3	GND	GND
6	GND	GND	L_CLK~	GND	L_DATA_3~	GND	GND
7	GND	L_OVR0	GND	L_DATA_2	GND		GND
8	GND	L_OVR1	GND	L_DATA_2~	GND		GND
9	GND	GND	L_DATA_1	GND	L_DATA_0	GND	GND
10	GND	GND	L_DATA_1~	GND	L_DATA_0~	GND	GND
11	GND	RESERVE_0	GND	RESERVE_1	GND	RESERVE_2	GND

SGU/2 Signal Generation Unit 10

Introduction 10.6

The SGU/2 is an improved version of Brukers self developed signal generation unit (SGU) for the new IPSO spectrometers. It is a broadband rf synthesizer with a high speed real-time interface.

On the transmission side the SGU/2 generates the signal frequency and phase and regulates the amplitude (including shape control) as well as the blanking and gating pulses. The information is received from the IPSO via the high speed LVDS link. The output of the SGU/2 is a low power rf signal, the small version of the final excitation signal.

During acquisition the SGU/2 generates the LO frequency and the receiver gating pluses.

There can be multiple SGU/2 in an AQS chassis representing different transmit channels. All SGU/2 are synchronized by the 20 MHz clock signal from the backplane. The clock signal is generated on the AQS Reference Board. The synchronization is essential for the phase coherence of the different rf channels.

One SGU/2 is selected to be the observing SGU/2 and generates the LO and the receiver timing. This can be any SGU/2 in the chassis depending on the frequency channel chosen as the OBS (observe) in the edsp menu.

Each SGU/2 has a dedicated hard-wired LVDS link to an F-Controller of the IPSO. The high speed link transfers all NMR relevant real-time events in two 12.5ns time slots to the corresponding SGU/2 (e.g. pulses, amplitude, phase, frequency etc.). Each rf channel is controlled by a separate high speed link. It is connected via a LVDS cable on the front panels of the two units (point to point connection).

Functions / Description 10.7

The central role played by the SGU/2 is evident from the extensive list of functions below. For further details on some of the specific details below see ***"Important signals" on page 216***.

All SGU/2:

1. Generation of the precise final transmission frequency by means of an onboard frequency generator. The SGU/2 implements all analog aspects of the signal including frequency, frequency shifts, phase, shape etc. The information regarding the precise characteristic of the signal is received from the IPSO via LVDS.
2. Amplitude control both in terms of magnitude (mult) and shape (mod). Although the SGU/2 delivers a max voltage of 1Vpp the linear nature of the amplifiers means that the SGU/2 has exclusive control of the final amplitude.
3. Generation of blanking signals for use in the various amplifiers. The AQS internal amplifiers receive the blanking directly from the backplane, whereas the

external amplifiers receive the signals from the PSD which in turn receives the signals from the backplane.

4. Downloadable DDS functionality due to FPGA technology

Observing SGU/2 only:

5. Generation of gating pulses to be used in the HPPR, Receiver, A/D Converter, RXAD, DRU
6. Generation of the dwell enable signal for the DRU
7. Generation of LO frequency for the receiver

SGU/2 on position 2:

8. Generation of the 'wobb' signal

The LO will be generated on the observing SGU/2 and daisy chained through all the succeeding SGUs to the receiver. This daisy chain is unidirectional in the direction of the receiver. E.g. in a four channel system with SGU-2 set OBS, SGU-2 will generate the LO and is daisy chained through SGU-3 and SGU-4 to the receiver. See ***Figure 10.3.***

Figure 10.3. LO daisy-chain for the case where SGU-2 is the observing SGU

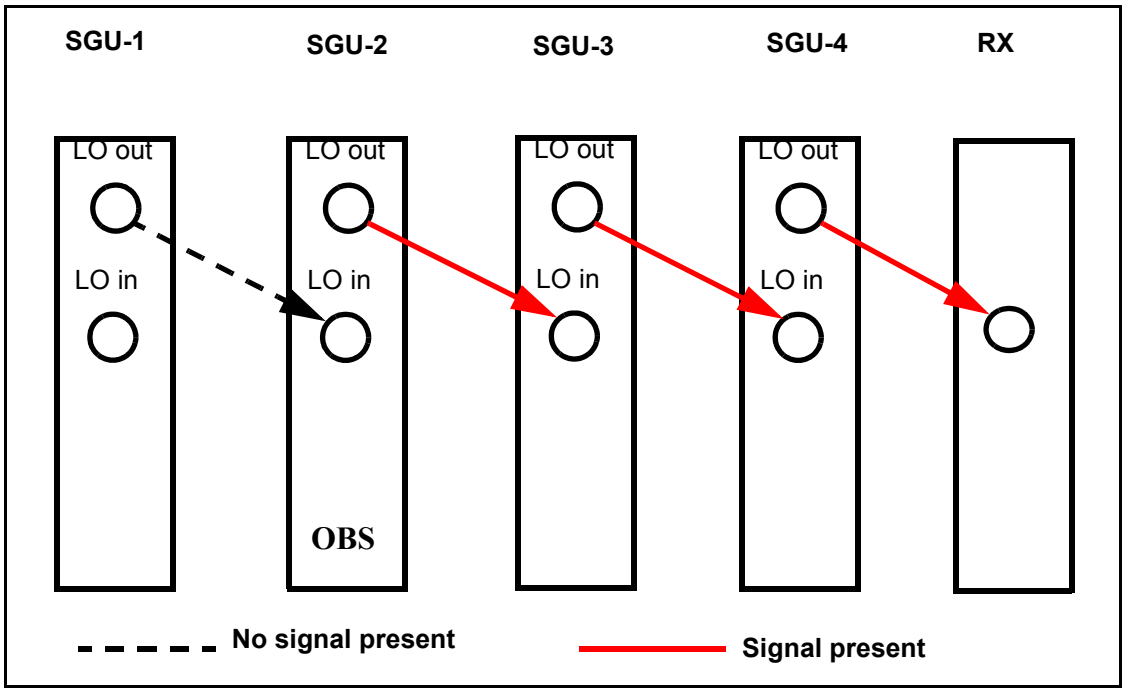
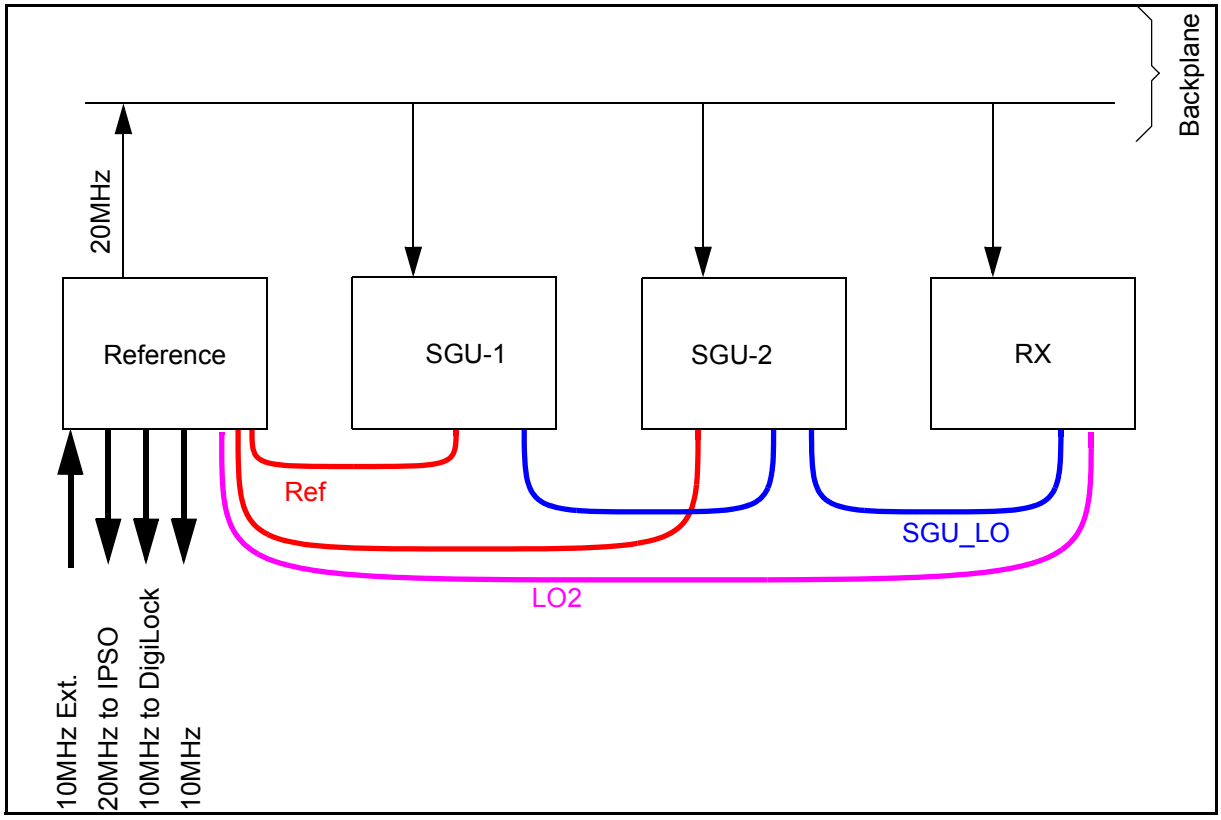


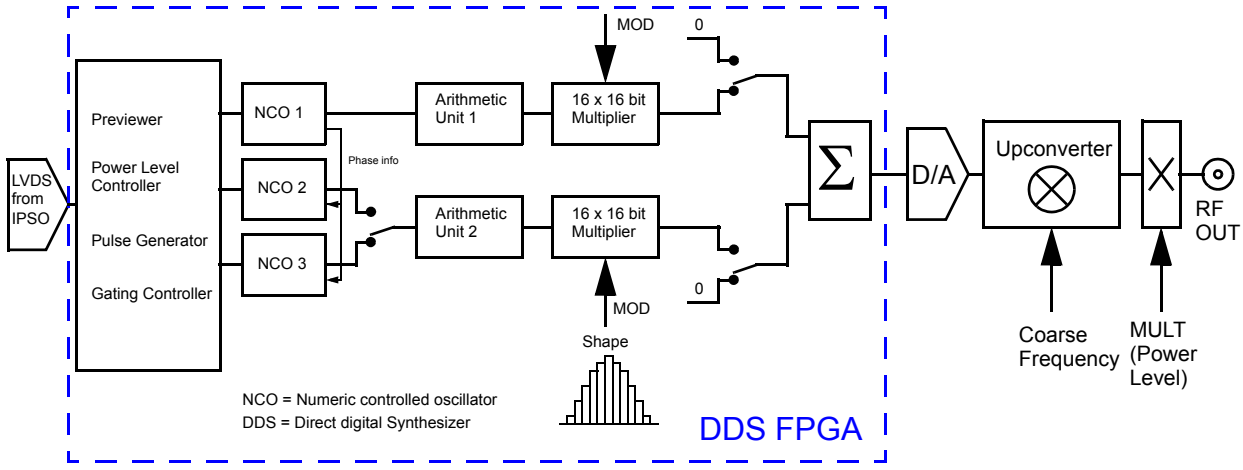
Figure 10.4. SGU/2 rf paths



Signal paths inside the SGU/2 *10.7.1*

The RF signal paths are shown schematically in ***Figure 10.6.*** Note that the signal path switching is controlled via the LVDS Interface.

Figure 10.5. Signal generation on the SGU/2



The core of the SGU/2 consists of three NCOs (Numerically Controlled oscillators) NCO1, NCO2, NCO3. NCO0 is used for zero transmission.

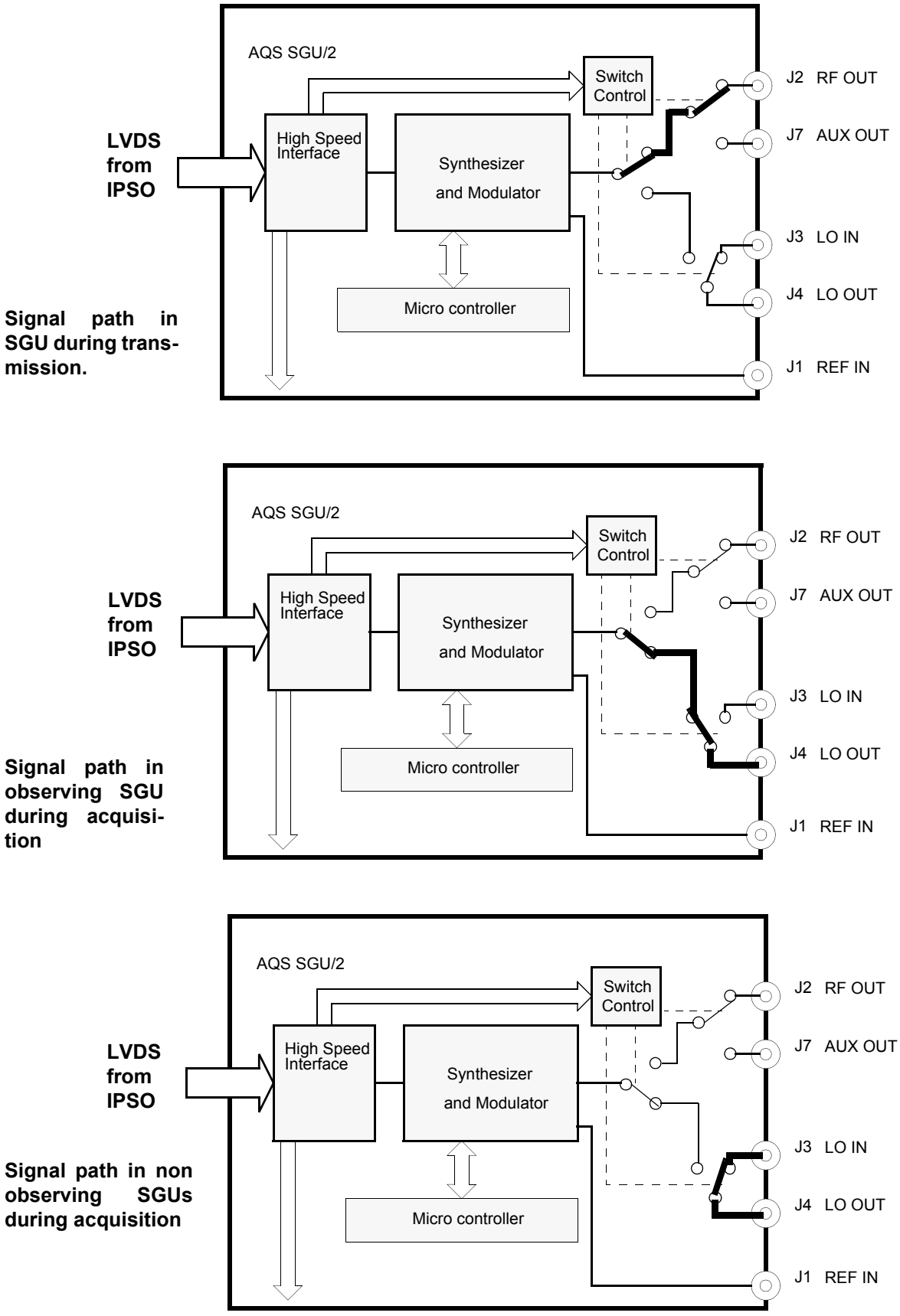
NCO1 is always used for the OBS frequency

Any shifts in frequency are implemented using NCO2.

NCO3 is always used for the LO frequency. This assignment of the various NCOs is illustrated in ***"NCO allocation" on page 204***

The advantage of using multiple NCOs is that frequency, amplitude and phase information can be loaded simultaneously. This facilitates instantaneous switching from one phase or frequency to another etc.

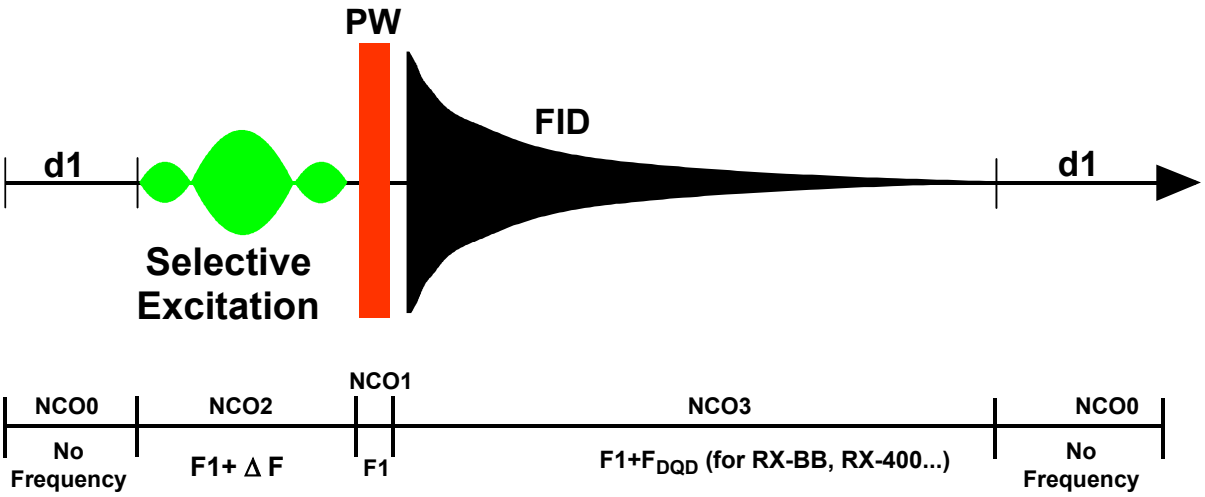
Figure 10.6. Signal paths inside the SGU/2



The timing of the NCO output is controlled by a series of instructions transmitted by the IPSO via LVDS with a 12.5ns timing resolution.

The output of the different NCOs is a digital representation of all characteristics of the required signal. This digital signal is then modulated using the 'MOD' input to implement the shape of the signal. At this point the signal is still digital which is then passed through a DAC to generate an analog output. The signal at this stage has still not the final frequency. This is obtained with the up converter which mixes the oscillator frequency with the appropriate frequency from the REF unit to produce the final transmission frequency. The last step is the power level adjust ('MULT') which sets the overall amplitude of the RF output.

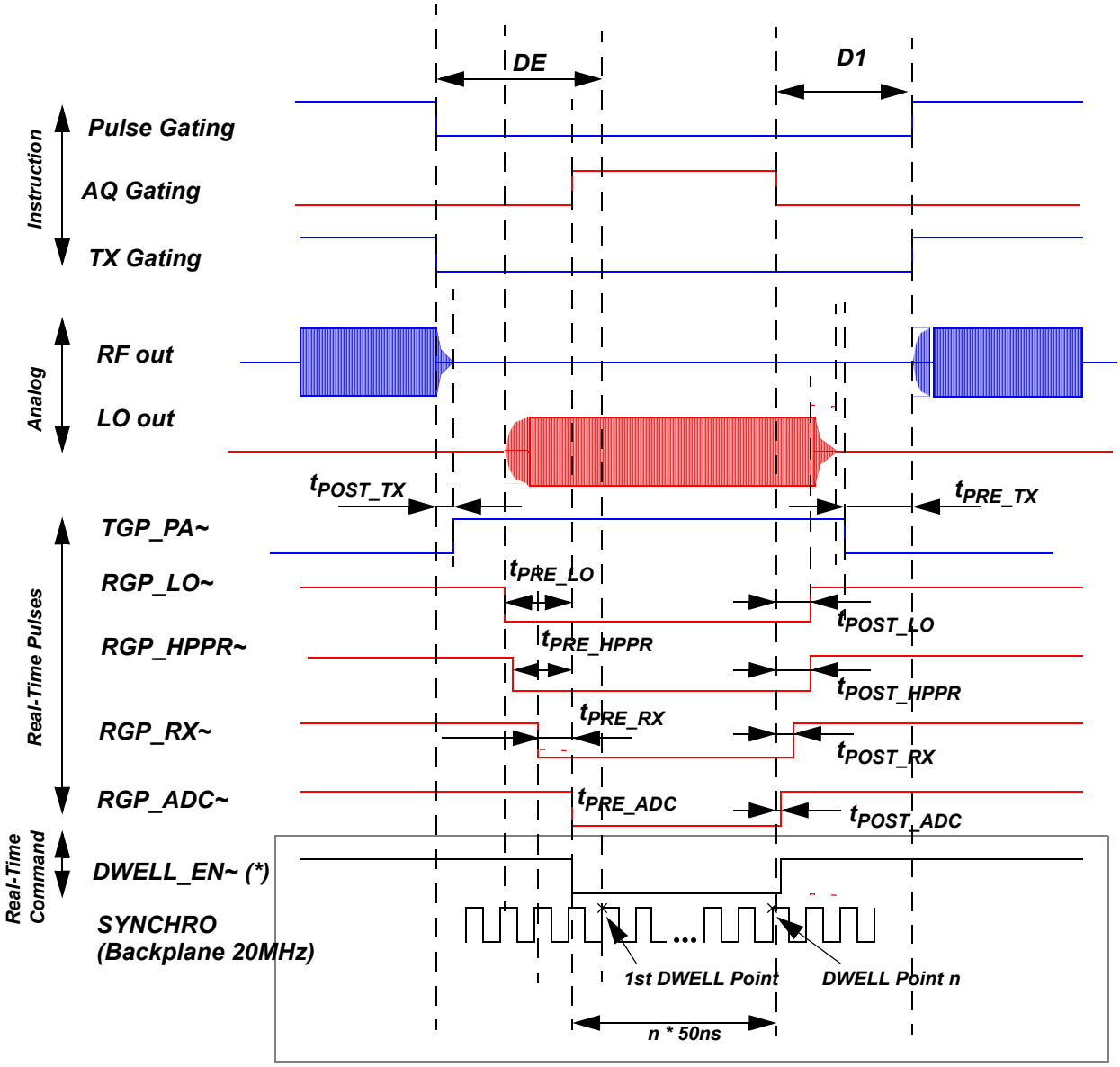
Figure 10.7. NCO allocation



Intelligent Pulse generation *10.7.2*

Compared to the old SGU, the SGU/2 offers more intelligence in pulse generation. The built-in previewer manages all delays required by the different hardware. All pre- and postdelays for the transmitter, preamplifier and receiver are generated automatically and can be configured on the SGU/2 (***Figure 10.8.***). Thus pulse programming gets much easier.

Figure 10.8. Intelligent pulse generation of the SGU/2



Unit Configuration / Version / Jumpers *10.8*

Four versions of SGU/2 have been produced.

- SGU/2 400 Part-No. Z103080, output frequency range limited to 430MHz
- SGU/2 600 Part-No. Z103081, output frequency range limited to 643MHz
- SGU/2 1000 Part-No. Z103082, output frequency range limited to 1072MHz
- SGU/2 FTMS Part-No. Z103083, output frequency range limited to 10MHz

Key specifications and digital control behavior are the same for all versions.

Through the ‘cf’ routine the number and location of all installed SGU/2 is determined. Each SGU/2 in the AQS chassis has a unique address given by its slot po-

sition. The addresses are used to distinguish the various SGU/2 from each other. There are no jumpers that need to be set.

Regardless of the system the SGU/2 are lined up on the left of the REF unit.

A micro bay system will accommodate up to three SGU/2.

A one bay system will accommodate up to four SGU/2 (three if internal amplifiers are used)

A two bay system will accommodate up to 8 SGU/2 (4 attached to REF1 and 4 attached to REF2)

Any of the SGU/2 may be selected as the Observe SGU. In the ‘edsp’ menu the F-Controller number is equivalent to the SGU number and so this menu will easily tell the operator which SGU is the observing SGU.

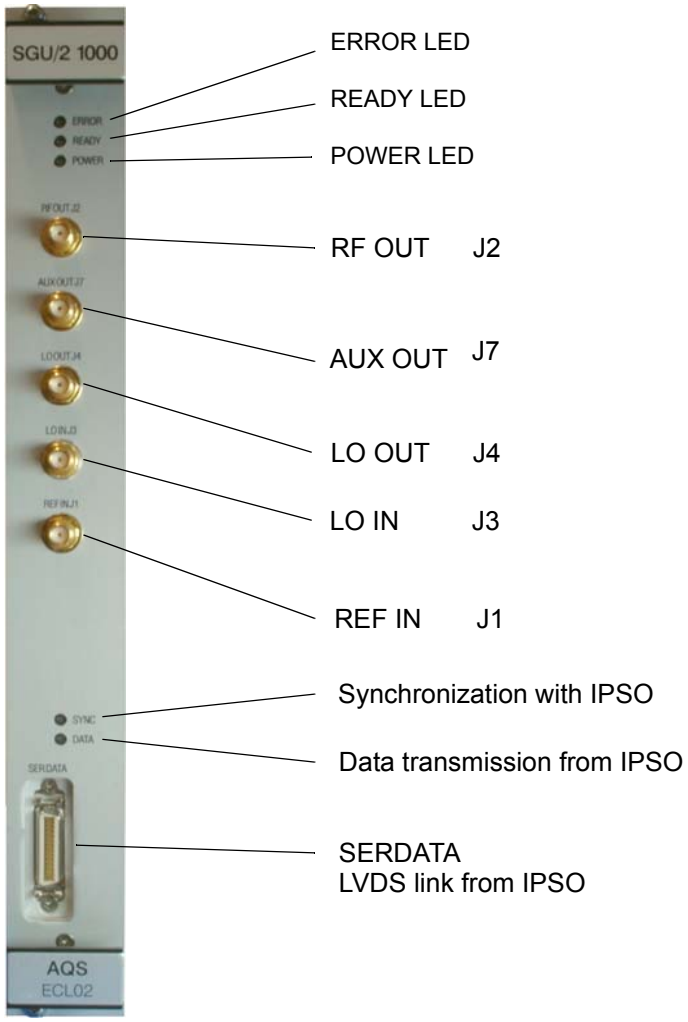
Table 10.4. Assignment of SGU/2

Physical SGU/2	Physical IPSO Channel	edsp display
1	F/G-Controller 1	SGU1
2	F/G-Controller 2	SGU2
3	F/G-Controller 3	SGU3
4	F/G-Controller 4	SGU4

Differences from previous versions *10.8.3*

The SGU/2 is a new development for the IPSO system and can not be used in older AV spectrometers.

Figure 10.9. SGU/2 front panel



RF OUT J2

This is the single RF output which will be connected either to an internal amplifier input directly or to the router on its way to an external amplifier. This signal will have a max amplitude of 1Vpp at a power setting of -6db. The signal will only be present during pulse transmission as the blanking takes place on the SGU/2 itself.

AUX OUT J7

The wobb signal ALWAYS comes from the AUX out of SGU-2 since this is hard wired to the 'Tuning In' input of the HPPR cover display module. On all other SGU/2 this output is left unconnected except for the case of SGU-1 where it can be connected to the 2HTX on an AQS with no router. The wobb signal will appear as a swept frequency whose variations in frequency will depend on the setting of 'wbsw'. On the scope it appears typically as a pulsing frequency of maximal 1Vpp. (note that the wobble signal amplitude for HPPR/2 can be set by software, typical values are around 150mVpp)

The LO for the WOBB routine will come from the observing SGU LO OUT. This will also appear as a swept frequency except that this time the central frequency will be the wobble frequency + detection offset frequency (LO, DQD).

Since all SGU/2 are physically identical the AUX OUT output would be capable of transmitting RF signal from any SGU/2 but this would require explicit pulse programming.

LO OUT J4

RF signal for the receiver (1.0Vpp at 50 Ohm). The signal is generated on the observing SGU and then daisy chained through successive SGUs in the direction of the receiver. This signal will only be present during AQ (acquisition time) and if the SGU in question is the observing SGU or is located to the right (further along the daisy chain) of the observing SGU.

LO IN J3

This signal will only be present if the SGU in question is located to the right (further along the daisy chain) of the observing SGU (1.0Vpp at 50 Ohm).

REF IN

Input RF signal from the REF unit. This is a set of frequencies which are used to generate the final transmission frequencies.

SERDATA

LVDS link from IPSO.

! ***Not compatible to former SGU or FCU.***

Front Panel SGU-FTMS

The SGU/2 FTMS has no LO output connectors because of the different receiver concept.

LED Display *10.9.4*

Power LED:

The power LED indicates that **all** necessary voltages are present and have the correct level. If one of the voltage level drops the power LED goes out.

The table below shows the states of the three front panel LEDS.

Table 10.5. LED States

ERROR (red)	READY (green)	POWER (green)	Description
-	-	off 	- Power supply not on or operating incorrectly
off 	on 	on 	- **Normal sleep mode** - ready for operation - SGU/2 micro controller is powered down

Table 10.5. LED States

ERROR (red)	READY (green)	POWER (green)	Description
off 	periodically flashing, approx. twice per second 	on 	READY LED on the SGU/2 front panel indicates with a ‚Heart Beat' flashing that the micro controller is running. During acquisition the micro controller on the SGU is in power save or sleep mode and the READY LED must be in a steady state. The SGU/2 board should always be in sleep mode, unless TopSpin is writing new configuration information or during ‚gs' or wobble. The sleep mode reduces power consumption, increases component reliability, improves thermal stability and avoids electrical noise.
off 	on resp. short-time flickering 	on 	- Communication LED. The unit has received a command from the RS485 bus master. The LED switches to off as soon as the SGU/2 acknowledges the command.
blinking slowly (approx. 3 Hz) 	on 	on 	- Indicates warning. The sleep mode during acquisition is disabled (‘gs’ mode). Caution: Sensitive NMR experiments are not possible in this mode due to disturbances of the controller system.
blinking slowly (approx. 3 Hz) 	off 	on 	- An error has occurred on the SGU/2
blinking fast 	-	on 	- Boot-mode Board not initialized yet or no application firmware found (e.g. because of power failure during firmware update).

SGU/2 Firmware 10.10

Identification of the firmware and DDS FPGA version 10.10.1

You can identify the SGU/2 firmware and DDS FPGA version using Unitool as described below:

via UniTool

1. Open a shell or the command prompt in the BRUKER Utilities folder when using Windows.
2. Start the UniTool with: `TopSpin -e UniTool`
3. -> `aqs`, confirm
4. -> decimal address for e.g. SGU-1 is 36, for SGU-2 is 37 etc., confirm
5. Choose -> 1 (Board Info), confirm

You will be given the details of firmware, boot software and DDS FPGA version.

via AQS Service Web

1. Start a web browser and open the AQS Service Web page. (see ***13.6***)
2. Go to the „AQS Control Overview“ page („Hosted Devices“ → „AQS Overview“). There you can see a table entry for each SGU. Follow the links to the AQS SGU page.

! ***Boards programmed in factory may show a different application firmware checksum compared to boards downloaded with UniTool***

Download new SGU/2 firmware 10.10.2

Please refer to the BRUKER Service Information to check out if a download is necessary.

! ***The download of the newest firmware is not always necessary. Please read the instructions carefully.***

! ***For proper operation all SGU/2 with same ECL must have identical firmware versions.***

Be sure that all SGU/2 have installed the **newest** corresponding firmware version.

Download procedure:

1. Download latest firmware (e.g. sgu2ab.hex) from ftp://ftp.bruker.ch/pub/NMR/download/servtools/firmware/aqs/ and save it to the following directory on your workstation:
   /Bruker/<`topspin release`>/conf/instr/servtool/UniTool/files/birds
2. Read the release notes carefully

3. Start UniTool from the Start Menu
4. -> `aqs`, confirm
5. Determine decimal address for SGU to be load down (36 for SGU-1, 37 for SGU-2 etc.)
6. Select *Auto Download*. The download routine checks if a download is necessary.

Further information about the demand of new firmware can also be found on the FTP server of BRUKER AG (B-CH):

ftp://ftp.bruker.ch/pub/NMR/download/servtools/firmware/aqs/

Download new DDS FPGA version *10.10.3*

Please refer to the BRUKER Service Information to check out if a download is necessary.

! ***For proper operation all SGU/2 with same ECL must have identical DDS FPGA versions.***

Download procedure:

1. Download latest DDS FPGA version (e.g. dds2ac.rbf) from ftp://ftp.bruker.ch/pub/NMR/download/servtools/firmware/aqs/ and save it to the following directory on your workstation:
   /Bruker/<`topspin release`>/conf/instr/servtool/UniTool/files/birds
2. Read the release notes carefully
3. Start UniTool from the Start Menu
4. -> `aqs`, confirm
5. Determine decimal address for SGU to be load down (36 for SGU-1, 37 for SGU-2 etc.)
6. -> `Service Functions`, confirm
7. Select *Download DDS FPGA*, confirm
8. Enter the filename of the DDS FPGA version, e.g. birds/dds2ac.rbf

Further information about the demand of new firmware can also be found on the FTP server of BRUKER AG (B-CH):

ftp://ftp.bruker.ch/pub/NMR/download/servtools/firmware/aqs/

Part Numbers *10.11*

- SGU/2 400 Part-No. Z103080 (430MHz)
- SGU/2 600 Part-No. Z103081 (643MHz)
- SGU/2 1000 Part-No. Z103082 (1072MHz)
- SGU/2 FTMS Part-No. Z103083 (10MHz)

Troubleshooting / Unit replacement / Tips 'n' Tricks *10.12*

General *10.12.4*

1. All SGU/2 are identical and interchangeable. If units are swapped re configuration is recommended to ensure that there are no inconsistencies in unit detection. Note that for best performance all SGU/2 should be of the same type and ECL.
2. Ensure that all SGU/2 are loaded with the same firmware. This can be done using UniTool.
3. Ensure that all SGU/2 are loaded with the same DDS FPGA version. This can be done using UniTool.
4. Do not open the SGU/2 in the field.
5. Ensure that the 26 pin LVDS cable from the IPSO is connected before power-up of the AQS. This will ensure the correct termination and prevents communication errors.

Error Messages *10.12.5*

Description of possible error messages:

Table 10.6. AQS SGU error messages

Error No..	Error Message	Description	Possible cause
Error No. 1	Serial RS485 time-out	slave device did not answer in expected time	slave device probably not initialized, check connections
Error No. 2	Checksum	wrong firmware checksum	internal hardware error or download failed
Error No. 4	Serial RS485 command, checksum error	RS485 protocol violation	spectrometer control software failure
Error No. 10	RAM self test error	RAM test failed	hardware failure
Error No. 11	no application firmware found	ROM test failed	hardware failure or firmware download failed
Error No. 13	Power failed	indicate that a power up has happened and the system is not initialized	ordinary power up or a power breakdown during an experiment
Error No. 15	Parameter exceeds valid range	value out of range	spectrometer control software failure or faulty input using Unitool
Error No. 17	Function not supported by board hardware version	selected feature not supported by actual hardware version	spectrometer control software failure, wrong command selected using UniTool
Error No. 18	Unknown version index in configuration page	internal validation of calibration data failed	hardware error
Error No. 20	Syntax error	selected feature not supported by actual firmware, board does not understand command	spectrometer control software failure, wrong board selected, hardware feature not supported by actual version
Error No. 22	RTX create error	operating system error	firmware or hardware error on SGU
Error No. 23	RTXmemory allocation error		
Error No. 24	RTX memory free error		
Error No. 25	RTX communication pool exhausted		
Error No. 26	RTX send signal error		
Error No. 27	RTX interrupt handling error		
Error No. 28	RTX semaphore waiting list full		
Error No. 29	RTX pool create error		

Table 10.6. AQS SGU error messages

Error No..	Error Message	Description	Possible cause
Error No. 36	Flash byte program error	failure during FLASH memory programming	hardware failure
Error No. 37	Flash erase error		
Error No. 40	Flash erase timer expired		
Error No. 41	Error in flash command sequence		
Error No. 42	Flash page mismatch, storing terminated		
Error No. 43	No valid calibration data		
Error No. 44	File not found	Message occurs only with UniTool	wrong file name or path
Error No. 50	RAM self test error	RAM test failed	hardware failure
Error No. 51	No application firmware found (wrong firmware checksum)	ROM test failed	download error or wrong firmware downloaded
Error No. 52	No application firmware found (wrong firmware name)	ROM test failed	download error or wrong firmware downloaded
Error No. 53	No application firmware found (wrong firmware ID)	ROM test failed	download error or wrong firmware downloaded
Error No. 54	Power supply failure detected	A power supply voltage is out of range.	hardware failure. Check also the power supplies.
Error No. 58	Corrupt BIS on board	BIS (Board Information System) test failed	hardware failure
Error No. 59	BIS checksum error	BIS (Board Information System) test failed	hardware failure
Error No. 60	Unknown rack code	Unknown rack code	invalid jumper setting on chassis user bus
Error No. 64	LVDS data link: parity bit fault	Parity bit fault on LVDS data link	LVDS data link disconnected and reconnected
Error No. 65	LVDS data link: synchronization bit fault	Synchronization bit fault on LVDS data link	LVDS data link disconnected and reconnected
Error No. 66	LVDS data link: instruction alignment fault	Alignment error on LVDS data link	FPGA reset on SGU/2
Error No. 67	Real-time instruction timing violation: DE time too short	Timing check error while changing to acquisition state	Time between transmit and acquisition too short
Error No. 69	Real-time instruction timing violation: SGU pre-delay 1 time too short	Timing check error while changing to tune state	Time between two tune sequences too short
Error No. 70	Real-time instruction timing violation: SGU pre-delay 2 time too short	Timing check error while changing to homo decoupling state	Time between transmit and homo decoupling too short
Error No. 71	Real-time instruction fault: invalid gating state transition	Invalid state transition of the gating state machine	Error in gating instruction from IPSO
Error No. 72	Real-time instruction fault: unknown instruction	Unknown real time instruction	Invalid real time instruction from IPSO

Table 10.6. AQS SGU error messages

Error No..	Error Message	Description	Possible cause
Error No. 73	Overflow in NCO combiner detected	Sum of amplitudes of NCO1 and NCO2 exceeds maximum value	NCO Amplitudes to high
Error No. 74	Scan Info lost	Timing violation while sending a Scan Info Instruction from IPSO via SGU to DRU.	Time between two Scan Info instructions too short.
Error No. 99	SSRB time-out error	Internal communication error	DDS FPGA error
Error No. 100	Serial DAC bus (SPI, 8420) error	on board serial DACs for calibration can not be set	hardware failure
Error No. 102	Missing valid configuration page	configuration data (calibration data) not available	hardware failure
Error No. 105	Flash table does not exist, using default table	configuration data (calibration data) not available	hardware failure
Error No. 107	Table address or identifier exhausts range	selected table not supported by actual hardware version	spectrometer control software failure, wrong command selected using UniTool
Error No. 109	SGU frequency range exceeded	value out of range	spectrometer control software failure or wrong SGU type in chassis (e.g. SGU400 in a AV600 system)
Error No. 110	Emergency stop is active, SGU forced to reset.	an emergency stop signal from backplane detected	emergency stop signal activated by any spectrometer unit or BSMS keyboard
Error No. 112	SBSB Wake-Up occurred during acquisition, SGU uP booted	SGU has been set to generate LO signal while the on-board microcontroller was running spectra may show spikes	spectrometer control software failure
Error No. 113	Function not allowed in present mode		spectrometer control software failure
Error No. 115	Board overheated, check AQS cooling and ventilation system!	on-board diagnostic detected board temperature of > 75°C	fans/ventilation broken down, power supply defect
Error No. 116	Power supply failure detected	on-board diagnostic detected drop of power supply voltages below specified range	power supply defect or on board voltage regulator failure

Diagnostic Tests *10.13*

Not applicable

Power supplies and board temperature are checked periodically by the on-board micro controller.

Important signals *10.14*

All signals described below are active low and TTL except for the blanking signals which use an open drain configuration.

BLKTR (amplifier blanking pulses)

A SGU/2 can control up to 8 power amplifiers with the corresponding BLKTR. The timing of the blanking pulses is controlled by the pulse gating from the IPSO and the configured pre and post delays of the SGU/2. All SGU/2 are capable of generating blanking pulses.

The internal amplifiers receive the blanking directly from the backplane, whereas the external amplifiers receive the signals from the PSD/3 which in turn receives the signals from the backplane.

RGP_HPPR~ (Preamplifier receiver gating pulse)

This pulse is generated by the observe SGU/2 and is used to gate the OBS module on the HPPR and used to implemented the transmit / receive switching. The timing of the pulse can be modified with the ‘edscon’ parameters. This signal is routed via the PSD/3 to the observe module in the preamplifier HPPR or HPPR/2. All other non lock HPPR modules are left permanently in transmission mode.

RGP_LO~ (Local oscillator gating pulse)

This pulse is generated by the observe SGU/2 and initiates the frequency switch to generate the LO frequency.

RGP_RX~ (Receiver gating pulse)

This pulse generated by the observing SGU/2 controls the opening and closing of the receiver and is transmitted directly over the backplane. The timing of the pulse can be modified with the ‘edscon’ parameters.

RGP_ADC~ (ADC gating pulse)

This pulse (also driven by the observe SGU/2) controls the ADC data. If the pulse is low and a dwell enable applied, the ADC will perform a conversion. If the pulse is high and a dwell enable is applied, the ADC generates ‘zero’ data. The RGP_ADC is routed over backplane to the ADC. This signal is specially used for digital homo decoupling with oversampling.

DWELL_ENABLE~

The signal is driven by the observe SGU/2 and is used to control the timing of the A/D conversion. A low level of this signal enables ADC conversion. The signal is generated on the SGU/2. The timing is controlled by the AQ gating from the IPSO and the pre and post delay configuration in den SGU/2. The pulse is routed over the backplane to the RXAD.

Specifications *10.15*

Timing

Minimum Pulse or delay duration: see specification of IPSO.

Time Resolution: 12.5ns

The resolution is given by the internal 80MHz clocking frequency of the SGU/2. Thus pulses or delays between pulses can thus be set to multiples of 12.5ns.

Frequency

Frequency Range SGU/2 400:	5-430	MHz
Frequency Range SGU/2 600:	5-643.450	MHz
Frequency Range SGU/2 1000:	5-1072.625	MHz
Frequency Range SGU/2 FTMS:	0,003-10	MHz

Frequency Stability: This is governed by the stability of the crystal oscillator on the REF. unit which is specified to 3 $x10^{-9}$/day and 1 $x10^{-8}$/year

Frequency Resolution: The DDS is clocked by 80MHz and the frequency setting is stored in a 34 bit register $\rightarrow$ 80 MHz/2^{34} <0.005 Hz.

Frequency Switching Time:

Instruction time for frequency steps: 25 ns with resolution of 12.5 ns

Further information on response time of analog hardware: see section ***"Hardware response" on page 218***

Phase

Phase Resolution: A 16 bit register is used to store phase values.
$\rightarrow$ 360°/2^{16} < 0.006°

Phase Switching Time:

Instruction time for phase steps: 25 ns with resolution of 12.5 ns

Total response time for any phase step to a phase error with less than 1° < 300ns

Further information on phase settling time: see section ***"Hardware response" on page 218***

Amplitude

Modulator Range: The Modulator values are stored in a 16 bit register which equates to a voltage dynamic range of 96dB. (20 log(2^{16}) =96 dB).

Power Level Range: The Power Level values are stored in a 15 bit register which equates to a voltage dynamic range of 90dB. (20 log(2^{15}) =90 dB)

Power Level resolution: 0.1 dB

Amplitude switching time:

Instruction time for amplitude: 25ns

Response time of analog hardware: <100ns

Hardware response *10.15.6*

The SGU/2 frequency, amplitude (MOD) and power level (MULT) registers can be set within 12.5ns, the actual update rate is limited by the serial link and the event synchronization to 25ns. The time until the new values are set on the output can be much longer because of the limited bandwidth in the analog sections inside the SGU/2.This additional time is called response time or settling time.

The settling time is independently of change frequency or phase. A quite hard test is to change phase by 180° and measure the time elapsed to achieve a remaining error of <1°.

Figure 10.10.Response 180° phase step

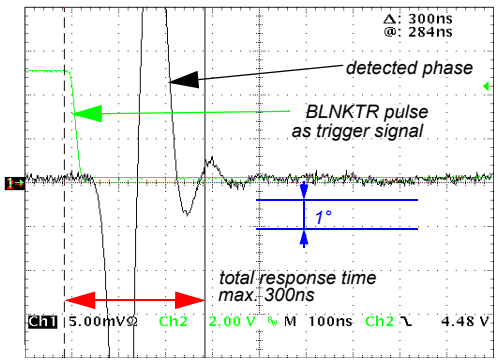
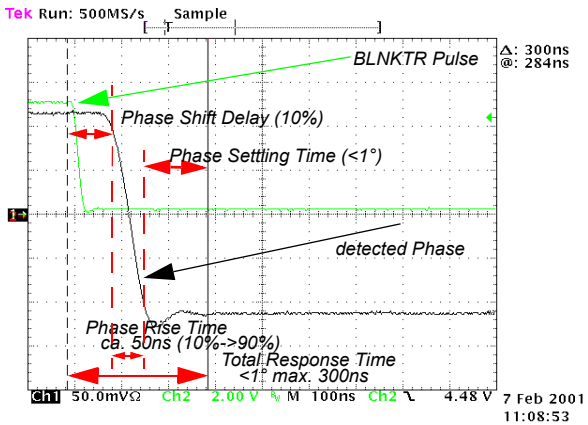


Figure 10.11.Response 90° step (45°/+135°)



Power Supply / Fuses *10.16*

See ***10.9.4***

Backplane Connector *10.16.7*

Table 10.7. shows a list of the signals transmitted to all user slots via the middle rear 110 pin connector J0.

Table 10.7. SGU/2 Backplane Connector

	z	a	b	c	d	e	f
1	GND	GND	INTRA_STATUS_INT	NC	GND	SAMPLE_INFO0	GND
2	GND	NC	GND	SAMPLE_INFO3	SAMPLE_INFO2	SAMPLE_INFO1	GND
3	GND	GND	NC	I2C_STATUS_INT	GND	SAMPLE_INFO4	GND
4	GND	20MHZ_CLK_X [a]	GND	INTERLEAVE_INCR	ADC_SEL1	ADC_SEL0	GND
5	GND	GND	20MHz_CLK_X [a]	SBSB_STATUS_INT	GND	RGP_LO	GND
6	GND	BLNKTR1	GND	BLNKTR2	RESERVE_6	RESERVE_4	GND
7	GND	BLNKTR3	BLNKTR4	NC	GND	RGP_ADC	GND
8	GND	BLNKTR5	GND	BLNKTR6	RESERVE_7	DWL_ENAB	GND
9	GND	BLNKTR7	BLNKTR8	NC	GND	RGP_RX	GND
10	GND	NC	GND	NC	NC	RESERVE_5	GND
11	GND	LOCAL_TX	LOCAL_RX	SBSB_TTL_WUP	GND	RGP_HPPR	GND

Key Area

15	GND	SLOT2	SLOT1	SLOT0	GND	NC	GND
16	GND	SLOT3	GND	I2C_SDA	NC	GND	GND
17	GND	EMERGENCY_STOP	I2C_BUS_REQ	I2C_SCL	GND	NC	GND
18	GND	NC	GND	I2C_2_SDA	I2C_2_SCL	GND	GND
19	GND	STXD [b]	SCLK [b]	SINTR [b]	GND	NC	GND
20	GND	SRXD [b]	GND	P2V	N2.5V	GND	GND
21	GND	P5V	P35V	P9V	P9V	P9V	GND
22	GND	P5V	RACK0	N9V	N9V	N9V	GND
23	GND	P5V	P19V	N19V	RACK1	P12V	GND
24	GND	P5V	P19V	N19V	RACK2	P12V	GND
25	GND	P5V	P19V	N19V	RACK3	P12V	GND

a x = Slot-No. (20MHZ_CLK_1 up to 20MHZ_CLK_8)
b unused

AQS Pulse & RF-Splitter 11

Introduction 11.1

The AQS PULSE SPLITTER and AQS RF-SPLITTER boards are used for the following signal distribution between AQS/2 or AQS/3 and AQS/2-M chassis:

- 20MHz clock
- 11 receiver (RX) pulses (RGP_LO~, RGP_ADC~, RGP_RX~, RGP_HPPR~, DWL_ENAB, INTRLEAVE_INCR~, SAMPLE_INFO[0:4] ~)
- LO-signal
- LO2-signal

The PULSE SPLITTER board is situated in one of the AQS slots in the front of the AQS/2 or AQS/3 chassis, the RF-SPLITTER in the rear of the AQS/2-M chassis.

PULSE and RF-SPLITTER are connected via a twisted pair cable with Mini-Delta-Ribbon (MDR) connectors. The cable has a differential impedance of 100Ω.

One PULSE SPLITTER can support up to 5 AQS/2-M chassis. Each AQS/2-M chassis needs one RF-SPLITTER board.

LO- and LO2-signals are split in the RF-SPLITTER. Each splitter has one input and 10 outputs. The LO-splitter has an additional input and LO-switch. All splitters are unity gain calibrated. Up to 3 RF-SPLITTER boards can be cascaded.

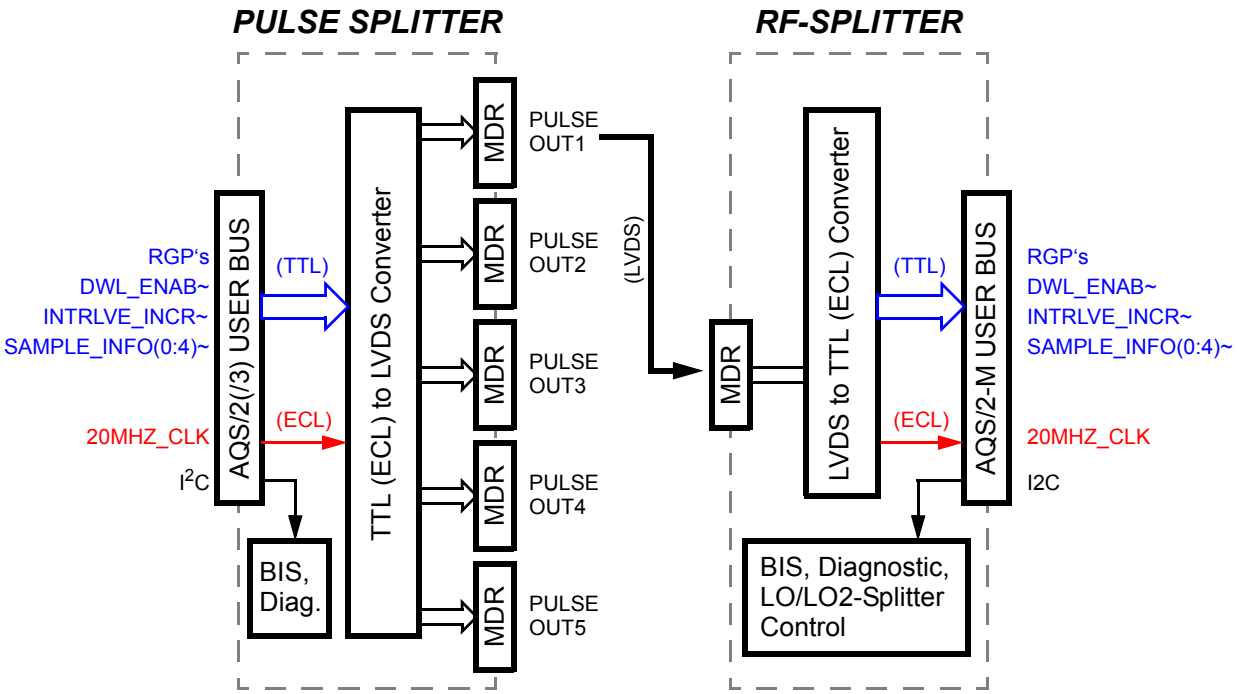
Both units are equipped with I^2C-bus and LED indicator diagnostic features. Gain calibration and LO-switch of the splitters are I^2C-bus controlled.

Functions/Description 11.2

20MHz Clock and RX-Pulse Distribution 11.2.1

The PULSE SPLITTER board receives both clock and RX-pulses from the user bus and converts them to LVDS-logic level signals. These are transmitted via the MDR-cable to the RF-SPLITTER. It converts them back to their former logic levels and routs them to the user bus.

Figure 11.1. Clock & RX-Pulse distribution



LO- & LO2-Splitter *11.2.2*

Both LO- and LO2-splitters are integrated into the RF-SPLITTER unit.

The LO-output signals from SGU1 and SGU2 are fed into the inputs LO_IN1 and LO_IN2. The outputs are either connected to a RXAD or a LO-splitter input on another RF_SPLITTER unit.

The LO2 output signal from the REFERENCE board is fed into the LO2_IN1. The outputs are either connected to a RXAD or a LO2-splitter input on another RF_SPLITTER unit.

Figure 11.2. LO/LO2- Splitter

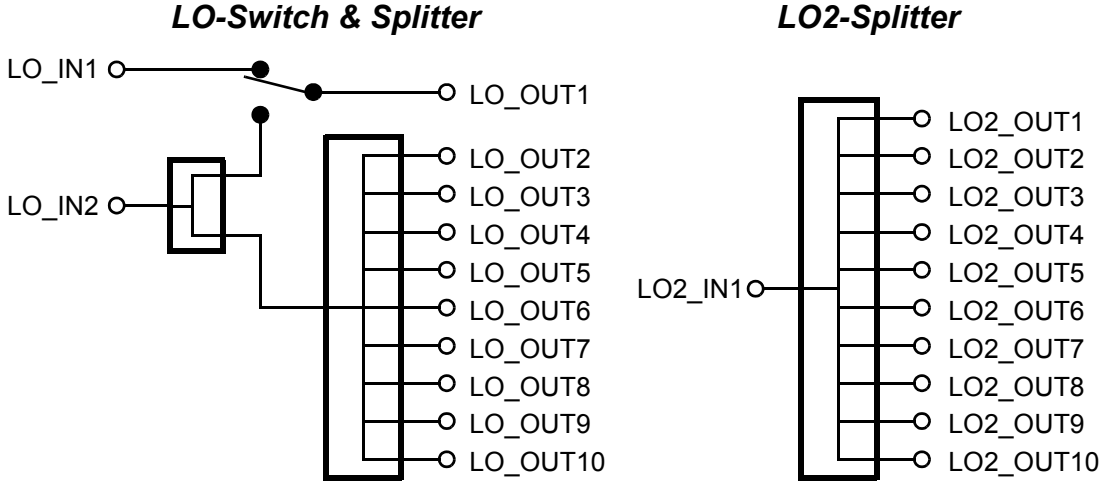
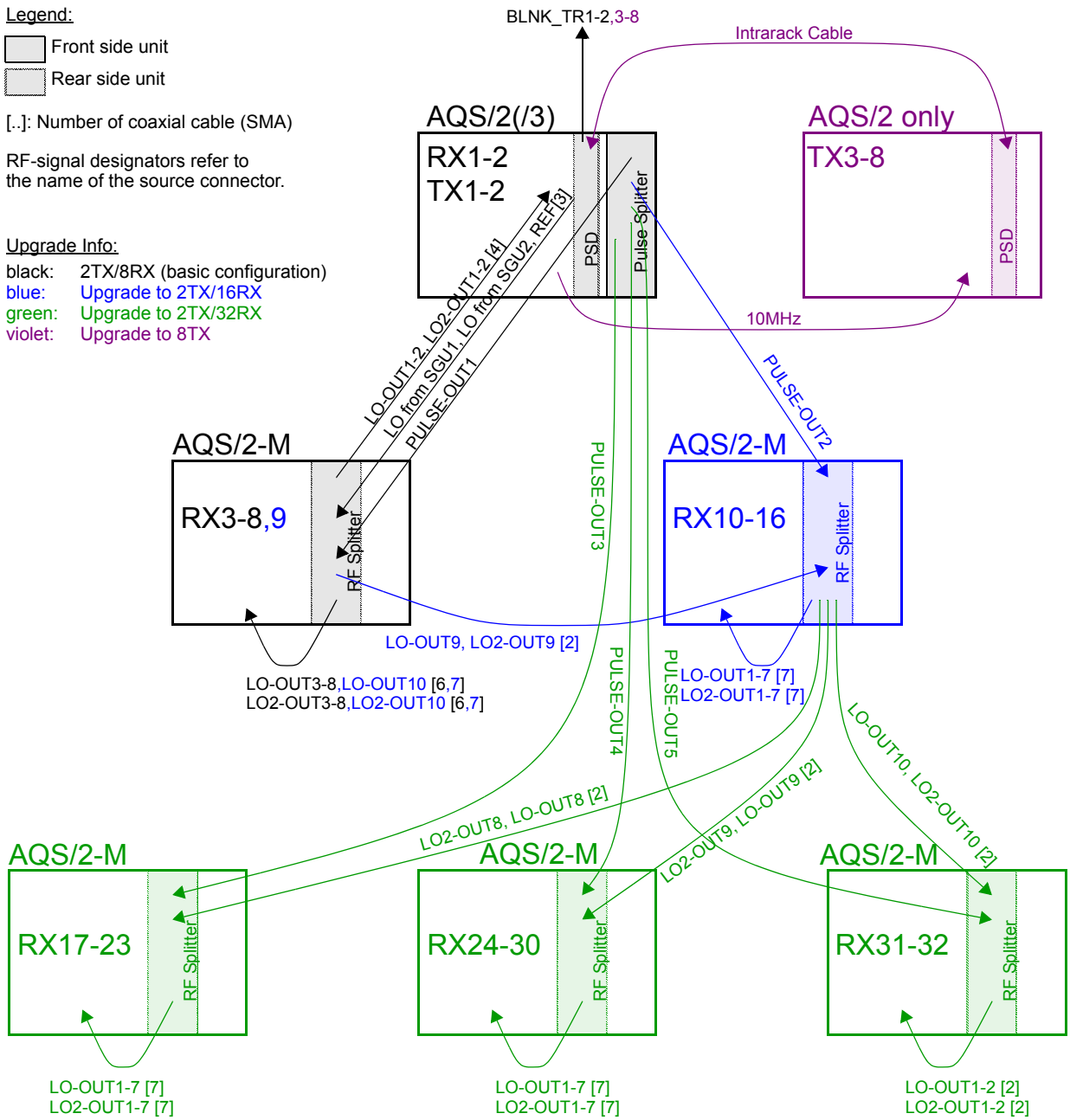
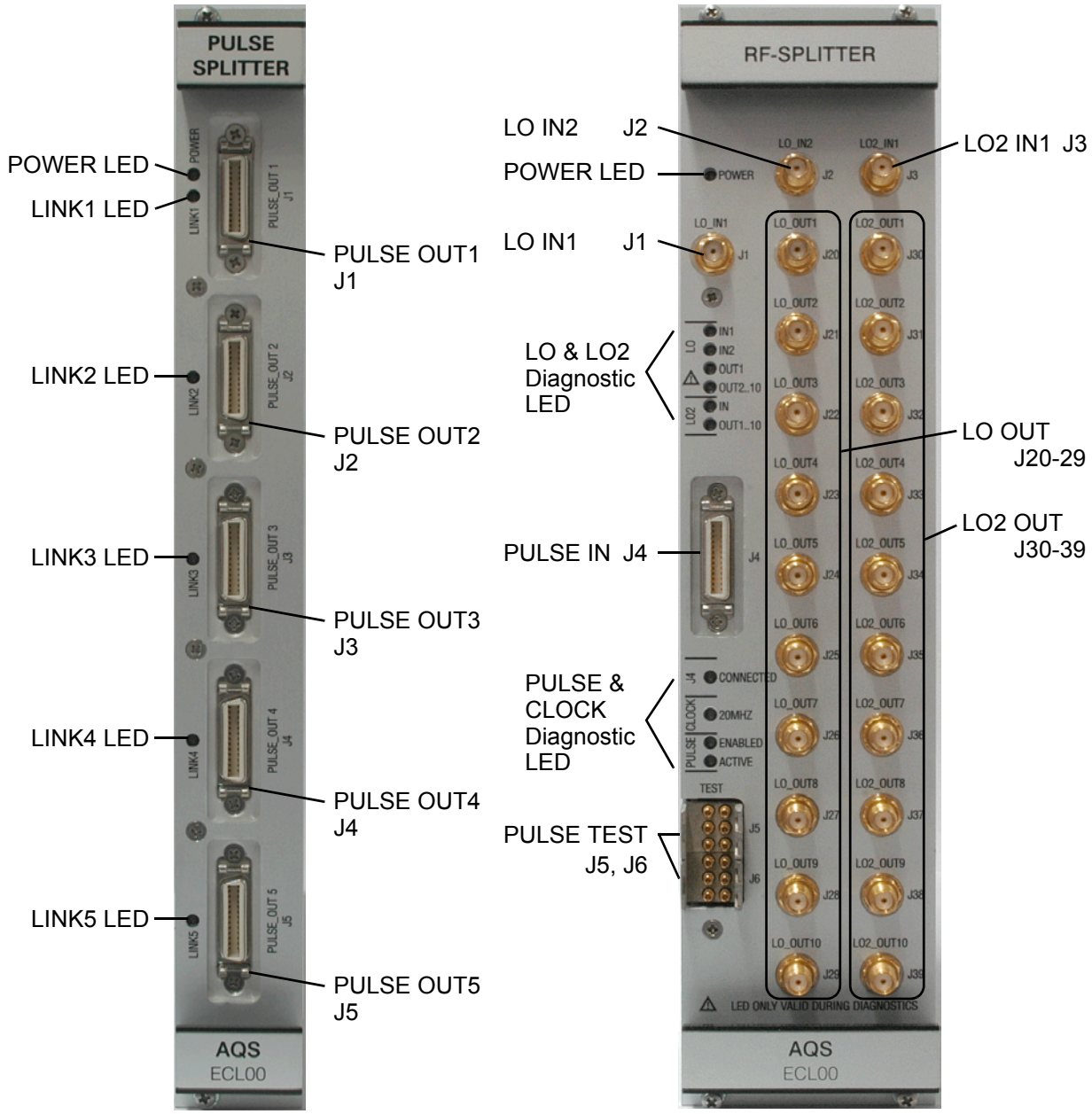


Figure 11.3. PULSE & RF-SPLITTER Wiring Diagram



Front Panel *11.4*

Figure 11.4. AQS PULSE- & RF-SPLITTER boards front panel view



LED Indicators 11.4.1

Table 11.1. PULSE SPLITTER LED Error Description

LED Name	Color	Error Description (LED OFF)
POWER	green	power supply failure
LINK1 LINK2 LINK3 LINK4 LINK5	green	MDR cable not connected to AQS RF-SPLITTER

Table 11.2. RF-SPLITTER LED Error Description

LED Name		Color	Error Description (LED OFF)
POWER		green	power supply failure
LO	IN1 IN2 OUT1 OUT2-10	yellow [a] yellow [a] yellow [a] yellow [a]	no RF-input signal no RF-input signal no RF-output signal no RF-output signal
LO2	IN OUT1-10	green green	no RF-input signal no RF-output signal
J4	CONNECTED	green	MDR cable not connected to AQS PULSE SPLITTER, no pulse output
CLOCK	20MHZ	green	no clock output signal
PULSE	ENABLED ACTIVE	green yellow [a]	pulse buffer disabled, no pulse output no pulse active

a Short pulses may not be visible in OBSERVE mode.

Front Panel Connectors PULSE SPLITTER 11.4.2

J1-J5 PULSE OUT1-5

Pulse and clock output to RF-SPLITTER board. All signals are in LVDS logic (Low Voltage Differential Signal). These signals can only be measured with proper LVDS termination (100Ω differential).

J1 LO_IN1

LO input signal (1Vpp at 50Ω load) from SGU1 or SGU LO-chain. This signal is only present during observe. It can be routed via the internal LO-switch to LO_OUT1 (J20).

J2 LO_IN2

LO input signal (1Vpp at 50Ω load) from SGU2 or SGU LO-chain. This signal is only present during observe. It is split and routed to LO_OUT2-10 (J21-29). It can also be routed via the internal LO-switch to LO_OUT1 (J20).

J3 LO2_IN1

LO2 input signal (1Vpp at 50Ω load) from REFERENCE board. This signal is split and routed to LO2_OUT1-10 (J30-39).

J4 PULSE IN

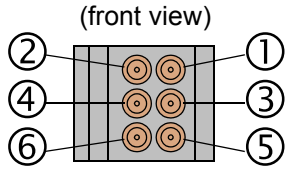
Pulse and clock input from PULSE SPLITTER. All signals are in LVDS logic.

J5/J6 TEST

Pulse and clock output test connector. Signal level = 1/10 TTL at 50Ω load.

Table 11.3. Pining J5/J6 Pulse Test Connector [1]

	J5	
20MHZ_CLOCK	② ①	DWL_ENAB~
RGP_HPPR~	④ ③	RGP_RX~
RGP_ADC~	⑥ ⑤	RGP_LO~
	J6	
SAMPLE_INFO(4)~	② ①	SAMPLE_INFO(3)~
SAMPLE_INFO(2)~	④ ③	SAMPLE_INFO(1)~
SAMPLE_INFO(0)~	⑥ ⑤	INTRLVE_INCR~



J20-29 LO_OUT1-10

LO output signal (1Vpp at 50Ω load) to RXAD or another RF-SPLITTER. These signals are only present during observe.

J30-39 LO2_OUT1-10

LO2 output signal (1Vpp at 50Ω load) to RXAD or another RF-SPLITTER.

1 Pin numbers according to test cable HZ10124 (CABLE 6P300 COAXIPACK ADAP BNC)

Diagnostics 11.5

The input signals of the PULSE SPLITTER and the output signals of the RF-SPLITTER are monitored by diagnostic circuits. Their status is displayed with LED indicators on the front panel of the units. Please refer to ***"LED Indicators" on page 225***.

The same information is accessible for the AQS controller via I^2C bus. The information may be accessed via the DRU web interface.
(Service web of DRU in Slot 1, see Main / Hosted Devices)

Figure 11.5. Pulse Splitter Device and Diagnostic Status

Device Status

Ready

Diagnostic

Diagnostic Testpoint	Description	Status
①	Power Supply Monitor (+3.3V, +5V)	o.k.
②	Pulse Input *	all pulses inactive
③	20MHz Clock Input	o.k.
④	LINK 1 (PULSE_OUT 1 J1)	connected
⑤	LINK 2 (PULSE_OUT 2 J2)	not connected
⑥	LINK 3 (PULSE_OUT 3 J3)	not connected
⑦	LINK 4 (PULSE_OUT 4 J4)	not connected
⑧	LINK 5 (PULSE_OUT 5 J5)	not connected
Refresh	Refresh F5	

click picture to enlarge

* pulses only active during acquisition

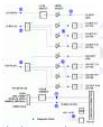
Figure 11.6. RF-Splitter Device and Diagnostic Status

Device Status

Ready

Diagnostic

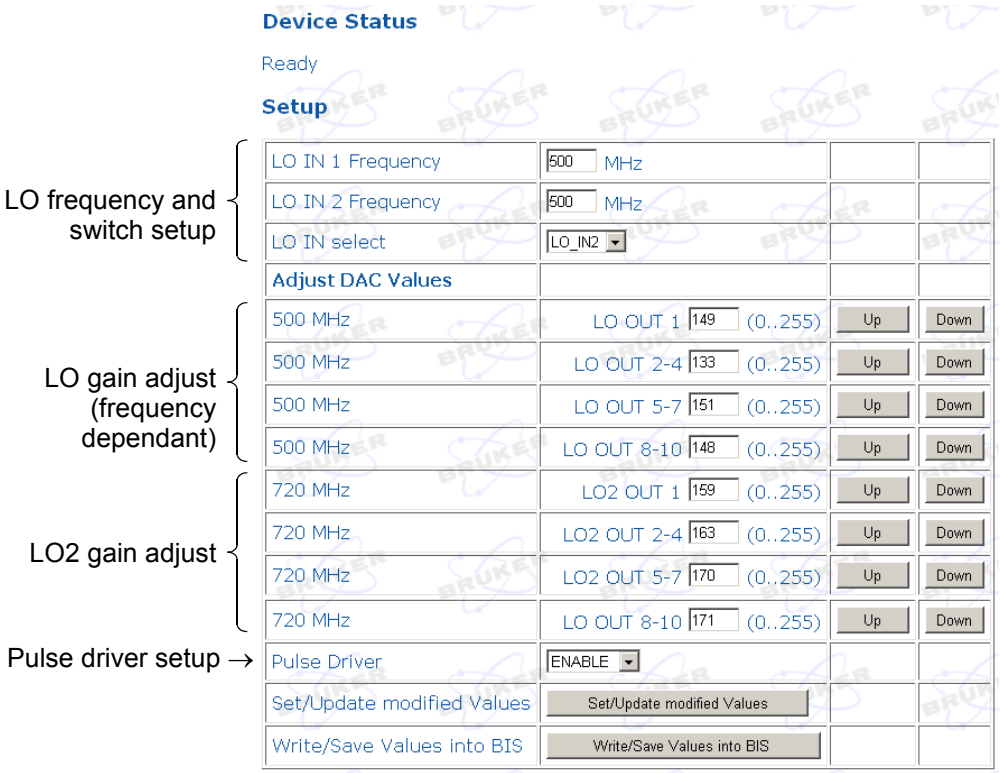
Diagnostic Testpoint	Description	Status
①	LO IN1 *	inactive or failed
②	LO IN2 *	inactive or failed
③	LO OUT1 *	inactive or failed
④	LO OUT 2-10 *	inactive or failed
⑤	LO2 IN	failed
⑥	LO2 OUT 1-10	failed
⑦	Pulse Output *	all pulses inactive
⑧	20MHz Clock Output	ok
⑨	Power Supply Monitor (+3.3V, +5V)	ok
Refresh	Refresh F5	



click picture to enlarge

* LO and pulses only active during acquisition

Figure 11.7. RF-Splitter Setup Window



Setup *11.6.1*

LO IN 1, LO IN 2 Frequency:

- Enter SGU frequency and press [Set/Update modified Values]

The adjust DAC values are set according to the calibration data list stored in the unit BIS. The controller uses the calibration data closest to the entered frequency value. The frequency display changes to the chosen data set.

LO IN select:

LO switch setting (see also ***"LO/LO2- Splitter" on page 222***)

- LO_IN1 = LO_IN1 → LO_OUT1 and LO_IN2 → LO_OUT2-10
- LO_IN2 = LO_IN2 → LO_OUT1-10

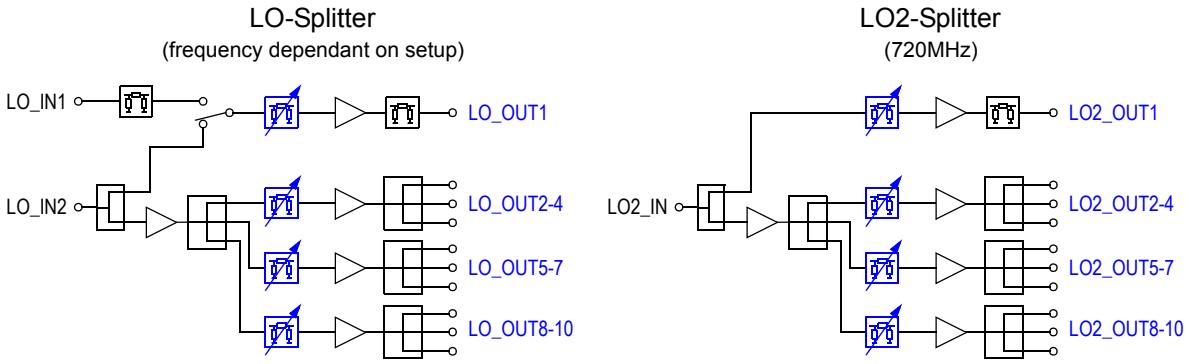
Pulse Driver:

- ENABLE = pulse driver from RF-Splitter to backplane enabled (Default)
- DISABLE = pulse driver from RF-Splitter to backplane disabled (only used when SGU in AQS/2-M Chassis)

Gain Adjust 11.6.2

The gain off the LO and LO2 splitters is adjusted to unity gain at the factory. This includes the connecting cables[1]. However if other cables are used or several RF-Splitters are cascaded, a fine adjust may be necessary. The gain adjusts are bundled as follows:

Figure 11.8. RF-Splitter gain adjust DAC



Gain Adjust Procedure:

- Disconnect the LO(2)_OUT cable from the RXAD and connect it to a power meter
- Check/set the correct RF-Splitter frequency
- Adjust the gain of the LO channel with the [Up] and [Down] buttons (Adjust value see ***"LO-Performance:" on page 230***)
- Save the DAC values with [Write/Save Values into BIS]
- Repeat the procedure for other frequencies or other LO channels

! ***Important Note:***

- Make sure that all unused outputs are properly terminated (50Ω)
- The four gain adjusts of the splitters are somewhat dependant on each other. If one channel is coarse adjusted, the other channels may detune slightly.

Part Numbers and Cables 11.7

- Z104431 AQS PULSE SPLITTER
- Z104432 AQS RF-SPLITTER
- HZ13238 CABLE RD 26P 3M MDR

Test Equipment:

- HZ10124 CABLE 6P300 COAXIPACK ADAP BNC

1 2x CABLE COAX ELSPEC 2000 SMA/SMA (HZ04329)

Technical Data *11.8*

PULSE SPLITTER *11.8.1*

Pulse Performance:

Pulse Input:	+5V TTL Logic Level
20MHz Clock Input:	+2/-2.5V ECL Logic Level
LVDS Output:	LVDS Logic Level

RF-SPLITTER *11.8.2*

LO-Performance:

Input Power:	+4.5 ±0.5	dBm
Frequency Range:	50..800	MHz
Insertion Loss: LO_IN1 → LO_OUT1 (dual LO mode)	0 ±0.5	dB
Insertion Loss: LO_IN2 → LO_OUT1..10	0 ±0.5	dB
LO-Switch Isolation: LO_IN1 → LO_OUT1 (single LO mode)	> 20	dB
LO-Switch Isolation: LO_IN1 → LO_IN2 (dual LO mode)	> 20	dB
VSWR: all Ports	≤ 1.4	

LO2-Performance:

Input Power:	+4 ±0.5	dBm
Frequency:	720	MHz
Insertion Loss : LO2_IN → LO2_OUT1..10	0 ±0.5	dB
VSWR: all Ports	≤ 1.4	

Pulse Performance:

LVDS Input:	LVDS Logic Level
Pulse OUT:	+5V TTL Logic Level
20MHz Clock OUT:	+2/-2.5V ECL Logic Level
Pulse & Clock Test OUT: (at 50Ω load)	1/10 TTL Logic Level

Power Supply / Fuses *11.9*

Both units are powered via their backplane connector from the user bus. For power supply status see ***11.4.1***. The units do not contain any fuses.

Backplane Connector *11.9.1*

Table 11.4. Pining user bus connector PULSE-SPLITTER (Slot 1-10, AQS/2, AQS/3)

	z	a	b	c	d	e	f
1	GND	GND			GND	SAMPLE_INFO0	GND
2	GND		GND	SAMPLE_INFO3	SAMPLE_INFO2	SAMPLE_INFO1	GND
3	GND	GND		I2C_STATUS_INT~	GND	SAMPLE_INFO4	GND
4	GND	20MHZ_CLK_X [a]	GND	INTERLEAVE_INCR~			GND
5	GND	GND	20MHz_CLK_X~ [a]		GND	RGP_LO~	GND
6	GND		GND				GND
7	GND				GND	RGP_ADC~	GND
8	GND		GND			DWL_ENAB~	GND
9	GND				GND	RGP_RX~	GND
10	GND		GND				GND
11	GND				GND	RGP_HPPR~	GND

Key Area

15	GND	SLOT(2)	SLOT(1)	SLOT(0)	GND		GND
16	GND	SLOT(3)	GND	I2C_SDA		GND	GND
17	GND		I2C_BUS_REQ~	I2C_SCL	GND		GND
18	GND		GND	I2C_2_SDA	I2C_2_SCL	GND	GND
19	GND				GND		GND
20	GND		GND			GND	GND
21	GND	P5V					GND
22	GND	P5V					GND
23	GND	P5V					GND
24	GND	P5V					GND
25	GND	P5V					GND

a x = Slot-Nb.

Table 11.5. Pining user bus connector RF-SPLITTER (Slot RF-SPLITTER (AUX2), AQS/2-M Rear Side)

	z	a	b	c	d	e	f
1	GND	SLOT4	SLOT3	SLOT2	SLOT1	SLOT0	GND
2	GND	I2C_SCL	I2C_SDA	I2C_BUS_REQ~	I2C_2_SCL	I2C_2_SDA	GND
3	GND	LOCAL_TX	LOCAL_RX	INTRA_STATUS_INT~	I2C_STATUS_INT~		GND
4	GND						GND
5	GND	GND	GND	GND	GND	GND	GND
6	GND	P12V	P12V	P12V	P12V	P12V	GND
7	GND						GND
8	GND	RESERVE(5)	RESERVE(4)	EMERGENCY_STOP~			GND
9	GND						GND
10	GND	P5V	P5V	P5V	P5V	P5V	GND
11	GND	GND	GND	GND	GND	GND	GND

Key Area

15	GND	GND	GND	GND	GND	GND	GND
16	GND	P9V	P9V	P9V	P9V	P9V	GND
17	GND	N9V	N9V	N9V	N9V	N9V	GND
18	GND	GND	GND	GND	GND	GND	GND
19	GND						GND
20	GND						GND
21	GND	GND	GND	GND	GND	GND	GND
22	GND			SAMPLE_INFO(0)	DWL_ENAB~	RGP-LO~	GND
23	GND	GND	SAMPLE_INFO(2)	SAMPLE_INFO(1	GND	RGP_ADC~	GND
24	GND	20MHZ_BACK_IN	GND	SAMPLE_INFO(3)	INTRLVE_INCR~	RGP_RX~	GND
25	GND	GND		SAMPLE_INFO(4)	GND	RGP_HPPR~	GND

AQS 2H TX 12

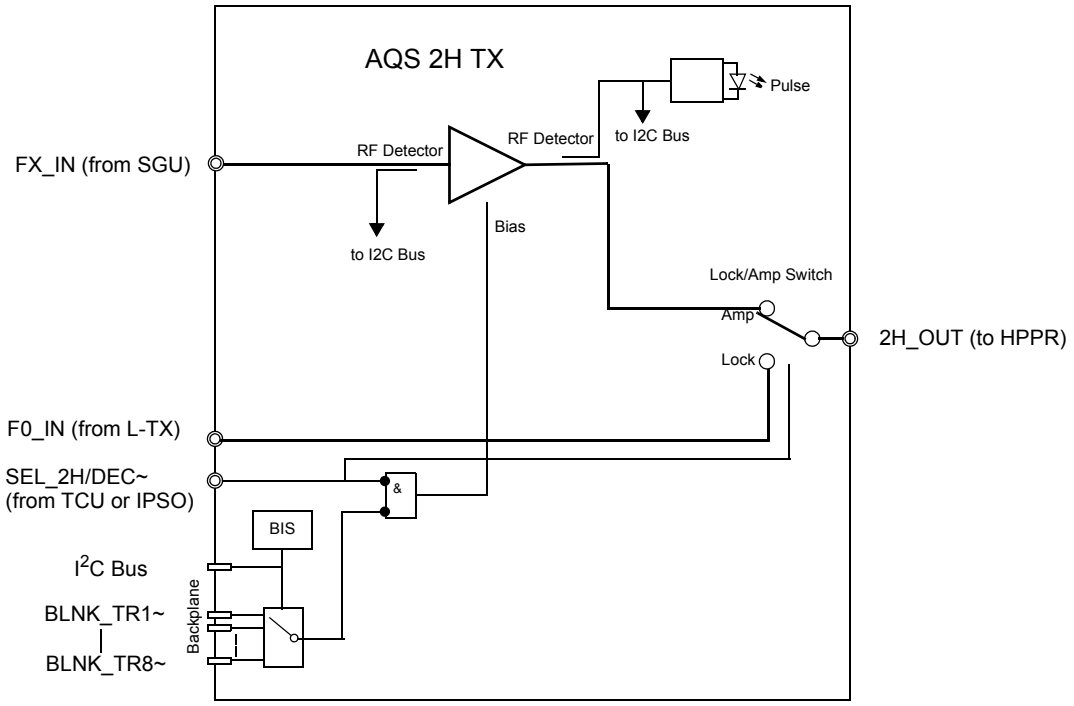
Function/Description 12.1

This AQS unit serves as a 80W power amplifier for deuterium. The unit is available in two frequency ranges for 300-400 and 500-1000MHz systems. This 2H-TX are intended to fit into the AQS/3 chassis in combination with a BLA2BB or in combination with external power amplifiers.

Features:

- 6TE wide AQS unit
- Included Lock-Switch
- Blanking pulse direct from AQS backplane (source software switchable, for setting Amplifier Housing see ***"Default values" on page 243***)
- Overheat protection
- Software readable RF input detector
- Software readable RF output detector

Figure 12.1. AQS 2H TX Blockdiagram



Front Panel *12.2*

All RF input and output signals of the AQS 2H TX are connected via SMA connectors on the front panel.

Two LEDs indicate the correct DC power supply (28V) and an output RF pulse exceeding approximately 1W. The pulse LED will be on at least about one second even for a very short RF pulse.

Part Numbers 12.3

Table 12.1. Part Numbers

Part	Description
Z103550	AQS 2H-TX BD 200-400
Z103551	AQS 2H-TX BD 500-1000

Technical Data 12.4

Table 12.2. Specifications

	Z103550 ECL>=01 (200-400)	Z103551 ECL>=00 (500-1000)
Minimum pulsed Output Power	>80W	>80W
1dB compression	80W typ.	80W typ.
RF Rise and Fall Time	<100ns	<100ns
Noise Figure	<7dB	<7dB
Amplitude Droop	<+-5%	<+-5%
Blanking Delay	<1us	<1us

AQS Controller 13

Introduction 13.1

The AQS controller is a part of the DRU firmware. It acts as a communication router for all RF boards inside the AQS Chassis. Furthermore the AQS controller hosts the firmware of all I^2C boards, e.g. reference board, AQS internal amplifiers, routers and splitters.

In case of a multiple receiver system, only the DRU placed in Slot 1 will start the AQS Controller.

At power-up of the AQS Chassis, the AQS controller executes a rack scan and initializes all boards.

To access the different RF boards in the chassis, two different tools are necessary:

1. UniTool for
   - AQS Controller
   - SGU/2
   - RXAD
   - AQS internal amplifiers
2. Web browser for
   - AQS/2, AQS/2-M and AQS/3 Chassis
   - Pulse- and RF Splitter
   - SGU/2
   - RXAD
   - AQS internal amplifiers
   - AQS internal preamps

UniTool 13.2

For service purposes BRUKER has developed an universal service tool (named UniTool) that allows access to boards with UniTool support for diagnostic, check and firmware upgrade over the RS485 serial bus (SBSB, description can be found on ***page 15***).

The UniTool acts as a browser, all menus are provided by the units themselves. Board specific UniTool access can be achieved by starting the UniTool with the matching SBSB address (for addresses see ***"AQS address mapping" on page 238***)

The following devices are supported by UniTool:

- AQS Controller (virtual, provided by the DRU)
- all SGU/2

- all RXAD variants
- all AQS internal amplifiers (reduced function)

! ***The AQS Controller is a (virtual) device with its own SBSB address, although its function is provided physically on the DRU hardware. The AQS Controller is a separate task of the DRU firmware.***

The AQS Controller function can be accessed on the AQS Controller address decimal 32.

Problems starting UniTool? *13.2.1*

UniTool is running on the SBSB libraries from XWINNMR or TOPSPIN, so a complete installation, valid paths and environment are necessary. Essentials for serial RS-485 / SBSB communication:

1. The directory <XWINNMRHOME>/conf/instr/spect/rs232_device/ must exist

In this directory the corresponding files must be created and edited: aqs and preamp1, e.g.

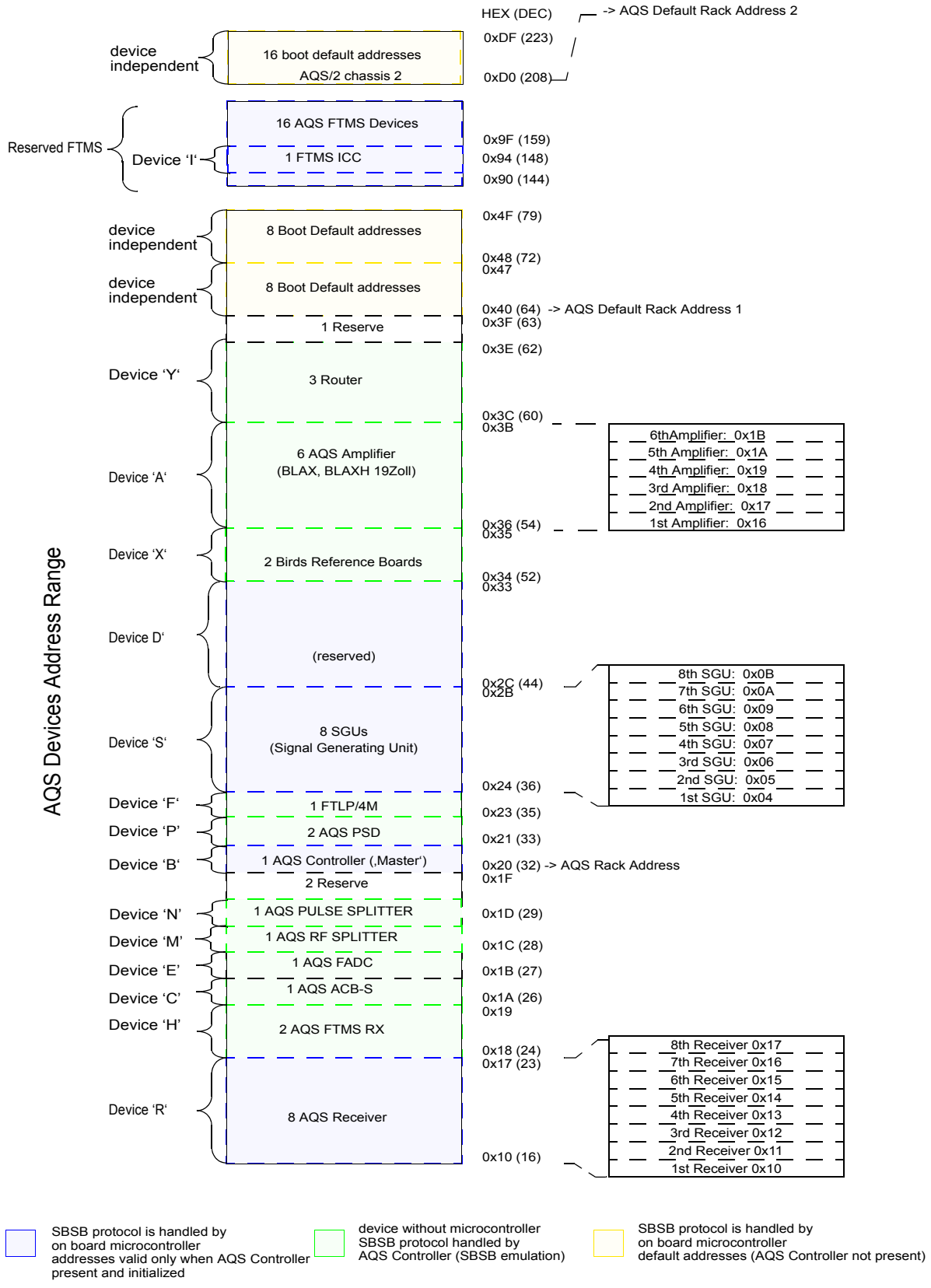
AQS address mapping *13.3*

Configuration and SBSB addresses can be found in

the ../conf/instr/<curinst> directory in the file uxnmr.info

or by ***"Identify your chassis configuration" on page 240*** using the UniTool.

Figure 13.1. SBSB addresses



Identify your chassis configuration 13.4

There are now two ways to identify your chassis configuration. The traditional way with the UniTool and the new way with the AQS Service web.

AQS Service web 13.4.1

The web page „AQS Control Overview“ („Hosted Devices“ → „AQS Overview“) shows all devices in the chassis controlled by the AQS Controller.

If there are internal Preamps (Preamps directly connected to the DRU) then they will be shown on the web page „HPPR/2 Control Overview“ („Hosted Devices“ → „HPPR/2 Overview“).

UniTool 13.4.2

The chassis configuration can be identified using UniTool:

1. Open a UNIX shell or the command prompt in the BRUKER Utilities folder when using Windows
2. Start the UniTool: xwinnmr -e UniTool
3. -> aqs, confirm
4. -> decimal address for the AQS Controller is 32, confirm
5. Choose -> [1], Rack Configuration, confirm

With the AQS Controller UniTool menu the chassis configuration can be read.

Figure 13.2. Determine chassis configuration

```
45% xwinnmr -e UniTool
Enter device name ['?' for details]  (aqs) >
Enter decimal SBSB address for board in AQS rack (36) > 32
device name taken from already existing configfile: /dev/tty10

B r u k e r  U n i T o o l
   Version: 1.0
   Compilation date: 000921

W A R N I N G:
   This is a hardware level debug tool.
   Improper operation may damage your hardware.

Connecting SBSB address 32 (0x20).

>>>   Rackmaster  Menu   <<<
============================
[0] Init Rack
[1] Rack Configuration
[2] Rack Delete Error
[3] Rack Querry Request
[A] Service Functions
[X] eXit UniTool
    your choice:1
```

AQS Board Type Codes *13.4.1*

Board type codes are shown in ***Table 13.1.*** Boards that are usually not in a system with IPSO are marked gray.

Table 13.1. Birds Board Type Identifier Codes

board type	board type	board description	BRUKER number
0x00	*0*	*SGU-C (frequency range 5..430MHz, print index C)* *SGU (regular frequency range 5..<643.45MHz, print index D)*	*Z003329* *Z003642*
0x01	1	board not inserted	
0x02	*2*	*AQS Reference Board for AQS Receiver (REF400)*	*Z003265*
0x03	*3*	*AQS Reference Board with 22MHz IF output for RX22 (REF400-22)*	*Z003351*
0x04	4	AQS Router Combiner	Z003624
0x05	5	AQS BLA2BB 150-60 dual amplifier 20-400MHz	W1345049
0x06	6	AQS BLAX300 single 300W X Amplifier	W1345052
0x07	7	AQS Controller	
0x08	8	AQS FTLP/4M filter board	Z002812
0x09	*9*	*AQS ACB standard*	*H9488*
0x0A	*10*	*AQS PSD power supply distribution board*	*H9530*
0x0B	*11*	*AQS RECEIVER BOARD RXAD FTMS*	*Z102501*
0x0C	12	AQS FTMS PSD power supply distribution board	A3142
0x0D	13	AQS FADC	H9685
0x10	*16*	*AQS SGU 400 (frequency range 5..430MHz)*	*Z003642* *ab ECL2.0*
0x11	17	AQS SGU/2 400 (frequency range 5..430MHz)	Z103080
0x18	*24*	*AQS SGU 600 (frequency range 5..<643.45MHz)*	*Z003831*
0x19	25	AQS SGU/2 600 (frequency range 5..<643.45MHz)	Z103081
0x28	*40*	*AQS SGU 1000 (extended frequency range 5..1072.625MHz)*	*Z003330* *ECL2.0* *and newer*
0x29	41	AQS SGU/2 1000 (extended frequency range 5..1072.625MHz)	Z103082
0x30	*48*	*AQS SGU-FTMS (ICR frequency range 0.003..10MHz print index D)*	*Z003643*
0x31	49	AQS SGU/2 FTMS (ICR frequency range 0.003..10MHz)	Z103083
0x42	66	AQS RXAD600 (standard frequency range 5..645MHz)	Z102117

Table 13.1. Birds Board Type Identifier Codes

board type	board type	board description	BRUKER number
0x52	82	AQS RXAD1000 (extended frequency range 5..1077.5MHz)	Z102118
0x60	*96*	*AQS RX-E (extended frequency range 5..1077.5MHz)*	*Z003689*
0x61	*97*	*AQS RX-BB (extended frequency range 5..1077.5MHz)*	*Z003689*
0x62	98	AQS RXAD-BB (extended frequency range 5..1077.5MHz)	Z102119
0x72	114	AQS RXAD400 (base frequency range 5..430MHz, ...)	Z102116
0x80	128	AQS DRU	
0xC0	192	AQS Reference Board for AQS Receiver RX600 (REF600)	Z003936
0xC1	193	AQS Reference Board for AQS Receiver RX1000 (REF1000)	Z003937
0xC2	*194*	*AQS Reference Board with 22MHz IF for RX22 (REF600-22)*	*Z003938*
0xC3	*195*	*AQS Reference Board with 22MHz IF for RX22 (REF1000-22)*	*Z003939*
0xC4	196	AQS BLA2BB 150-60 dual amplifier 20-500MHz	W1345072
0xC5	197	AQS 1to4 Router	Z101247
0xC6	198	AQS/2 Chassis	Z101618
0xC7	199	AQS 2H-TX BD 200-400	Z103550
0xC8	200	AQS 2H-TX BD 500-1000	Z103551
0xC9	201	AQS REF/2 1000	Z104236
0xCA	202	AQS RF SPLITTER BOARD	Z104432
0xCB	203	AQS PULSE SPLITTER BOARD	Z104431
0xCC	204	AQS BLAXH300 300/50 500-600	Z1235056
0xCD	205	AQS PSD/2	H14107
0xCE	206	AQS/2-M Chassis	Z103493
0xCF	207	AQS PSD/3	H14109
0xD0	208	AVANCE CONSOLE NB-E WIRED (NanoBay Chassis)	Z108356
0xD1	209	AQS/3 Chassis	Z106171
0xD2	210	AVANCE ACQ SYSTEM NANOBAY FTMS (NanoBay Chassis)	Z105194

New configuration of the AQS amplifiers *13.5*

! ***Remember that Unitool and AQS Service Web are hardware level debug tools. Improper operation may damage your hardware. Please read the following lines carefully.***

According to the document “BIS Groups and Values” (Andreas Hünnebeck (AH), version 2.6 and higher), the amplifiers provide a housing information in its BIS that allows the software to determine an SBSB address.

Later versions of the amplifiers have this entry in their BIS. If an error message like

"no amplifier housing information in BIS, using default address " or

"multiple amplifier housing information in BIS, using default address "

is printed out you should read the following lines.

For future 3 channel configurations with internal AQS amplifiers, housing information must be programmed in the BIS.

Default values *13.5.1*

Default values in the amplifier BIS should be:

BLA2BB: Housing, Hsg = 1 (amplifier 1)

BLAX300: Housing, Hsg = 2 (amplifier 2)

AQS 2H-TX: Housing, Hsg = 3 (amplifier 3) for NanoBay console
Housing, Hsg = 8 (amplifier 8) for all other console types

To change the housing setting see ***13.5.2*** and ***13.5.3***.

In a 2 channel AV with one BLA2BB without a housing entry, no error or warning message is given (backward compatibility to most used configurations). BLA2BB is amplifier 1.

For a 3 channel AV with BLA2BB and BLAX300, where both amplifier do not have a housing entry, warning messages are given and default values are set. These values can be modified using the UniTool with the BLA SBSB address.

Default SBSB addresses, ***when no housing*** is originally programmed

1. BLA2BB in slot 8: 0x36
2. BLA2BB in slot 8, BLAX300 in slot 6 (on the left side of BLA2BB):

   BLA2BB: 0x36 (decimal 54)

   BLAX300: 0x37 (decimal 55)
3. AQS 2H-TX in slot 9: 0x38 for NanoBay console
   0x3D for all other console types

Check the addresses before changing any entry. This can be done with the AQS Service Web as follows:

1. Start a Webbrowser and open the AQS Service Web page. (see ***13.6***)
2. Go to the „AQS Control Overview“ page („Hosted Devices“→„AQS Overview“).

or with the UniTool:

1. Start the UniTool in a Shell: `xwinnmr -e UniTool`
2. -> `aqs`, confirm
3. -> decimal address of the AQS Controller is **32**, confirm
4. Select 1, Configuration-> a list is shown (see ***"Identify your chassis configuration" on page 240***) with the SBSB addresses of the devices.

Adding Housing Setting (via UniTool) *13.5.2*

Follow these instructions to add the housing information to amplifiers with old BIS.

Conditions:

- BLA2BB in Slot 8
- BLAX300 in Slot 6

1. Power up the AQS Chassis
2. Start the UniTool in a Shell: `xwinnmr -e UniTool or topspin -e UniTool`
3. -> `aqs`, confirm
4. -> SBSB address of the amplifier BLA2BB is hex 0x36 resp. decimal **54**, confirm,
5. Change at menu Point 2 the housing information (1 for BLA2BB recommended). The setting is saved automatically. Exit UniTool.
6. Start the UniTool in a Shell: `xwinnmr -e UniTool or topspin -e UniTool`
7. -> `aqs`, confirm
8. -> SBSB address of the amplifier BLAX300 is hex 0x37 resp. decimal **55**, confirm,
9. Change at menu Point 2 the housing information (2 for BLAX300 recommended). The setting is saved automatically. Exit UniTool.
10. Perform an AQS power down
11. Power up the AQS chassis and initialize the spectrometer with “cf”
12. Check SBSB addresses with UniTool on AQS Controller address 32:
13. BLAX300 in Slot 6 with housing 2: 0x37, amplifier is AMP2
14. BLA2BB: in Slot 8 with housing 1: 0x36, amplifier is AMP1

Adding Housing Setting (via AQS Service Web) *13.5.3*

1. Power up the AQS Chassis
2. Start a web browser and open the AQS Service Web page. (see ***13.6***)
3. Go to the „AQS Control Overview“ page („Hosted Devices“ → „AQS Overview“). There you can see a table entry for each amplifier. Follow the links to the device configuration page.
4. Select the housing and write the settings into the Amplifier.

5. Go back to the „AQS Control Overview“ page and perform a complete AQS-Rack scan or power the AQS Chassis down and up again.
6. Check the addresses of all amplifiers on the „AQS Control Overview“ page.
7. Remember that you have now changed the configuration and you have to perform a „cf“.

AQS Service Web 13.6

The following AQS devices in the AQS Chassis are currently supported by the AQS Service Web:

- Chassis (AQS/2, AQS/2-M and AQS/3)
- SGU/2
- RXAD
- Reference Boards
- Amplifiers (BLA2BB, BLAX300, BLA2HTX)
- Internal preamplifiers (HPPR/2)
- RF Splitter (in AQS/2-M Chassis)
- Pulse Splitter

When a DRU is AQS Controller the „DRU service web“ will become the „AQS service web“. You can get access to the „AQS Service Web“ like to a „DRU Service Web“ (see ***9.3.1***). The web pages have been testet with Micorosoft Internet Explorer and Mozilla Firefox.

Figure 13.3. Access to the devices in the AQS Chassis.

Figure 13.4. Hosted Devices

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