AQS Technical Manual with DRU Systems

(AVANCE II)

Version 003

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Safety Instruction 1

Terms and symbols 1.1

WARNING: Disregard of this may lead to personal injury.

NOTE: Hint for good operating practice.

Figure 1.1. High voltage!

Indicates dangerous voltage. Do not open cover with this label!

Figure 1.2. Dangerous device!

Instruction manual symbol. It is necessary for the user to refer to the manual prior to the use of marked items.

Figure 1.3. Electrostatic sensitive Device!

Observe precautions for handling.

Figure 1.4. Protective ground (earth) terminal

Used to identify any terminal which is connected to the external protective conductor for protection against electrical shock in case of fault.

Disclaimer 1.2

The following general safety precautions must be observed during all phases of operation and service of the AQS system. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture and intended use of the AQS system.

BRUKER assumes no liability for the customer‘s failure to comply with theses requirements and is therefore not responsible or liable for any injury or damage that occurs as a consequence of non-approved manipulations on the AQS system.

Emergency 1.3

The mains switch on the AQS chassis front serves as an EMERGENCY OFF. It powers down the systems.

Personnel safety *1.4*

Ground connection *1.4.1*

WARNING: To minimize shock hazard the AQS chassis must be connected to an electrical ground.

The electronics cabinet is equipped with a three-conductor ac power cable. Do only use power cables approved by BRUKER or compliant with IEC safety standards.

Technically qualified personnel only *1.4.2*

WARNING: Installation and servicing should only be done by BRUKER qualified personnel. Always disconnect power cable before servicing. Under certain conditions dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

NOTE: Operating personnel must not remove chassis covers except as described in this manual. Do not replace AQS units with mains switch turned on.

User interface, system messages, and manuals require a good understanding of the English language.

Electrical safety *1.4.3*

The AQS systems's degree of protection against electrical hazard complies with IEC IP20, i.e. all electrical parts are protected against touching.

WARNING: All electrical connectors must be used as supplied by BRUKER. Do not substitute them by other types.

Lifting the AQS chassis *1.4.4*

WARNING: At least two people are needed to insert and remove the AQS chassis from the electronics cabinet. A fully equipped AQS system can weight in excess of 50kg.

NOTE: Remove some or all of the AQS units from the chassis prior to handling to reduce weight.

Cleaning *1.4.5*

WARNING: Always switch power off and disconnect the power cable before cleaning. Never power on until all surfaces are completely dry.

Clean the outside of the AQS chassis and units with a soft, lint-free cloth dampened in water. Do not use any detergent or other cleaning solvents.

Acquisition System with RXAD and DRU 2

Introduction 2.1

The first Acquisition System (AQS) was introduced into the market in 1999. The main reason was the development of a BRUKERs own synthesizer (SGU) based on a novel channel concept. The construction of the former AQR and AQX units have been unified, higher integrated and more standardized. During the last years the architecture has been completed with additional and more diversified configurations based still on a unified hardware and software concept. With this it was possible i.e. to enhance Solids configurations (RX-BB instead of SE451), to higher integrate High Resolution spectrometer electronics (AQS integrated LNA preamplifiers instead of HPPR), to generate new MRI solutions (Pharmascan and Biospec with multiple RX) and standardize the FTMS platforms (SGU FTMS).

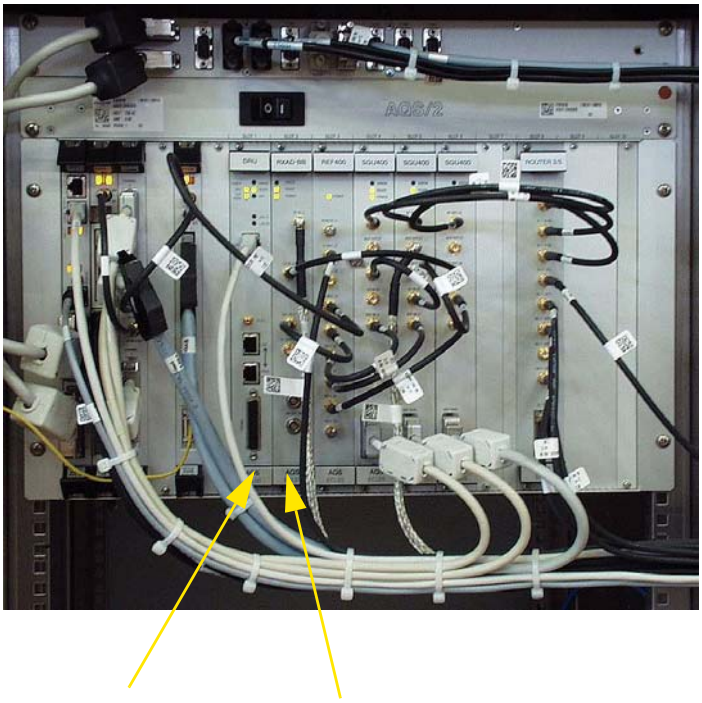
The new AQS/2 chassis is now the consecutive development of the well proven AQS chassis and still allows almost all of the former configurations but also offers new configurations like the new digital receiver electronics with the recently developed **RXAD** (receiver with integrated analog to digital converter) and **DRU** (digital receiving unit). Conspicuous signs are the vanished analog and digital interconnections between receiver, A/D converter and digital filters at the front side of the new AQS/2 system.

At a second view one can remark that the VME bus section has been reduced by two slots. Using a modern, distributed connectivity via Ethernet driven JAVA applications (TopSpin) with direct communication and data transfer to the workstation, this is giving access to new and more open system concepts. For instance, new HTTP based units can be easily accessed and serviced by a commercially available web browsers.

Features

- Prepared for up to 10 6TE RF and other NMR electronic units
- Support of the recently new developed **RXAD** and **DRU** digital receiver electronics
- Expandable with additional, integrated power amplifiers (i.e. AQS 2H-TX)
- Provisions made to increase the number of RX channels for MRI applications (5 and more)
- Support of mixed systems (HR and multiple RX imaging) by a versatile backplane pulse routing under software control
- Increased flexibility by the operative introduction of the „scan control“ mechanism (sample information bus)
- Fan rotation supervision and easy serviceable fan tray

Figure 2.1. 3 Channel AQS/2 with RXAD and DRU



Acquisition control

By the elimination of the acquisition control and data transfer via the CCU and VME bus, a new and more powerful synchronization channel has been introduced. The already in the basic channel concept defined „sample information bus“ is now being used for the control of the realtime actions in the digital receiver chain. Synchronous scan information (e.g. receiving phase, file handle, wobble control, accumulation and display management) is distributed over this bus from the acquisition main controller (timing control) via the observe SGU. This bus replaces and enhances the well working AQ Bus within the new receiving concept.

Analog to Digital Conversion

Newest A/D converter technologies allow sampling rates up to 20MHz with even very high dynamic ranges. In conjunction of the tremendous progress in digital signal processing (DSP technology) and very fast and highly integrated flexible digital hardware (FPGA based) it allows enormous higher DQD bandwidths and with that less audio artefacts as anyone could expect in earlier times.

Automatic DC compensation and higher frequency digital local oscillators (NCO, numeric controlled oscillators) but last but not least better performance is also achieved by continuos A/D converter operation (non start/stop mode). Inherent thermal settling of the A/D chips by using start/stop mode disappears. The DWELL clock is derived directly from the basic phase noise minimized spectrometer reference increasing the spectral purity. Finally the DWELL clock generation for such a system is much more easier, because the gating is handled in the DSP by managing the data flow using previously mentioned ‚scan control‘.

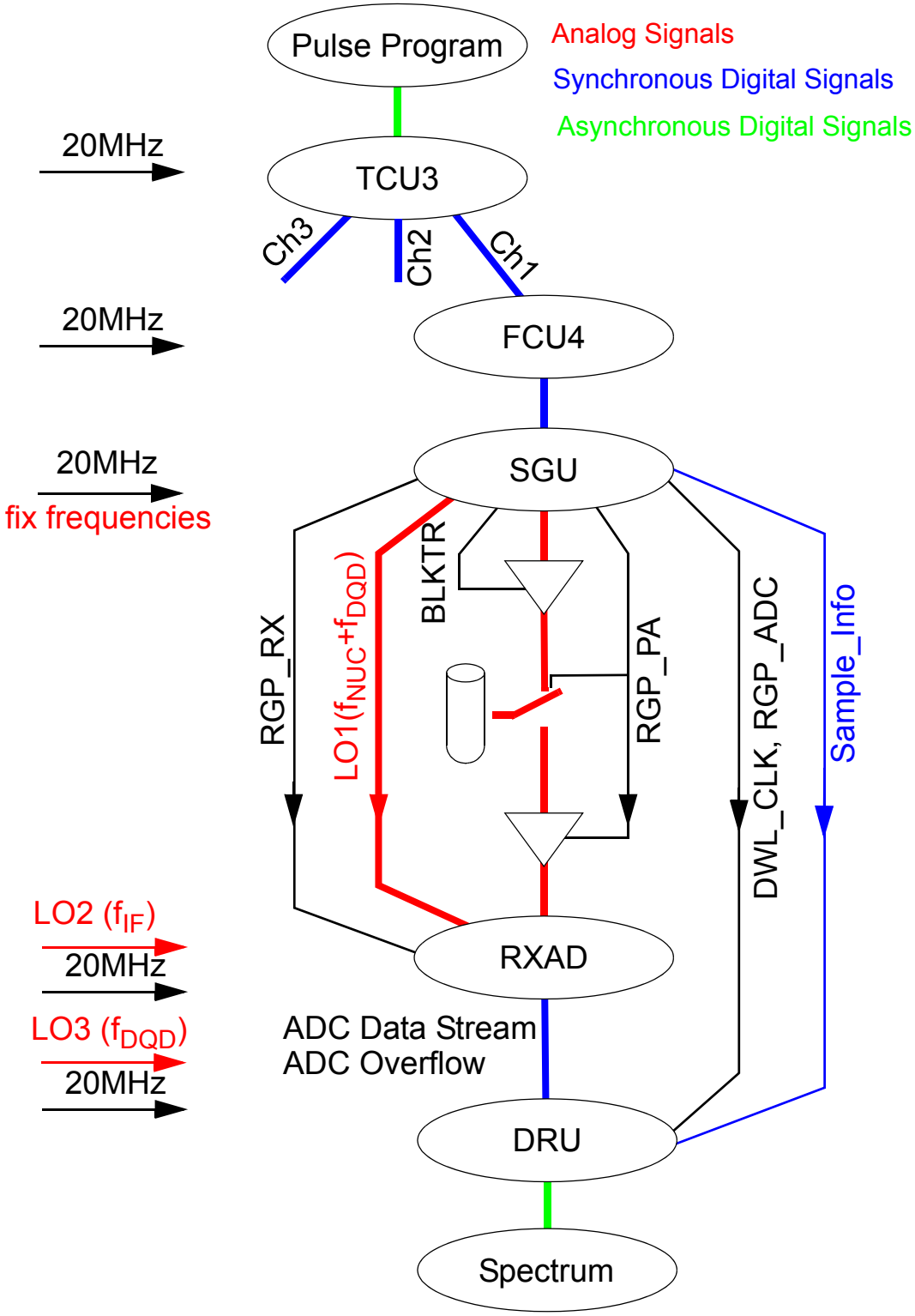
The channel concept *2.2*

With the introduction of the AQS/2 Chassis, the well proven AQS channel concept has been further extended by the replacement of the former receiver units (RX-22, SADC, HADC/2, FADC, FTLP-4M, RCU) with the recently developed **RXAD** and **DRU**.

It was possible to reduce the control and routing of important channel related real time events and analog signals to only a few dedicated units. All these channel oriented signals (RF signals, shaping, gating and blanking pulses, dwell clocks etc.) are generated in the so called SGU (**S**ignal **G**eneration **U**nit) under full timing control of pulse programs. The SGU is physically controlled by the FCU4 (a last successor of the AQX FCU) via a digital high speed link.

The following diagram shows the consequent implementation of this concept. The number of analog interconnections is reduced to a few dedicated units. All important RF signals, blanking pulses and dwell clock are channel related and follow a straightforward channel philosophy. In this way, extended and independent multi channel operation can be performed in a much more transparent way. Less Interfaces and units allow a general guaranteed stability and reliability.

The channel concept



AQS/2 signal and information paths 2.3

Before one can go into details, it is important to distinguish and understand the three different signal categories used in the AQS/2 Chassis (as already introduced with the first AQS Chassis):

Analog signals: These signals are typically RF or audio signals, which have no time and amplitude discrete values and may be easily checked with a scope. Examples of such signals are the local oscillator signals (i.e. LO1 and LO2) or the NMR signal at the input of the digitizer.

Synchronous signals: These signals are the basic spectrometer auxiliary, control and timing signals for each transmit but also receive channel. They are all derived from one master oven controlled oscillator (OCXO). Most important are the 10MHz, 20MHz, but also every transmitter blanking and the receiver gating pulse.

Asynchronous signals: Asynchronous signals fall into the category of general information transfer protocol signals. These signals are represented by examples like Ethernet, RS232, RS485 and I^2C.

Basics of the AQS/2 Chassis 2.3.1

The AQS/2 has been designed to support more than one AQS/2 chassis to allow a very flexible extension of NMR transmitting channels, multireceiving capabilities and setting up numerous different NMR application spectrometers configurations. To manage all these configurations, one has to select the required operation by selecting the appropriate rack address only. The rack address can be set with jumpers on the rear side of the AQS/2 backplane (***"Rackadress Settings" on page 74***.)

Viewing the AQS/2 chassis from front side, on left side a conventional VME32 bus with the BRUKER extension (AQ-Bus, F-Bus) for 6 slots is incorporated. On right side, the extended AQS/2 User bus is able to supply as will be shown later on a lot of different AQS functional units (signal generators, receivers, preamplifiers, amplifiers, etc.).

Every slot on the AQS/2 User Bus backplane is hardware coded, so that every unit can be addressed via its unique slot address. The AQS/2 User Bus backplane connector pin assignment is identical for all ten 6TE slots. That means each common signal respectively signalpath is accessible on every slot (exceptions are power supply for BLA2BB, the data transfer to the DRU and signals for the reference board).

RS485 Buses (SBSB[1]), Intra Rack Bus 2.3.2

The AQS/2 incorporates two independent SBSB buses called SBSB_1 and SBSB_2. The first one represents the system tty10, the second one the tty20.

The RS485 buses are originating at the CCU (SBSB_1 and SBSB_2), but may be in future also be under control of other AQS Controller capable boards (i.e. DRU). They are hard-wired internally in the backplanes and are not any more accessible

1 SBSB: serial BRUKER SPECTROSPIN bus (historical name)

on the AQX RS plug. The SBSB_1 is galvanic isolated (SBSB_1_TTL) on the ACB standard (ACB-S) or PSD, depending on the configuration of the AQS/2 rack. This reduces interferences between NMR RF, audio and digital units.

The SBSB_1 is the main SBSB which controls most of the NMR units. These are all SGUs, all RXADs and the HPPR/2 preamplifier system. The SBSB_2 is used for the control of the ACB and its connected power amplifiers (BLA).

One SGU, which is typically situated in slot 3 in the AQS/2 User Bus (3rd from the left), serves as the 'rack master' or *AQS Controller*. This *AQS Controller* overtakes general control and configuration tasks in the initialization phase which must be setup according to the rack address. This AQS Controller SGU recognizes its position automatically and switches into AQS Controller mode whereas all other SGUs are set to slave mode. The AQS Controller SGU reacts to ‚master' commands (e.g. power up, init...) incoming via the SBSB_1 from the spectrometer control software through the CCU (VME backplane to user bus backplane to ACB-S). It also reacts to incoming virtual SBSB commands for devices which do not have own SBSB interfaces (refer to I2C bus).

Internal AQS/2 communication between AQS/2 SBSB devices like slave SGU's and RXAD (e.g. clearing power up errors etc.) is done via the so called Intra-Rack bus (serial asynchronous bus, TTL levels) with the AQS Controller SGU as bus master.

The AQS Controller SGU is not only AQS Controller, but it behaves identically to a slave SGU and interprets and executes the commands accepted from the corresponding channel setup (i.e. edasp in TopSpin). It operates as physical channel (e.g. SGU1). As SGU1 it reacts to RF channel1 commands transferred via the SBSB_1, as well as all other SGUs' react to their corresponding RF channel commands.

I2C buses and I2C adresses *2.3.3*

For functional units without an intelligent and powerful micro controller, because it doesn't calculate to have an own costly controller, a multi master capable I2C connectivity is used. The AQS Controller (i.e. SGU) drives these units via different I2C buses and plays so the role of a virtual unit controller for each non microprocessor unit. Such units are the AQS BLA2BB, the AQS Router, AQS REF but more may be coming soon. Incoming spectrometer SBSB commands from SBSB_1 for I2C devices are converted by the AQS Controller to I2C commands.

Example: To set the ‚Mini ROUTER' located within the BLA2BB, the incoming SBSB command from the acquisition control software is transformed into I2C compatible commands and then sets up the minirouter inside the BLA2BB.

To exceed the limitation of max. 8 I2C devices a second I2C bus is located on the AQS/2 User Bus backplane to allow the control a total of 16 I2C slaves.

High Speed Link *2.3.4*

The high speed link (LVDS[1]) from FCU4 to SGU transfers all NMR relevant real time events originating from the pulse program in 50ns time intervals to corre-

1 LVDS: Low voltage differential signaling

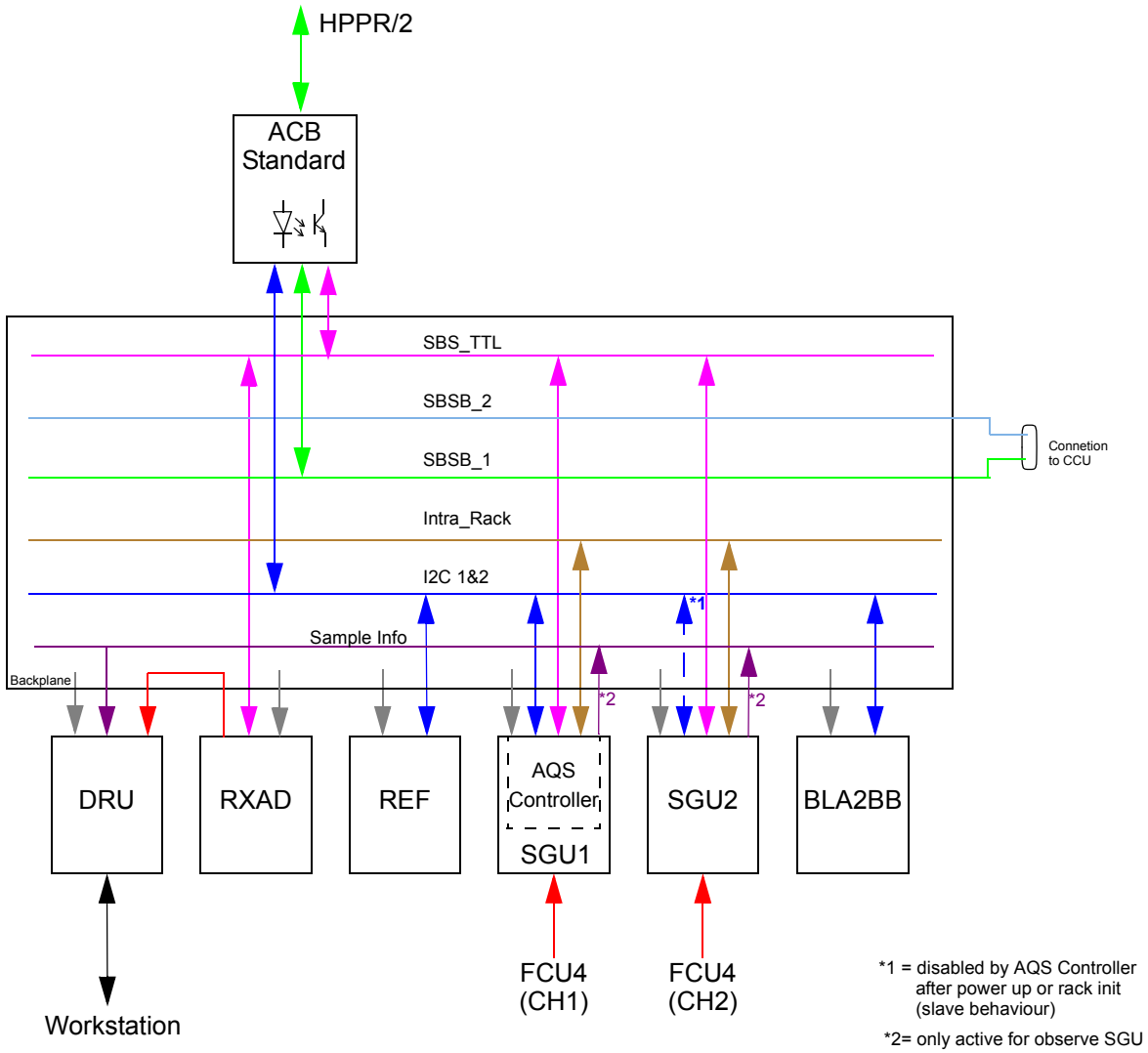
sponding SGU (e.g. pulses, shapes, phase jumps, frequency jumps, etc.). Each RF channel is connected by a separate high speed link to the FCU4. To allow a flexible extension of NMR channels, the wiring is located on the front side of the corresponding boards. To allow highest speed, a point to point connection architecture has been chosen.

Similarly the A/D converter output of a RXAD is coupled to the DRU via an own and well proven LVDS high speed link. With that it is possible to transfer a complex digital data point (real and imaginary) within 50ns and so allowing DWELL clocks up to 20MHz. Because each receiver channel consists of one RXAD and one DRU this link is physically located on the AQS/2 user bus, allowing to minimize cable connections on front side.

Sample Info *2.3.5*

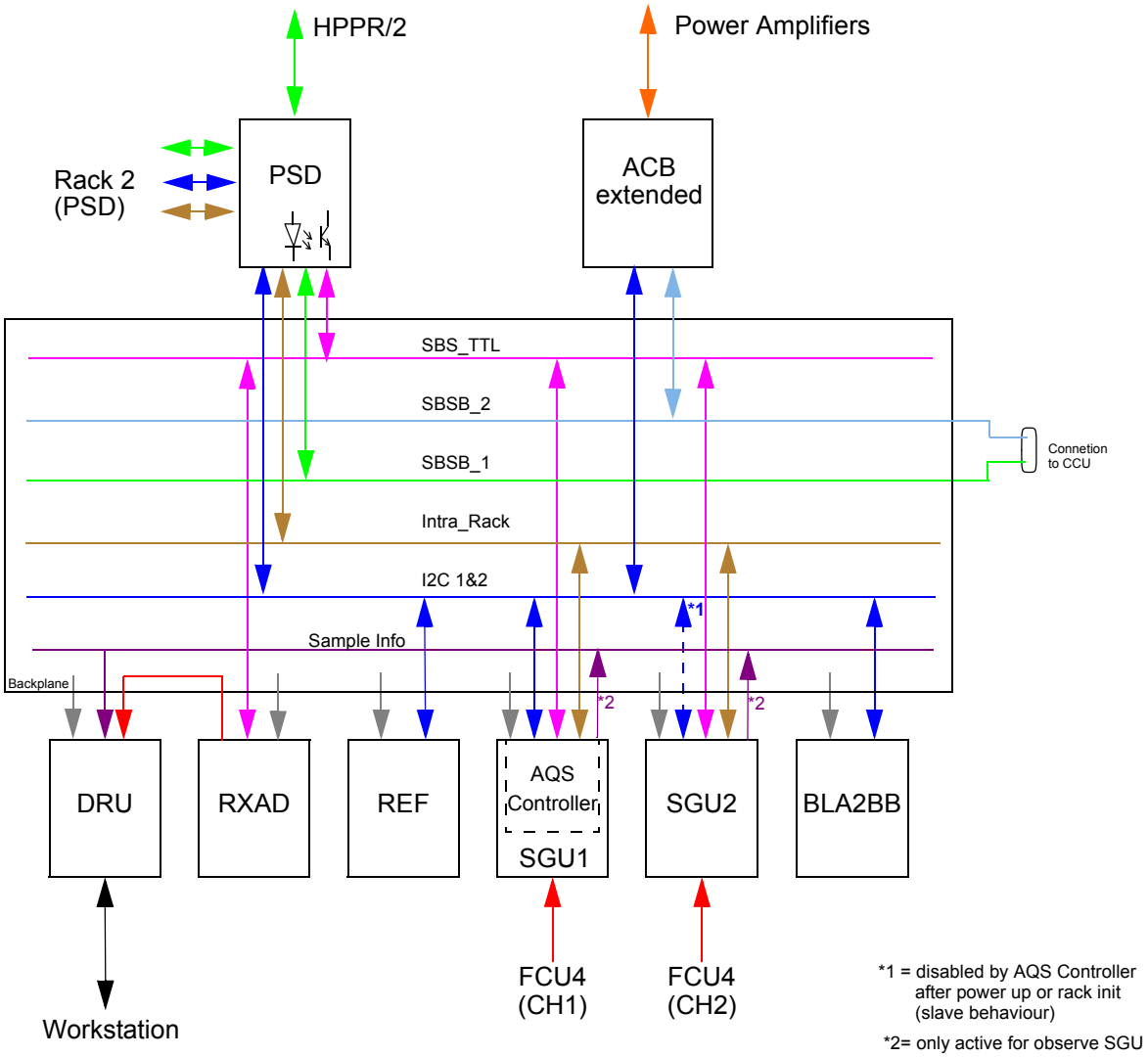
As already foreseen in the AQS Chassis backplane an acquisition synchronous scan information mechanism has been installed to control the receiver signal and process chain even over distributed hardware architectures. It is now possible to handle the receiver phase within the DRU, the data storage within the workstation onto disk, the display mode operation of the acquisition within the workstation and other not yet defined functions. Because it is under pulse program control, a full synchronicity with the acquired scan or in case of single data point acquisitions singular sample information can be maintained and finally the data can be easily traced within the disk file by storing the complete set of the ‚Sample Information'.

AQS Buses for a two channel system (internal BLA)



- High Speed Link (LVDS)
- RS485 (SBSB_1) from CCU
- RS485 (SBSB_2) from CCU
- SBS_TTL (galvanic isolated SBSB_1)
- Intra Rack Bus
- I^2C (1&2)
- Slot and Rack Adresses
- Ethernet
- Sample Info

Figure 2.2. AQS Buses for a two channel system (external BLA)



High Speed Link (LVDS)

RS485 (SBSB_1) from CCU

RS485 (SBSB_2) from CCU

SBS_TTL (galvanic isolated SBSB_1)

Intra Rack Bus

I^2C (1&2)

Slot and Rack Adresses

Ethernet

Sample Info

SBSB_2 (only used for ACB extented to control external power amplifiers)

Synchronous signals 2.4

Realtime control-pulses (RCP) on the AQS/2 User Bus 2.4.1

BLKTRx~ (Blanking pulses for power amplifiers)

Each BLKTR must be routed to the corresponding power amplifier. A SGU can control up to 8 power amplifiers with the corresponding BLKTR. The SGU must be initialized via SBSB_1 before starting the experiment. Each SGU will apply under high speed link control the required BLKTR pulse in real time onto the AQS/2 User Bus backplane. The BLKTR has wired nor logic on the backplane so that BLKTRs from different SGU can be combined to one amplifier (easy pulseprogramming, channel concept).

No additional cables are necessary to control the internal power amplifiers (e.g. BLA2BB). The BLKTR are routed directly on the backplane from the SGU to the corresponding BLA channel. BLKTR for external power amplifiers may be accessed on the front of the power supply and distribution board (PSD).

RGP_PA~ (Preamplifier receiver gating pulse)

This pulse (also mentioned as RGP_HPPR) is controlled by the SGU which is initialized as observing SGU. This signal is routed via the ACB-S standard (or PSD) to the observe module in the preamplifier HPPR or HPPR/2. All other non lock HPPR modules are in transmit or decoupling mode.

Note: In contrast to previous AVANCE systems, the preamplifier RGP will not be connected to the AQR RX22 but to RXAD for multi receiver configurations only.

RGP_LO~ (Local oscillator gating pulse)

This internal pulse enables the local oscillator generation inside the RXAD. The pulse is automatically generated by the observe SGU after switching to receive mode.

RGP_RX~ (Receiver gating pulse)

This pulse controls the gating inside the receiver e.g. the RXAD. The pulse is driven by the observe SGU and can be delayed with the spectrometer pulse program software. The signal is directly routed from the observe SGU via AQS/2 User Bus backplane to the receiver RXAD. With this signal the receiver may be ‚opened' later in respect to the preamplifier to prevent saturation.

Dwell_Clk~ (ADC dwell clock)

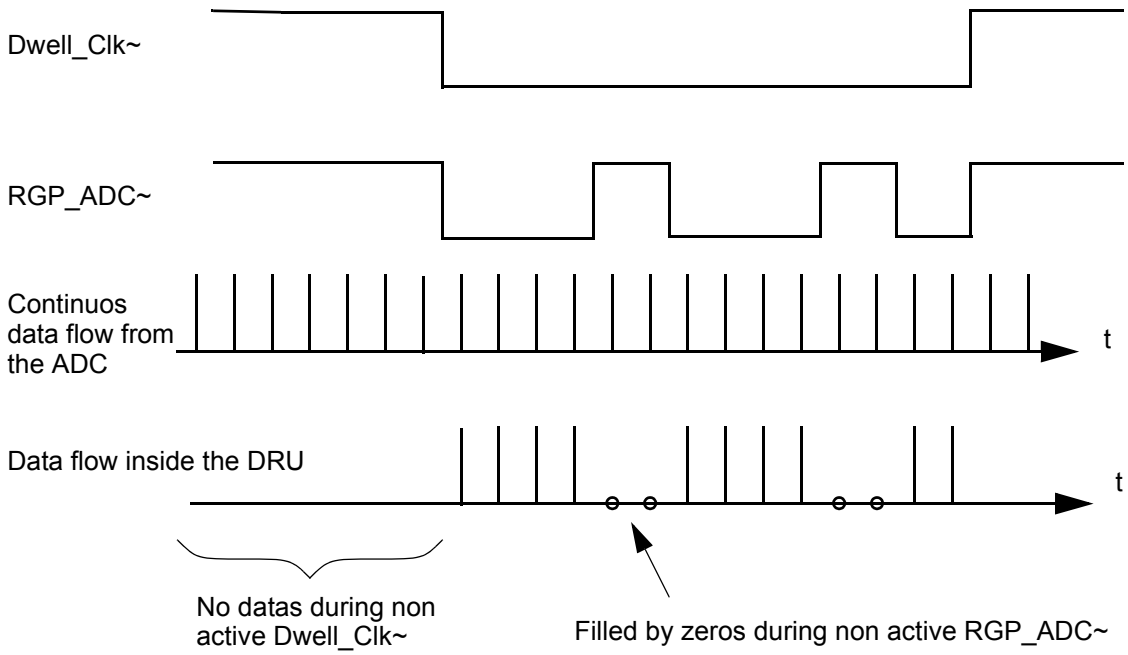
In fact the Dwell_Clk~ has changed operational behaviour in respect to previous AVANCE systems. It serves now as a dwell enable in the new system and with that doesn‘t reflect the physical AD converter rate anymore. The AD converter rate is now fixed to an oversampling frequency of 20MHz, is running continuously and the data stream is being enabled (gated) by the Dwell_Clk~ inside the DRU. The signal is also driven by the observe SGU.

RGP_ADC~ (ADC gating pulse)

This pulse (also driven by the observe SGU) controls the ADC data stream. For a non active RGP_ADC~ the data stream is filled with zeros inside the DRU, during the active pulse, ADC data is passed unchanged.

This signal is specially used for experiments like digital homodecoupling with oversampling.

Figure 2.3. Explanation of Dwell_Clk~ and RGP_ADC~



Sample Info

The Sample Info channel consists of the five lines SAMPLE_INFO(4:0) originating at the corresponding SGU. The interface is synchronous to the 20 MHz system clock (20MHZ_CLK) and hence the word rate is 20MW/s

The scan control commands have a fixed length of 6 words. Bit 4 of the first word carries the start bit which is always 1. Bit 4 of the last word must be set to 0. With that, all listeners to these lines are able to synchronize to the information contained within burst sent under pulse program control.

In between two Sample Info bursts, a recovery time of 10us must be granted.

The information is clustered to two groups, each with an individual enable bit:

The first group (enabled by bit „ScanCtrl“) carries information which must be available before a scan (e.g. scan phase, memory buffer, accumulation control). This information is associated to the upcoming scan.

The second group (enabled by bit „WriteCtrl“) carries information on how to proceed with a scan that has been readily accumulated (e.g. file seek, file change). This information is associated to the past scan.

Table 2.1. Data format of the 6 sample info words (5 Bits each)

word	Bit4 Pin E3	Bit3 Pin C2	Bit2 Pin D2	Bit1 Pin E2	Bit0 Pin E1
1	1 (Start)	ScanCtrl	PhaseRun	Phase (0,90,180,270)	
2	reserved=0	st0	st	zd	ze
3	OffsMeas	DruParamIndex			
4	WriteCtrl	FileNumber (0-15)			
5	reserved (set zero)		Write	Seek	
6	0 (Stop)	reserved (set zero)			

ScanCtrl

Enable bit for the first group. This bit must be set to prepare an upcoming scan.

PhaseRun

If this bit is set, the phase accumulator immediately starts running (synchronously to the Sample Info). If this bit is cleared, phase accumulation is delayed until Dwell_Clk~ becomes active for the first time.

Phase

Accumulation phase.

0 = 0 deg
1 = 90 deg
2 = 180 deg
3 = 270 deg

st0 , st

Controls the memory buffer handling.

st0,st	
0,0	accumulate the upcomming scan to the current buffer
0,1	accumulate the upcomming scan to the next buffer
1,0	accumulate the upcomming scan to the first buffer
1,1	reserved

zd, ze

Controls the accumulation.

zd,ze	
0,0	add the upcomming scan to the buffer
0,1	write the upcomming scan to the buffer
1,0	write the upcomming DummyScans+1 scans to the buffer
1,1	reserved

OffsMeas

This bit is partially independent of the groups „ScanCtrl“ and „WriteCtrl“ and triggers the DC offset calibration. The filed „DruParamIndex“ is co-used with „ScanCtrl“ but besides of this it is independent of the other two groups.

Dwell_Clk~ and RGP_ADC~ must be active for at least 1ms. During this time the DC offset is measured by averaging 16384 ADC samples.

DruParamIndex

These four bits select one out of 16 preloaded acquisition parameter sets. This is intended for interleaved acquisition, where all parameters have to change on the fly. (e.g. SWH, TD, DC offset)

WriteCtrl

Enable bit for the second group. This bit must be set to write a scan to disk.

FileNumber

These four bits select one of 16 disk files to write to or to manipulate the file pointer. Data source is always the memory buffer of the last acquisition.

„FileNumber“ can be chosen independently of the preloaded acquisition parameter sets (addressed by „DruParamIndex“) in the range 0-15.
(DataSetList, ifp, dfp, rfp):

0-12: directly access the files 0-12
13: use current file, then decrement file number
14: use current file, no change
15: use current file, then increment file number

Write (wr)

„Write“ = 1: Write TD*NBL samples to the file selected by „FileNumber“.

„Write“ = 0: disk file pointer manipulation only.

Seek (if,df,rf)

Manipulate the disk file pointer of the file „FileNumber“.

All 16 disk file pointers are cleared at experiment setup time.

0=none
1=increment disk file pointer by TD*NBL
2=decrement disk file pointer by TD*NBL
3=reset disk file pointer

SEL_ADCx~ (Select A/D converter)

Obsolete.

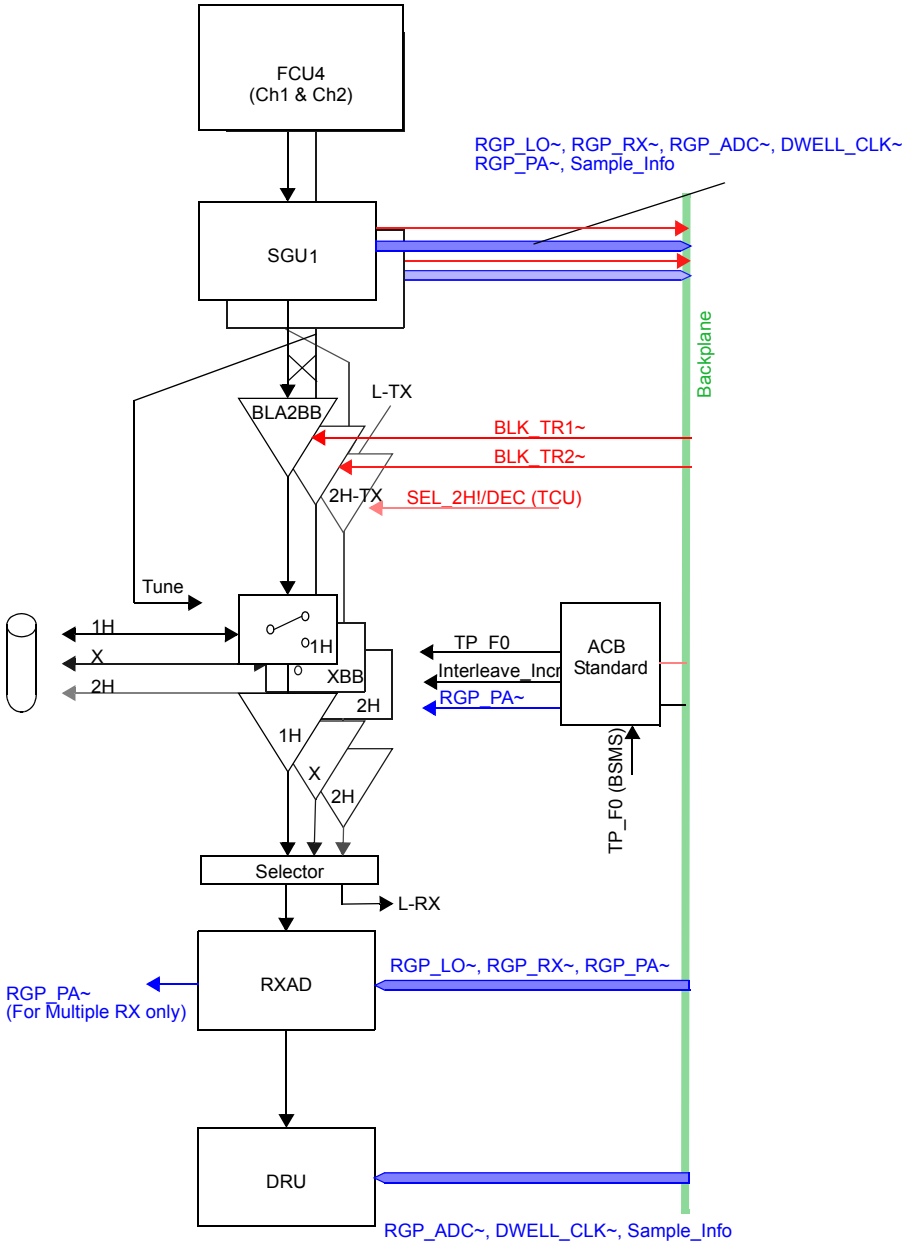
Interleave_Incr~

This pulse allows to switch between different preloaded modes under pulseprograme control. E.g. real time switching between 2H lock mode and 2H decoupling mode of the HPPR/2 can be controlled via this pulse or different receiving parameters can be selected during the experiment for interleaved acquisition.

ADC Overflow

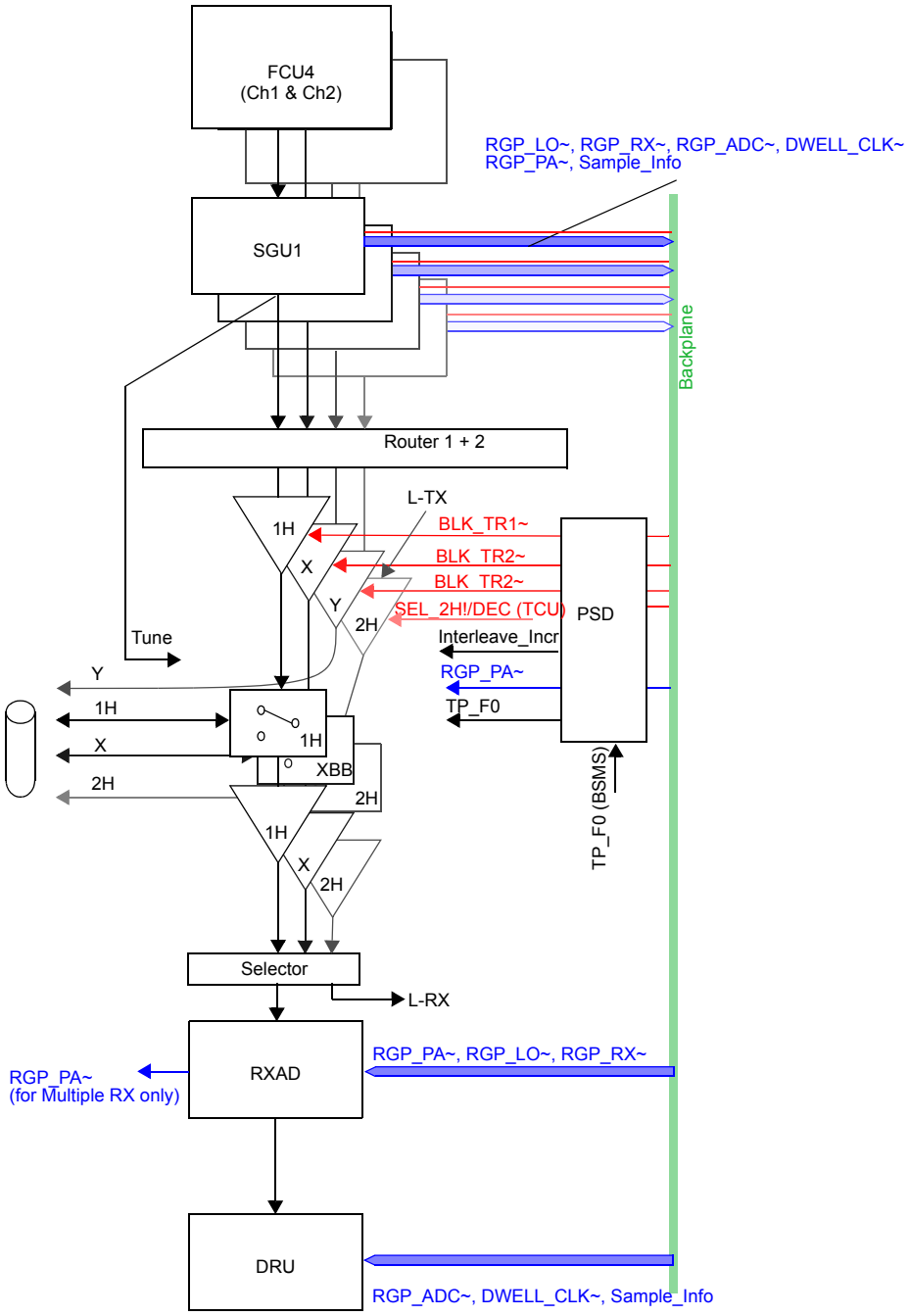
The ADC Overflow signal indicates an overdriven analogue to digital converter. Data are useless in such a situation, a corresponding error message will occur.

Figure 2.4. Pulse distribution on a two channel AVANCE (internal amplifiers)



In this configuration exist three amplifiers
but only two SGUs.
SGU2 can either be used for the BLA2BB or
the 2H-TX (for 2H decoupling or 2H shimming).
There is no blanking pulse required for the 2H-TX.
Controlling Lock mode or 2H-TX mode is done
via the signal SEL2H/!DEC) from the TCU3

Figure 2.5. Pulse distribution on a four channel AVANCE (external amplifiers)



Receiver pulse separation for multiple-receiver systems *2.5*

All receiver specific pulses must be separated between receivers in multiple receiver systems. These pulses are:

- RGP_PA~, RGP_LO~, RGP_RX~, RGP_ADC~
- DWELL_CLK~
- SEL_ADCx~
- SAMPLE_INFO(0:4), INTERLEAVE_INCR~

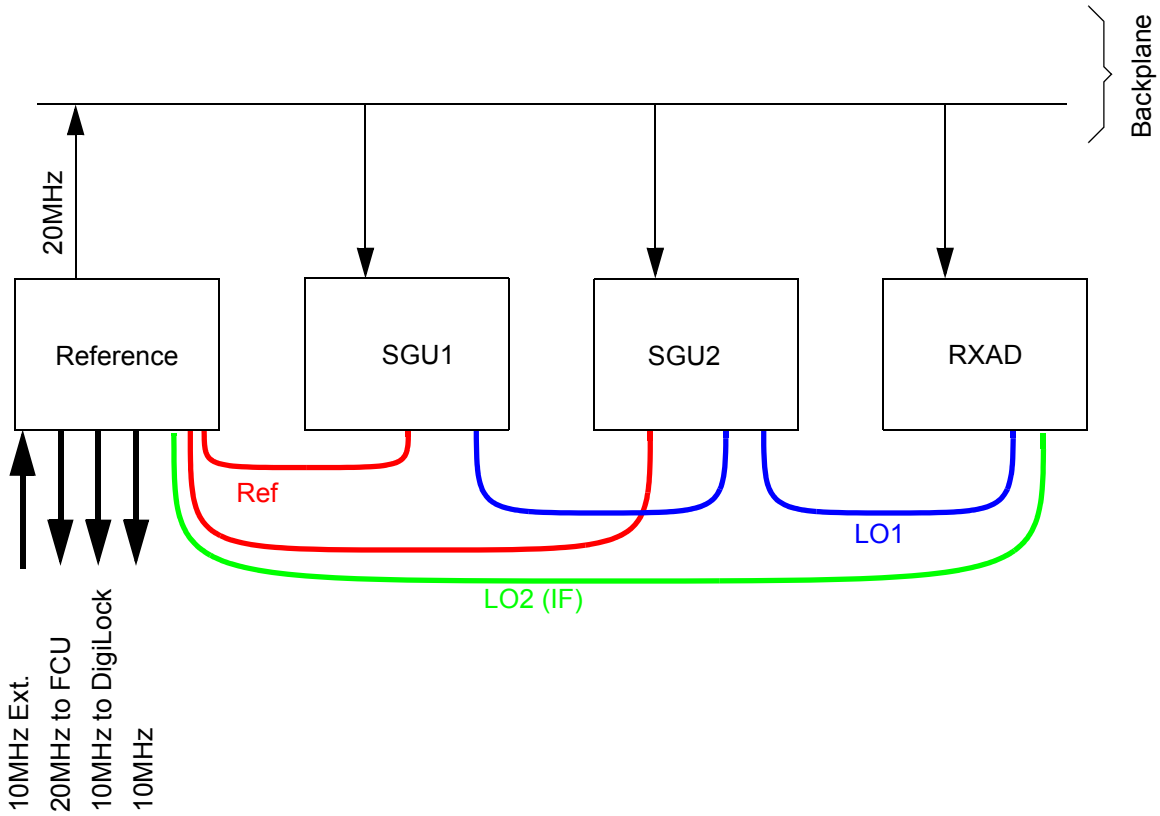
The separation is done with bus switch on the backplane. The bus switch are either controlled by jumper or via I2C. Details see ***"Pulse switch for receiver pulse separation" on page 73***

RF signal paths 2.6

The following RF signals are required in a AQS system:

1. The RF output of every SGU must be connected to a power amplifier or to a router/combiner.
2. Each SGU can be initialized as observe SGU and therefore each SGU must be able to drive the local oscillator signal for the receiver. Every SGU has a local oscillator input and a local oscillator output. The LO is looped through every SGU except the observe SGU, which is driving the local oscillator.
3. Several fixed frequencies are generated on the reference board (AQS REFERENCE). These signals are required for the upconversion electronics located in the SGU. One reference board can drive up to four SGUs.
4. The 10MHz output of the reference board is used to synchronize various units like the BSMS Lock. The reference board switches automatically to the external 10MHz input if a signal is applied.
5. The detection reference signal (LO 2) is directly wired from the reference board to the receiver.

Figure 2.6. RF distribution



20MHz Clock Distribution 2.7

Introduction 2.7.1

This section describes the clock distribution for all AQS units. It's very important for a synchronous system to have a clock distribution with smallest skew between the different units.

Between the clock source and the various boards the same number of drivers and the same length of cable must be used.

The FCU4 clock signal is looped through all FCUs and is finally terminated on the TCU3.

Blockdiagram 2.7.2

Figure 2.7. Clockdistribution for a single rack version

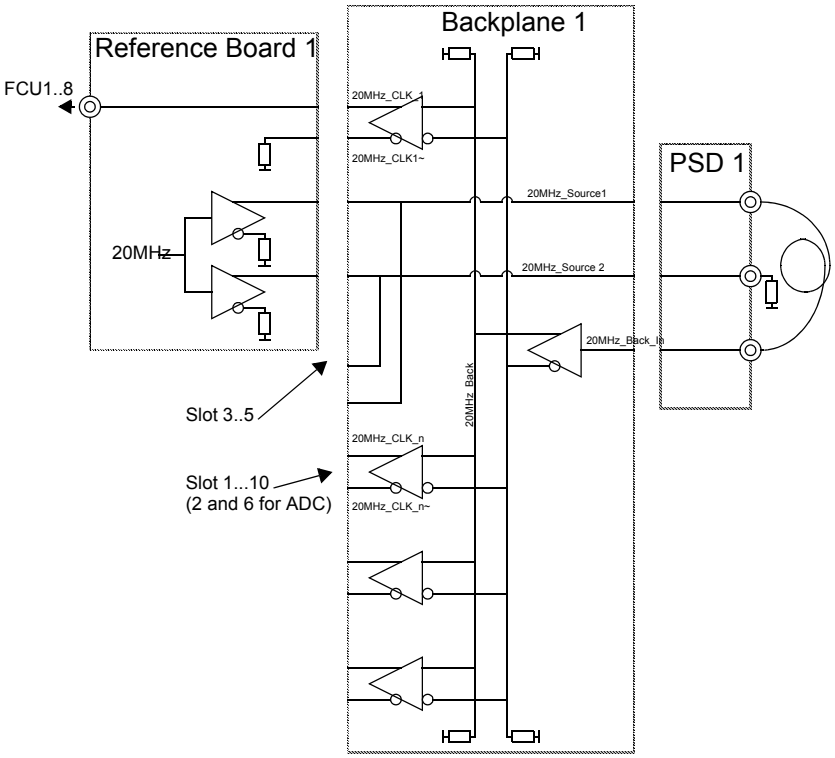
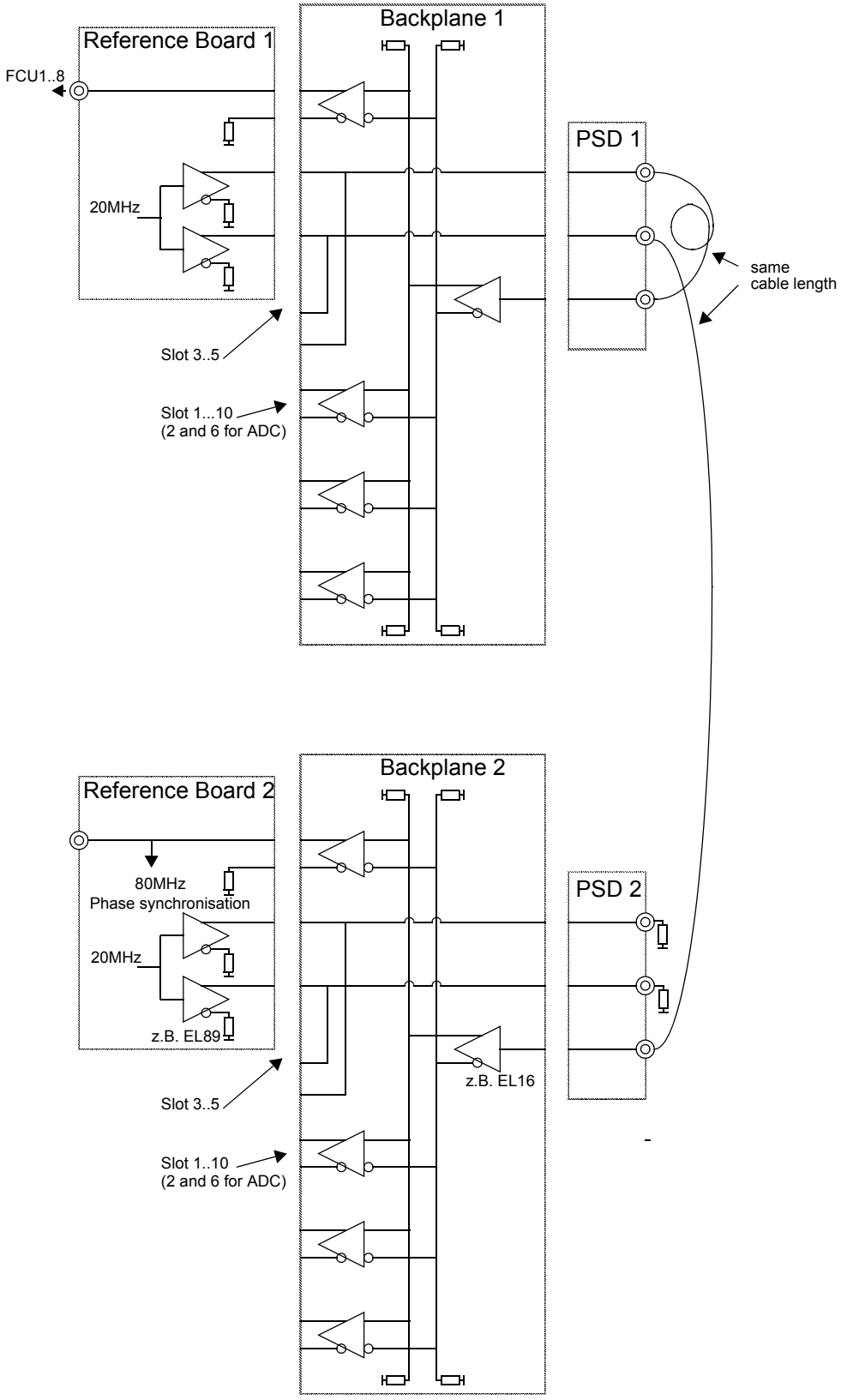


Figure 2.8. Clockdistribution for a dual rack version



AQS/2 Configurations 3

A typical 2 to 3 Channel AQS/2 HR (200-400MHz, internal BLA2BB & BLAX300) 3.1

Bill of Material 3.1.1

Table 3.1. Bill of material

Pos.	Units	Part Number	Description *Units for 3rd channel extension written in italics.*	MP[a]
1	1	Z101618	AQS/2 CHASSIS WIRED	
2	1	H9489	AQS POWER SUPPLY DIGITAL 350W	
3	1	Z12170 *W1345050*	BSMS FRONTPLATE BLIND 12TE *AQS POWER SUPPLY BLA 28V 20A*	MB
4	1	W1345050	AQS POWER SUPPLY BLA 28V 20A	
5	1	Z003403	AQS PSM2 POWER SUPPLY MODULE	
6	1	Z003402	AQS PSM1 POWER SUPPLY MODULE	
7	1	H9488	AQS ACB STANDARD BOARD	
8	1	H9503	AQS CCU11 COM CONTR UNIT	
9	1	H5813	AQS TCU3 TIMING CONTR BOARD	
10	1	H9773	AQS FCU4/2 CONTROLLER BOARD	
11	3	Z2778	BSMS FRONTPLATE BLIND 4TE	MB
12	1	Z100977	AQS DRU	
13	1	Z102116	AQS RECEIVER BOARD RXAD 400	
14	1	Z003265	AQS REFERENCE BOARD 400	
15	2	Z003642	AQS SGU 400	
16	1	Z15201 *see pos. 15*	AQS FRONTPLATE 1MM 16TE *AQS SGU*	MB
17	1	Z15202 *W1345052*	AQS COVERPLATE 16TE *AQS BLAX300 6-243MHZ*	MB
18	1	W1345049	AQS BLA2BB150/60 20-400	

Table 3.1. Bill of material

Pos.	Units	Part Number	Description *Units for 3rd channel extension written in italics.*	MP[a]
19	1	Z14133	AQS FRONTPLATE BLIND 2TE	MB
- [b]	12	25958	SCREW RRCH KR M2,5 x 12,3	MB

a MEC Part: MB = Part contained in AQS/2 MEC-PARTS MB (Z102136)

b use for pos. 3, 11 and 16

Jumper Setting *3.1.2*

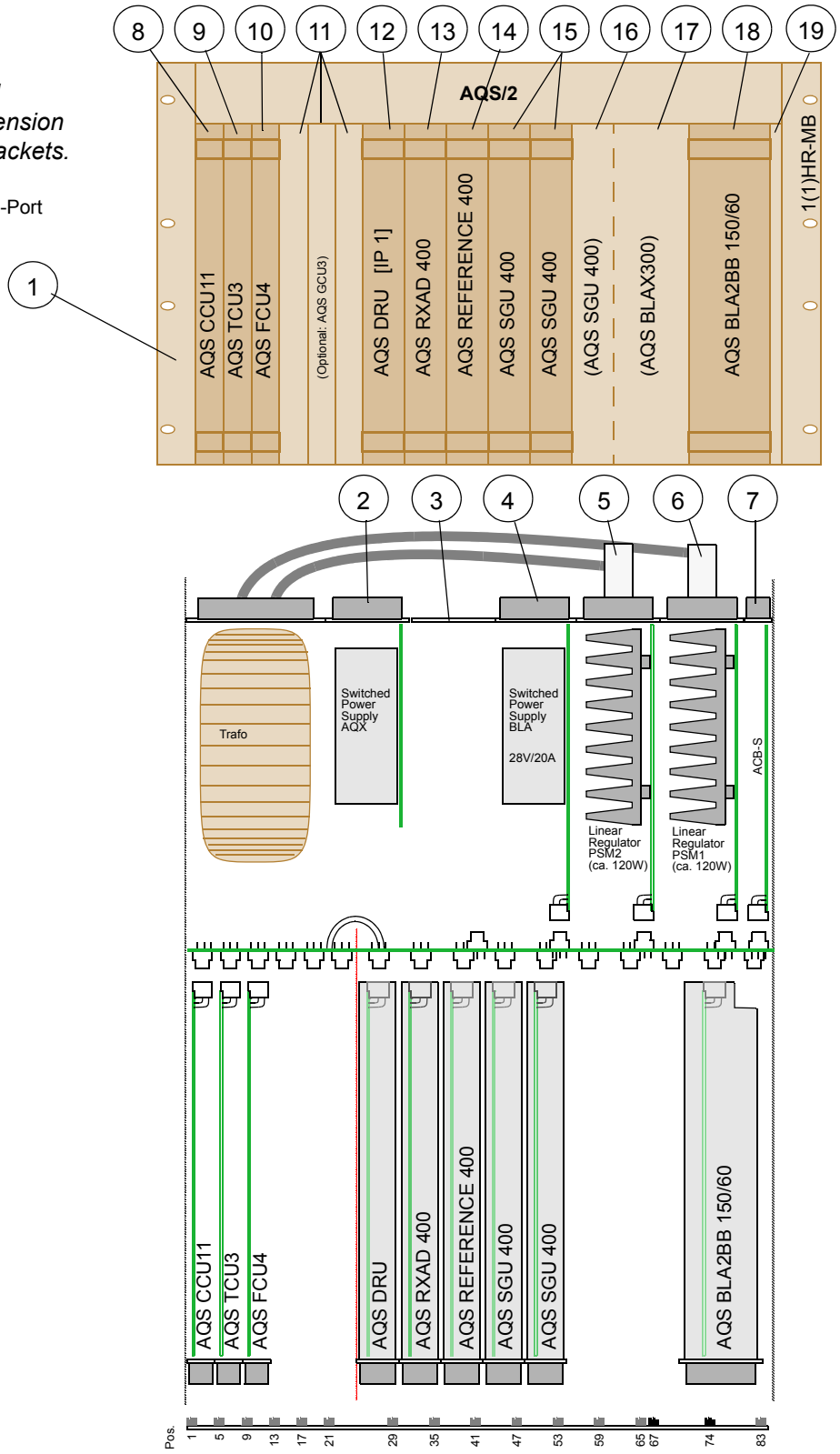
The rack address must be set to ‘0x39’ (JU1A and JU1D to JU1F on the AQS/2 user bus rear side must be closed).

See ***"Rackadress Settings" on page 74***

Figure 3.1. AQS/2 for 2 Channel AVANCE

Units for 3rd channel extension written in brackets.

[IP x] = DRU IP-Port



A typical 3 Channel AQS/2 HR (500-600MHz, internal BLAXH & 2H-TX) 3.2

Bill of Material *3.2.1*

Table 3.2. Bill of material

Pos.	Units	Part Number	Description	MP[a]
1	1	Z101618	AQS/2 CHASSIS WIRED	
2	1	H9489	AQS POWER SUPPLY DIGITAL 350W	
3	2	W1345050	AQS POWER SUPPLY BLA 28V 40A	
4	1	Z003403	AQS PSM2 POWER SUPPLY MODULE	
5	1	Z003402	AQS PSM1 POWER SUPPLY MODULE	
6	1	H9488	AQS ACB STANDARD BOARD	
7	1	H9503	AQS CCU11 COM CONTR UNIT	
8	1	H5813	AQS TCU3 TIMING CONTR BOARD	
9	1	H9727	AQS FCU4/4 CONTROLLER BOARD	
10	3	Z2778	BSMS FRONTPLATE BLIND 4TE	OB
11	1	Z100977	AQS DRU	
12	1	Z102117	AQS RECEIVER BOARD RXAD 600	
13	1	Z003936	AQS REFERENCE BOARD 600	
14	3	Z003831	AQS SGU 600	
15	1	Z103551	AQS 2H-TX BD 500-1000	
16	1	W1345056	AQS BLAXH 300/50 500-600MHZ	
- [b]	14	25958	SCREW RRCH KR M2,5 x 12,3	OB

a MEC Part: OB = Part contained in AQS/2 MEC-PARTS MB (Z102137)

b use for pos. 10

Jumper Setting *3.2.2*

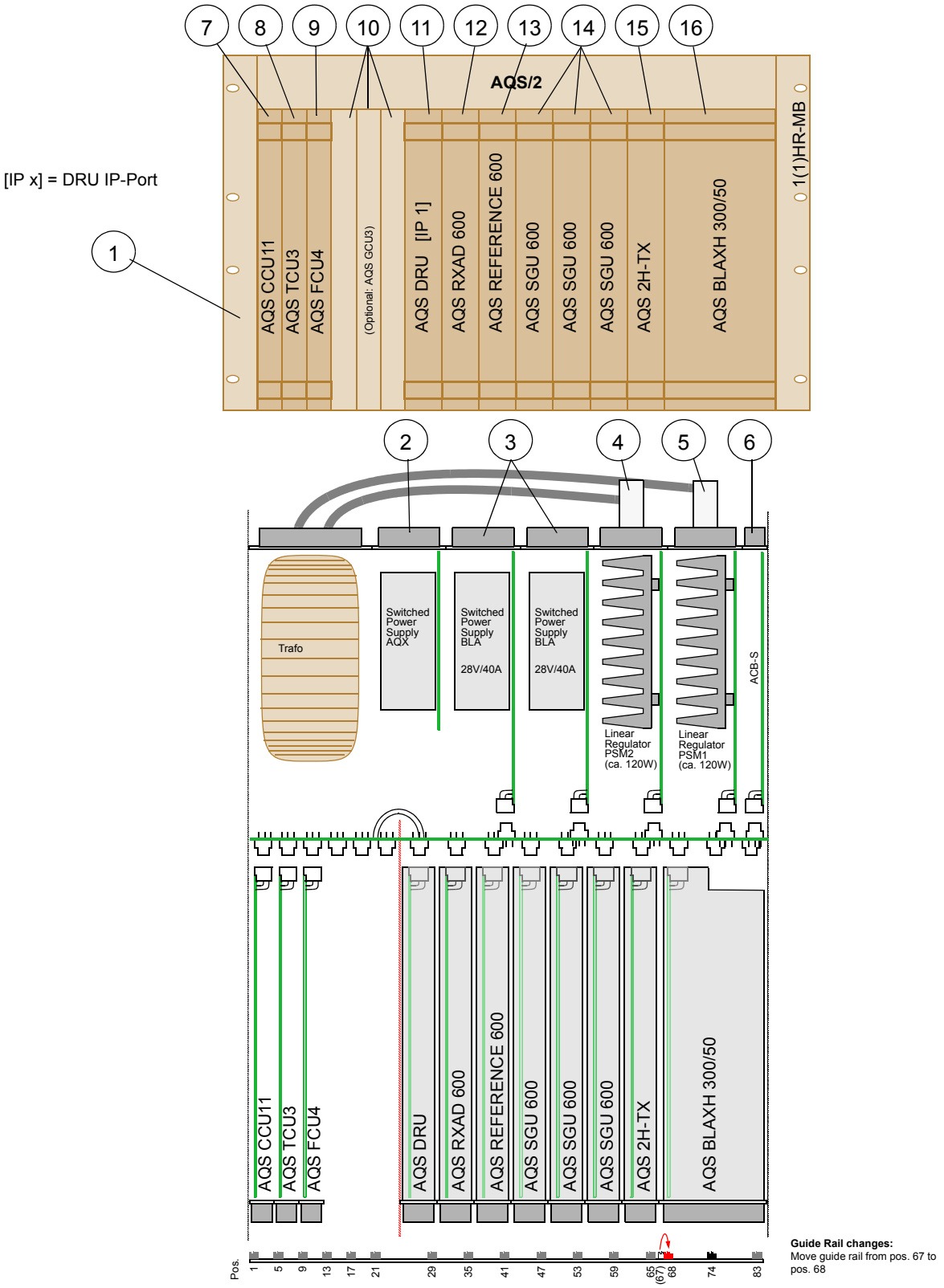
The rack address must be set to ‘0x39’ (JU1A and JU1D to JU1F on the AQS/2 user bus rear side must be closed).

See ***"Rackadress Settings" on page 74***

Guide Rail changes *3.2.3*

Move guide rail from pos. 67 to pos. 68

Figure 3.2. AQS/2 for 2 Channel AVANCE



A typical 2 Channel AQS/2 HR with internal PREAMP and BLA2BB (300 and 400MHz) *3.3*

Bill of Material *3.3.1*

Table 3.3. Bill of material

Pos.	Units	Part Number	Description	MP[a]
1	1	Z101618	AQS/2 CHASSIS WIRED	
2	1	H9489	AQS POWER SUPPLY DIGITAL 350W	
3	1	Z12170	BSMS FRONTPLATE BLIND 12TE	MB
4	1	W1345050	AQS POWER SUPPLY BLA 28V 20A	
5	1	Z003403	AQS PSM2 POWER SUPPLY MODULE	
6	1	Z003402	AQS PSM1 POWER SUPPLY MODULE	
7	1	H9488	AQS ACB STANDARD BOARD	
8	1	H9503	AQS CCU11 COM CONTR UNIT	
9	1	H5813	AQS TCU3 TIMING CONTR BOARD	
10	1	H9773	AQS FCU4/2 CONTROLLER BOARD	
11	4 *(1)*	Z2778 *Z003961*	BSMS FRONTPLATE BLIND 4TE *AQS PREAMP CONTROL BD* [b]	MB
12	1	Z100977	AQS DRU	
13	1	Z102116	AQS RECEIVER BOARD RXAD 400	
14	1	Z003265	AQS REFERENCE BOARD 400	
15	2	Z003642	AQS SGU 400	
16	1	Z003950 Z003951	AQS 1H2H PREAMP 300 AQS 1H2H PREAMP 400	
17	1	Z003954 Z003955	AQS XBB19F 2HS PREAMP 300 AQS XBB19F 2HS PREAMP 400	
18	1	W1345049	AQS BLA2BB150/60 20-400	
19	1	Z14133	AQS FRONTPLATE BLIND 2TE	MB
-	12	25958	SCREW RRCH KR M2,5 x 12,3	MB

a MEC Part: MB = Part contained in AQS/2 MEC-PARTS MB (Z102136)

b Only necessary if DRU is **not** HPPR/2 controller

Jumper Setting *3.3.2*

The rack address must be set to ‘0x39’ (JU1A and JU1D to JU1F on the AQS/2 user bus rear side must be closed).

See ***"Rackadress Settings" on page 74***

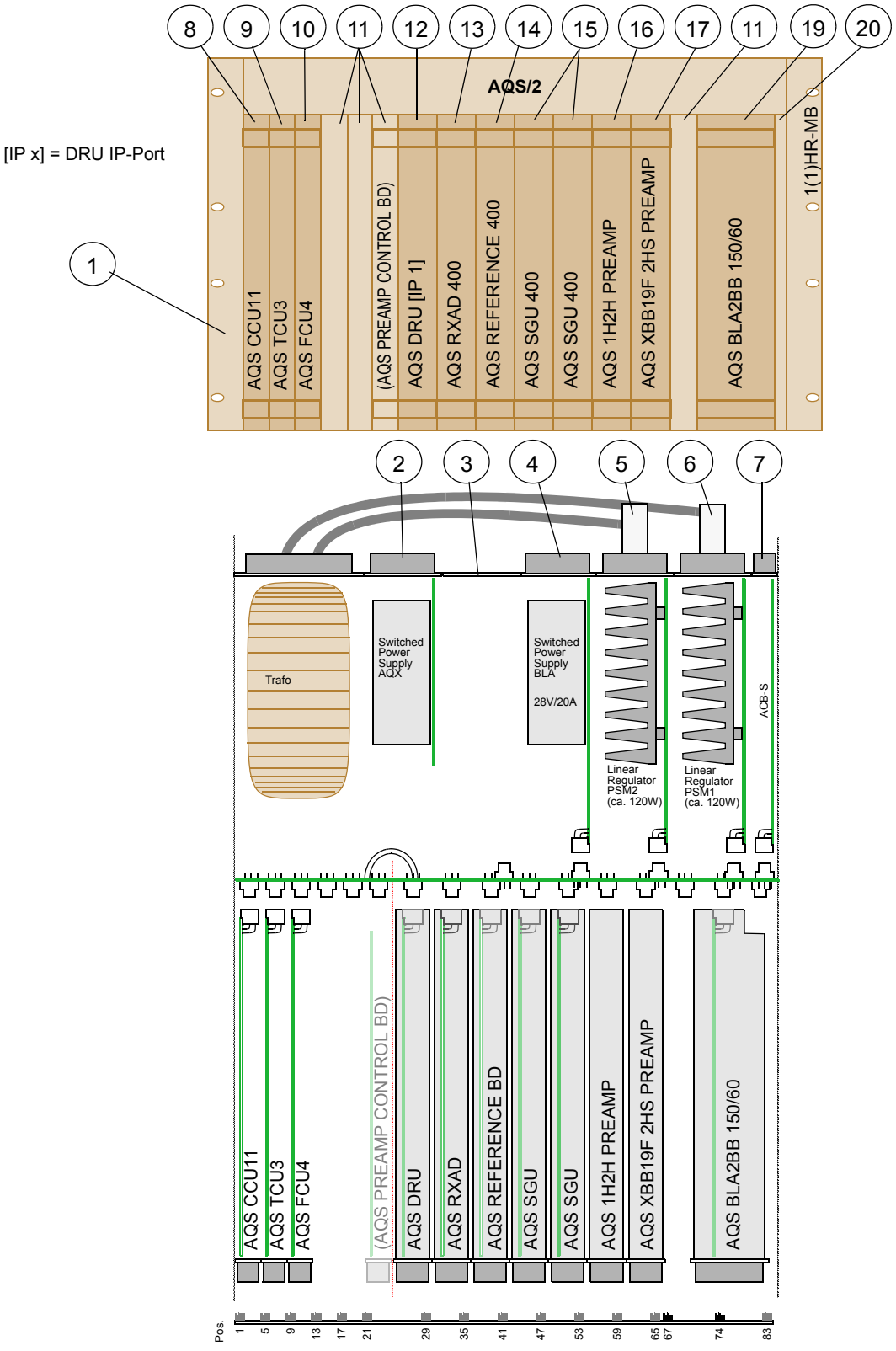
50 Ohm Terminators on AQS PREAMP’s *3.3.3*

The AQS PREAMP modules are delivered with ext. 50 Ohm terminators (SMB plug). They must be mounted as follows:

- AQS 1H2H Preamp: LOCK IN
- AQS XBB19F 2HS PREAMP: RF IN and TUNE OUT

Board location ***3.3.4***

Figure 3.3. AQS/2 for 2 Channel AVANCE with internal PREAMP and BLA



A typical 2 to 4 Channel AQS/2 HR & Solids (with external BLA) 3.4

Bill of Material 3.4.1

Table 3.4. Bill of material

Pos.	Units	Part Number	Description *Units for 3rd or 4th channel extension written in italics.*	MP[a]
1	1	Z101618	AQS/2 CHASSIS WIRED	
2	1	H9520	AQS POWER SUPPLY DIGITAL 450W	
3	1	H9500	AQS ACB EXTENDED BOARD	
4	1	Z12170	BSMS FRONTPLATE BLIND 12TE	OB
5	1	Z102023	AQS PSM5 POWER SUPPLY MODULE	
6	1	Z003402	AQS PSM1 POWER SUPPLY MODULE	
7	1	H9530	AQS PSD BOARD	
8	1	H9503	AQS CCU11 COM CONTR UNIT	
9	1	H5813	AQS TCU3 TIMING CONTR BOARD	
10	1	H9773 *H9727*	AQS FCU4/2 CONTROLLER BOARD *AQS FCU4/4 CONTROLLER BOARD*	
11	4	Z2778	BSMS FRONTPLATE BLIND 4TE	OB
12	1	Z100977 Z102520	AQS DRU (≤ 400MHz) AQS DRU-E (≥ 500MHz)	
13	1	Z102116 Z102117 Z102118 Z102119	AQS RECEIVER BOARD RXAD 400 AQS RECEIVER BOARD RXAD 600 AQS RECEIVER BOARD RXAD 1000 AQS RECEIVER BOARD RXAD-BB	
14	1	Z003265 Z003936 Z003937	AQS REFERENCE BOARD 400 AQS REFERENCE BOARD 600 AQS REFERENCE BOARD 1000	
15	2	Z003642 Z003831 Z003830	AQS SGU 400 AQS SGU 600 AQS SGU 1000	
16	1	Z14119 *see Pos.15* *Z12489*	AQS FRONTPLATE BLIND 1MM 12TE *AQS SGU* *AQS FRONTPLATE BLIND 6TE*	OB OB
17 [b]	1	Z14120 *see Pos.15*	AQS COVERPLATE 8TE *AQS SGU*	OB
18	1	Z003624	AQS 3-CHANNEL ROUTER BOARD	

Table 3.4. Bill of material

Pos.	Units	Part Number	Description *Units for 3rd or 4th channel extension written in italics.*	MP[a]
19	1	Z12490 *Z003624*	AQR FRONTPLATE BLIND 7TE *AQS 3-CHANNEL ROUTER BOARD*	OB
20	1	Z003349	AQS ADAPTER ROUTER DUAL	
- [c]	14	25958	SCREW RRCH KR M2,5 x 12,3	OB

a MEC Part: OB = Part contained in AQS/2 MEC-PARTS ONE-BAY (Z102137)
b used only with pos. 16 as frontplate
c used for pos. 4, 11, 16, and 19

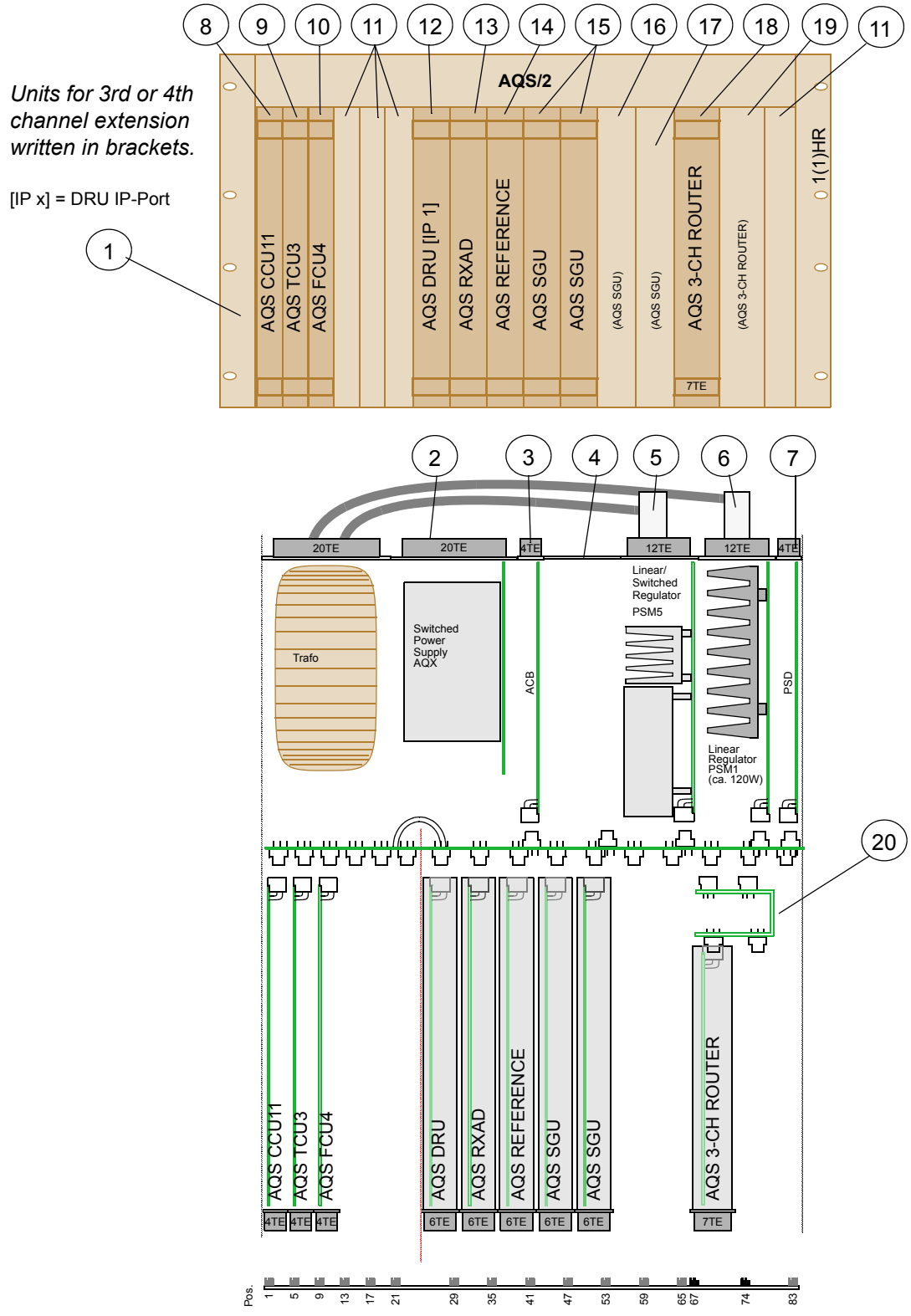
Jumper Setting *3.4.2*

The rack address must be set to ‘0x39’ (JU1A and JU1D to JU1F on the AQS/2 user bus rear side must be closed).

See ***"Rackadress Settings" on page 74***

Board location ***3.4.3***

Figure 3.4. AQS/2 for 2 to 4 Channel AVANCE (with ext. BLA)



A typical 5 to 8 Channel AQS/2 HR & Solids (2 Chassis, 3-CH Router) 3.5

Bill of Material *3.5.1*

Table 3.5. Bill of material: Rack 1

Pos.	Units	Part Number	Description *Units for 6th channel extension written in italics.*	MP[a]
1	1	Z101618	AQS/2 CHASSIS WIRED	
2	1	H9520	AQS POWER SUPPLY DIGITAL 450W	
3	1	H9500	AQS ACB EXTENDED BOARD	
4	1	Z12170	BSMS FRONTPLATE BLIND 12TE	MB
5	1	Z102023	AQS PSM5 POWER SUPPLY MODULE	
6	1	Z003402	AQS PSM1 POWER SUPPLY MODULE	
7	1	H9530	AQS PSD BOARD	
8	1	H9503	AQS CCU11 COM CONTR UNIT	
9	1	H5813	AQS TCU3 TIMING CONTR BOARD	
10	1	H9727	AQS FCU4/4 CONTROLLER BOARD	
11	1	H9773	AQS FCU4/2 CONTROLLER BOARD	
12	2 *1*	Z2778 *H5817*	BSMS FRONTPLATE BLIND 4TE *AQS GCU3 GRAD CONTR UNIT*	MB
13	1	Z100977 Z102520	AQS DRU (≤ 400MHz) AQS DRU-E (≥ 500MHz)	
14	1	Z102116 Z102117 Z102118 Z102119	AQS RECEIVER BOARD RXAD 400 AQS RECEIVER BOARD RXAD 600 AQS RECEIVER BOARD RXAD 1000 AQS RECEIVER BOARD RXAD-BB	
15	1	Z104236	AQS REFERENCE BOARD/2 1000	
16	5	Z003642 Z003831 Z003830	AQS SGU 400 AQS SGU 600 AQS SGU 1000	
17	2 *1*	Z12489 *see Pos. 16*	AQR FRONTPLATE BLIND 6TE *AQS SGU*	2nd
18	1 *(2)*	Z102000	AQS BB SPLITTER 2-WAY	
19	1	45999	ATTENUATOR SMA-SMA 6DB	
- [b]	12	25958	SCREW RRCH KR M2,5 x 12,3	MB

a MEC Part: OB = Part contained in AQS/2 MEC-PARTS MB (Z102136)

b used for pos. 4, 12 and 17

Table 3.6. Bill of material: Rack 2

Pos.	Units	Part Number	Description *Units for 8 channel extension written in italics.*	MP[a]
30	1	Z101618	AQS/2 CHASSIS WIRED	
31	1	H9489	AQS POWER SUPPLY DIGITAL 350W	
32	2	Z12170	BSMS FRONTPLATE BLIND 12TE	2nd
33	1	Z003403	AQS PSM2 POWER SUPPLY MODULE	
34	1	Z003402	AQS PSM1 POWER SUPPLY MODULE	
35	1	H9530	AQS PSD BOARD	
36	2	Z13955	AQS FRONTPLATE BLIND 1MM 18TE	2nd
37	2	Z13954	AQS COVERPLATE 18TE	2nd
38	1 *1*	Z13955 *Z003265* *Z003936* *Z003937*	AQS FRONTPLATE BLIND 1MM 18TE *AQS REFERENCE BOARD 400* *AQS REFERENCE BOARD 600* *AQS REFERENCE BOARD 1000*	2nd
39	1 *2*	Z13954 *Z003642* *Z003831* *Z003830*	AQS COVERPLATE 18TE *AQS SGU 400* *AQS SGU 600* *AQS SGU 1000*	2nd
40	1	Z14119	AQS FRONTPLATE 1MM 12TE	2nd
41	1	Z14120	AQS COVERPLATE 8TE	2nd
42	2	Z003624	AQS 3-CHANNEL ROUTER BOARD	
43	1	Z2778	BSMS FRONTPLATE BLIND 4TE	2nd
44	1	Z003349	AQS ADAPTER ROUTER DUAL	
45	1	Z15357	SCHILD PL GE “AQS RACK ON” Z4K-4466 (Marking Z4K-4466 on ***left*** side)	2nd
46	1	Z15358	SCHILD PL GE “AQS EXT RACK ON” Z4K-4467 (Marking Z4K-4467 on ***right*** side)	2nd
47	1	HZ13413	CABLE RD 68P1000 DRU INTRA RACK [b]	
- [c]	18	25958	SCREW RRCH KR M2,5 x 12,3	2nd

a MEC Part: 2nd = Part contained in AQS/2 MEC-PARTS 2ND-CHASSIS (Z102138)

b Cable supplied with cable kit

c used for pos. 32, 36, 38, 40 and 43

Jumper Setting *3.5.2*

Rack 1:

The rack address must be set to ‘0x39’ (JU1A and JU1D to JU1F on the AQS/2 user bus rear side must be closed).

See ***"Rackadress Settings" on page 74***

Rack 2:

The rack address must be set to ‘0x36’ (JU1B, JU1C, JU1E and JU1F on the AQS/2 user bus rear side must be closed).

Guide Rail changes *3.5.3*

Rack 1:

To change the guide rails correctly please follow the exact order as described below.

1. Move guide rail from pos. 83 to pos. 71
2. Move guide rail from pos. 67 to pos. 77
3. Move guide rail from pos. 74 to pos. 83

Rack 2:

No changes

The REFERENCE BOARD 400..1000 can only support 4 SGU with the necessary reference frequencies. For more than 4 SGU in one chassis a REFERENCE BOARD/2 1000 must be used.

The REFERENCE BOARD/2 has 2 standard and 2 boosted REF outputs.

- Standard Outputs: REF 1 (J6) and REF 2 (J7)
- Boosted Outputs: REF 3+4 (J8) and REF 5+6 (J9)

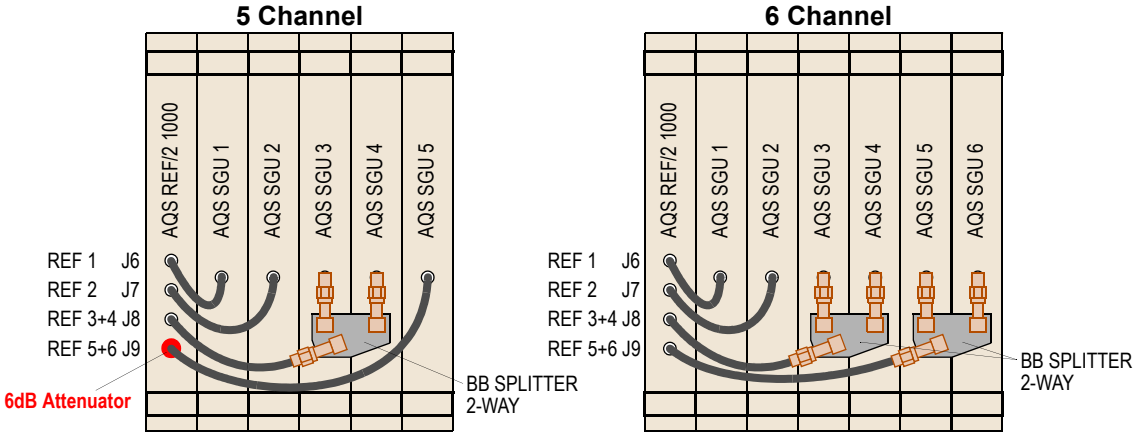
5 Channel Configuration:

The standard outputs REF1 and REF2 supply the first two SGU. SGU3 and SGU4 are connected to output REF3+4 with the AQS BB SPLITTER 2-WAY. SGU5 is connected to output REF5+6 with a 6dB attenuator.

6 Channel Configuration:

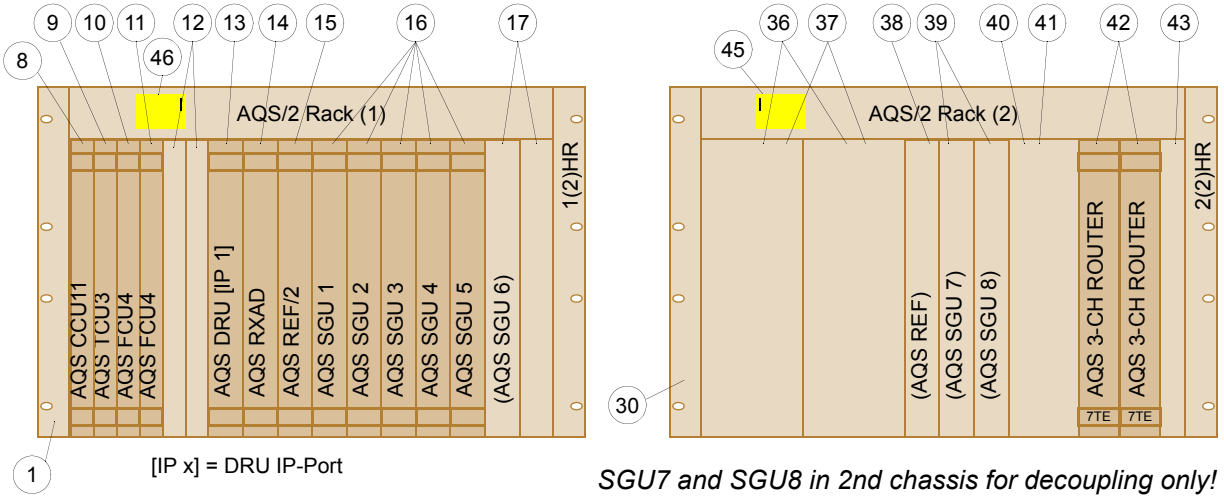
The standard outputs REF1 and REF2 supply the first two SGU. SGU3 and SGU4 are connected to output REF3+4 with the first AQS BB SPLITTER 2-WAY. SGU5 and SGU6 are connected to output REF5+6 with the second AQS BB SPLITTER 2-WAY.

Figure 3.5. REF/2 1000 & BB Splitter Connection

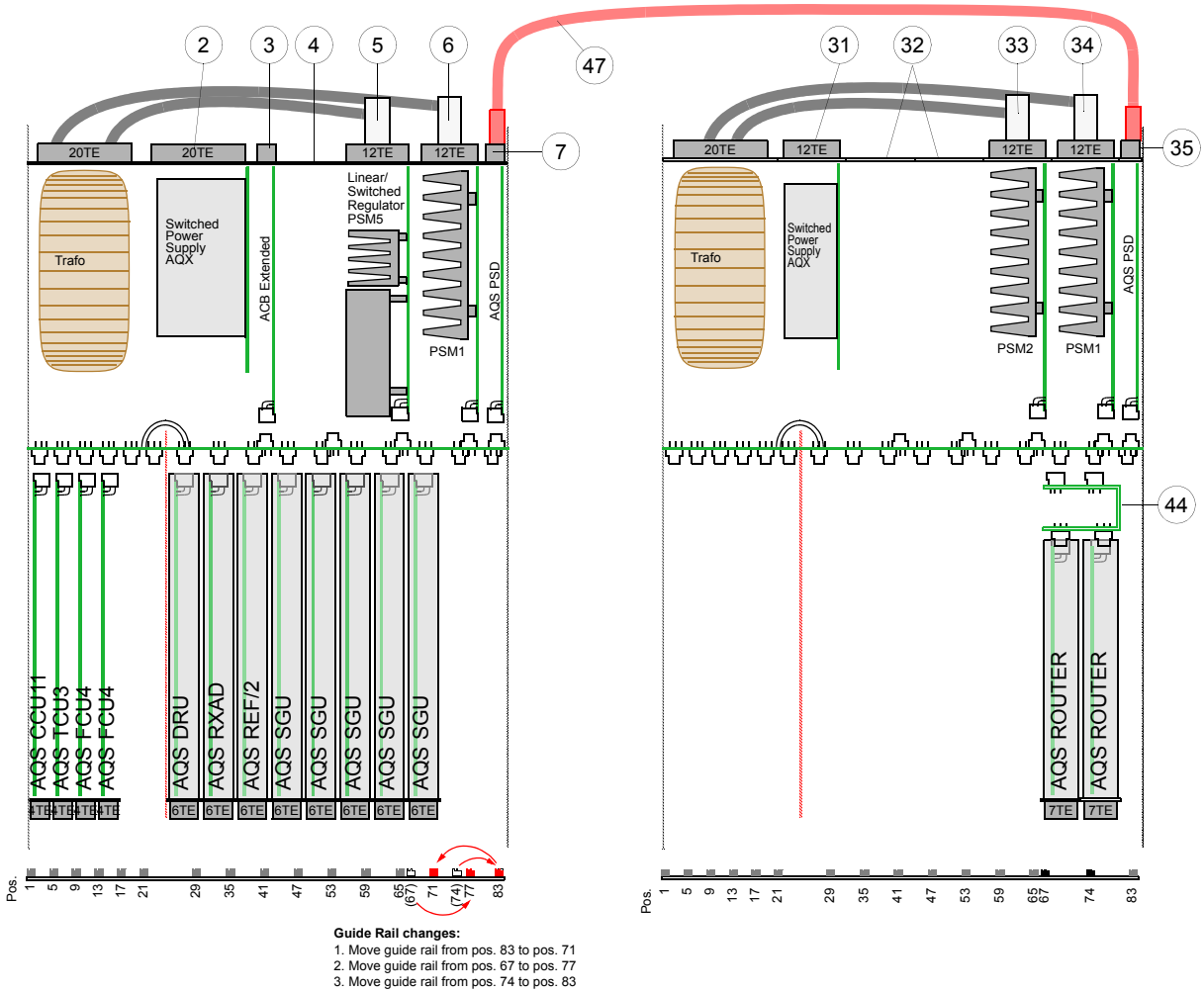


Board location 3.5.5

Figure 3.6. AQS/2 for 5 to 8 Channel AVANCE (2 Chassis, 3-CH Router)



SGU7 and SGU8 in 2nd chassis for decoupling only!
Units for 6 to 8 channel extension written in brackets.

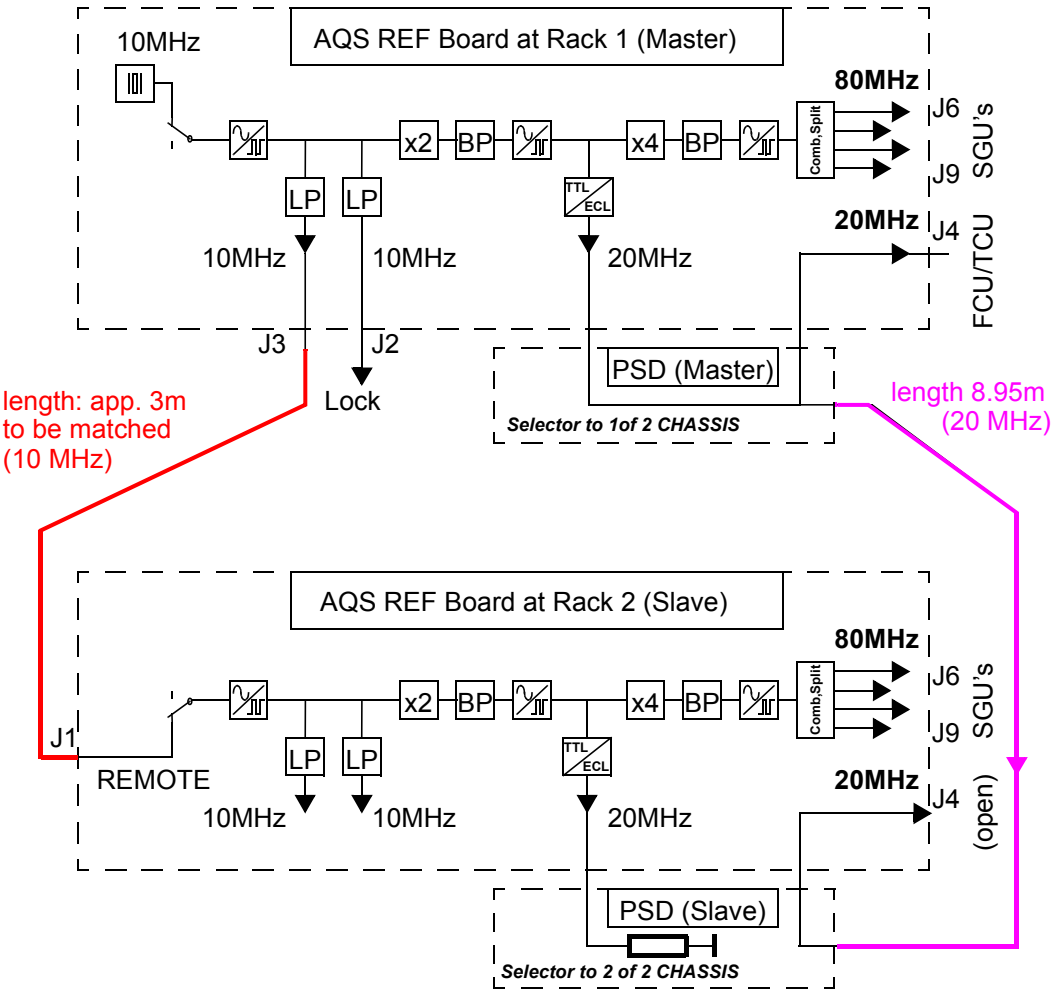


Guide Rail changes:
1. Move guide rail from pos. 83 to pos. 71
2. Move guide rail from pos. 67 to pos. 77
3. Move guide rail from pos. 74 to pos. 83

Adjusting the AQS Reference Board phase 20/80 MHz 3.5.6

The phases of the signals 20 MHz and 80 MHz, out of the two AQS Reference Board (Z104236 or Z003265) at rack 1 and rack 2, has to be the same. The time between the negative slope of the 80 MHz and the positive slope of the 20 MHz signal is a critical value.

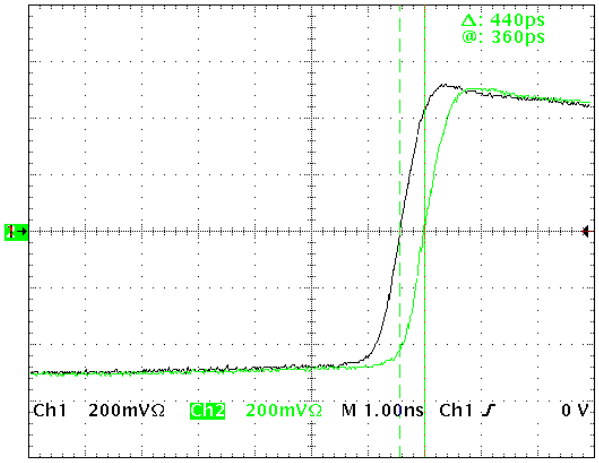
Figure 3.7. Connection between the two racks: overview



20 MHz Phase:

The length of the 20 MHz interconnection (HZ10146) does influence the phase of the 20 MHz signal at AQS Reference Board / J4 (rack 2). Using a length of 8.95 m will turn the phase to 0° (360°) and a measurement by scope will show the difference (+/- 1ns max.)

Figure 3.8. Phase difference of the 20 MHz



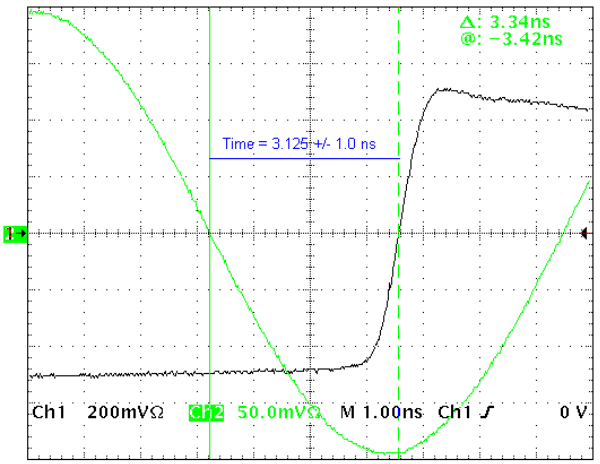
80 MHz phase:

To observe the 80 MHz signals at J6...9, a bandpass filter has to be inserted. The Mini-Circuits Model SLP-90 and SHP-25 filter, together with the coaxial cable HZ04057, will select the 80 MHz out of the multiple frequency signal and change the phase app. 0° (360°). That can be easy tested by using 80 MHz out of the SGU and observe the phase difference with and without the filter combination, when the monitor is external triggered by 20 MHz.

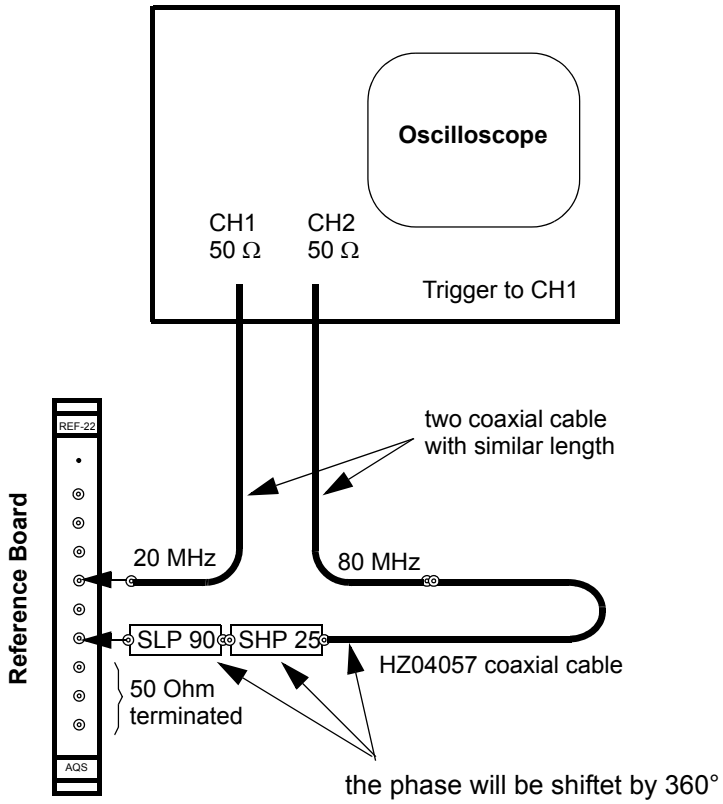
The length of the 10 MHz REMOTE interconnection does influence the phase of the 80 MHz signal on J6...9 of the rack 2. Use H10045 Cable Set 2nd REF for adjusting the optimum length. The cable set and the 80 MHz Filter is a part of the 5 to 6 Channel AVANCE Wiring.

! ***Time between negative slope of 80 MHz and positive slope of 20 MHz has to be 3.125 ns ± 1 ns. The adjustment must be done after every change of a AQS Reference Board.***

Figure 3.9. Phase 20/80 MHz



Measurement settings:



A typical 1 Channel AQS/2 PharmaScan with 1 RX 3.6

Bill of Material 3.6.7

Table 3.7. Bill of material

Pos.	Units	Part Number	Description	MP[a]
1	1	Z101618	AQS/2 CHASSIS WIRED ≥ ECL 01 [b]	
2	1	H9520	AQS POWER SUPPLY DIGITAL 450W	
3	1	H9500	AQS ACB EXTENDED BOARD	
4	1	Z12170	BSMS FRONTPLATE BLIND 12TE	MRX
5	1	Z102023	AQS PSM5 POWER SUPPLY MODULE	
6	1	Z003402	AQS PSM1 POWER SUPPLY MODULE	
7	1	H14107	AQS PSD/2 BOARD	
8	1	H9503V1	AQS CCU11 COM CONTR UNIT	
9	1	H5813F2	AQS TCU3/4MB TIMING CONTR BOARD	
10	1	H9773	AQS FCU4/2 CONTROLLER BOARD	
11	1	H5817F1	AQS GCU3/4MB GRAD CONTR UNIT	
12	2	Z2778	BSMS FRONTPLATE BLIND 4TE	MRX
13	1	Z102520	AQS DRU -E ≥ ECL 02	
14	1	Z102116 Z102117	AQS RECEIVER BOARD RXAD 400 AQS RECEIVER BOARD RXAD 600	
15	1	Z003265 Z003936	AQS REFERENCE BOARD 400 AQS REFERENCE BOARD 600	
16	1	Z003642 Z003831	AQS SGU 400 AQS SGU 600	
17	6	Z12489	AQR FRONTPLATE BLIND 6TE	MRX
- [c]	20	25958	SCREW RRCH KR M2,5 x 12,3	MRX

a MEC Part: MRX = Part contained in AQS/2 MEC-PARTS MRX (Z105180)

b Chassis ≥ ECL01 necessary for pulse switch setting via software (the required BIS information is only in these chassis available)

c used for pos. 4, 12 and 17

The rack address must be set to ‘0x01’ (JU1A on the AQS/2 user bus rear side must be closed).

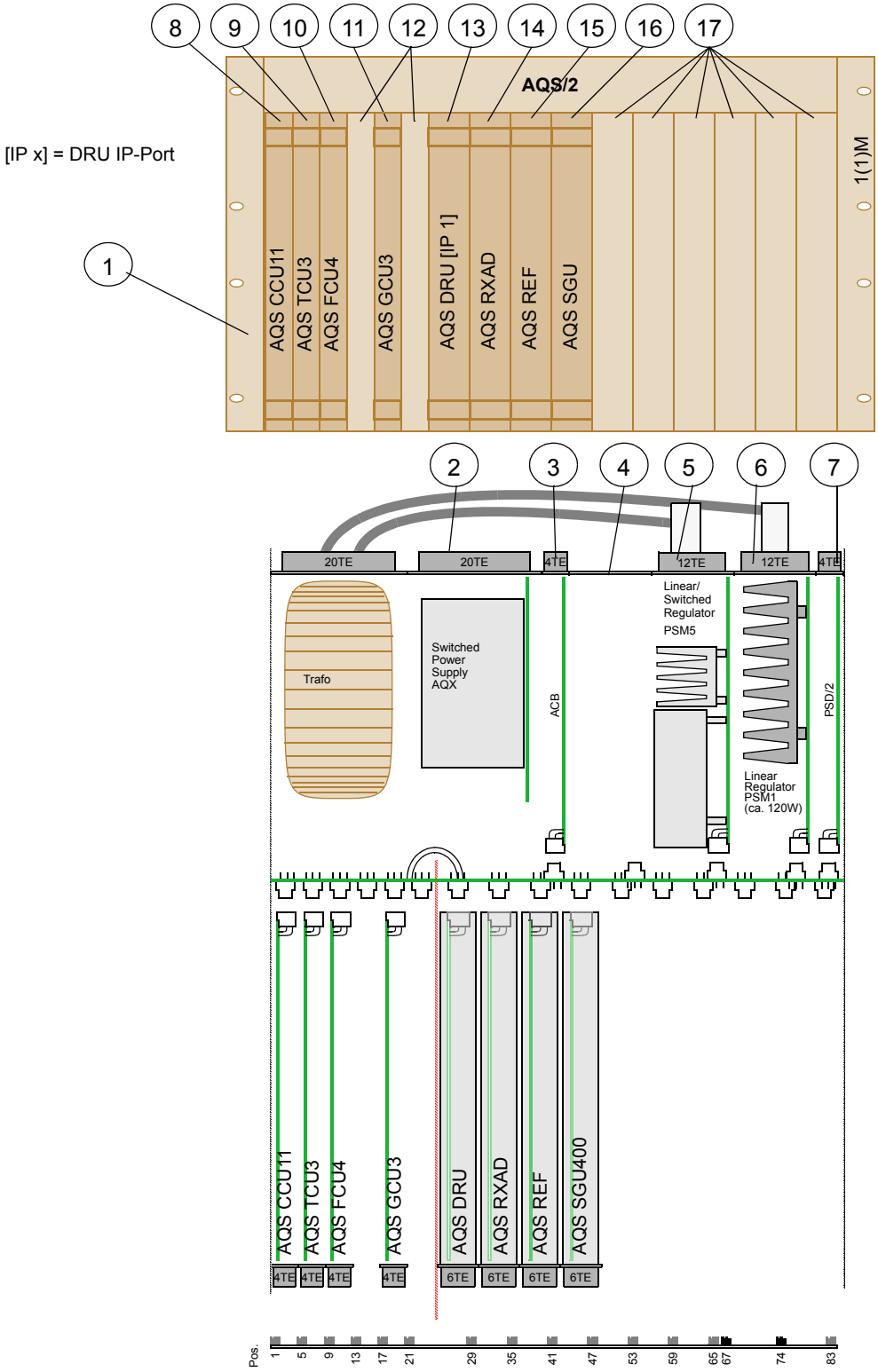
See ***"Rackadress Settings" on page 74***

! ***Pulse Switch Setting:***

Both pulse switches must be closed via AQS controller.

Board location ***3.6.9***

Figure 3.10. AQS/2 for 1 Channel (TX & RX) PharmaScan AVANCE



A typical 2 Channel AQS/2 BioSpec (2TX/1RX) 3.7

Bill of Material 3.7.1

Table 3.8. Bill of material

Pos.	Units	Part Number	Description	MP[a]
1	1	Z101618	AQS/2 CHASSIS WIRED ≥ ECL 01 [b]	
2	1	H9520	AQS POWER SUPPLY DIGITAL 450W	
3	1	H9500	AQS ACB EXTENDED BOARD	
4	1	Z104783	AQS PSM HPLNA	
5	1	Z102023	AQS PSM5 POWER SUPPLY MODULE	
6	1	Z003402	AQS PSM1 POWER SUPPLY MODULE	
7	1	H14107	AQS PSD/2 BOARD	
8	1	H9503V1	AQS CCU11 COM CONTR UNIT	
9	1	H5813F2	AQS TCU3/4MB TIMING CONTR BOARD	
10	1	H9773	AQS FCU4/2 CONTROLLER BOARD	
11	1	H5817F1	AQS GCU3/4MB GRAD CONTR UNIT	
12	2	Z2778	BSMS FRONTPLATE BLIND 4TE	MRX
13	1	Z102520	AQS DRU -E ≥ ECL 02	
14	1	Z102116 Z102117	AQS RECEIVER BOARD RXAD 400 AQS RECEIVER BOARD RXAD 600	
15	1	Z003265 Z003936	AQS REFERENCE BOARD 400 AQS REFERENCE BOARD 600	
16	2	Z003642 Z003831	AQS SGU 400 AQS SGU 600	
17	5	Z12489	AQR FRONTPLATE BLIND 6TE	MRX
- [c]	14	25958	SCREW RRCH KR M2,5 x 12,3	MRX

a MEC Part: MRX = Part contained in AQS/2 MEC-PARTS MRX (Z105180)

b Chassis ≥ ECL01 necessary for pulse switch setting via software (the required BIS information is only in these chassis available)

c used for pos. 12 and 17

The rack address must be set to ‘0x01’ (JU1A on the AQS/2 user bus rear side must be closed).

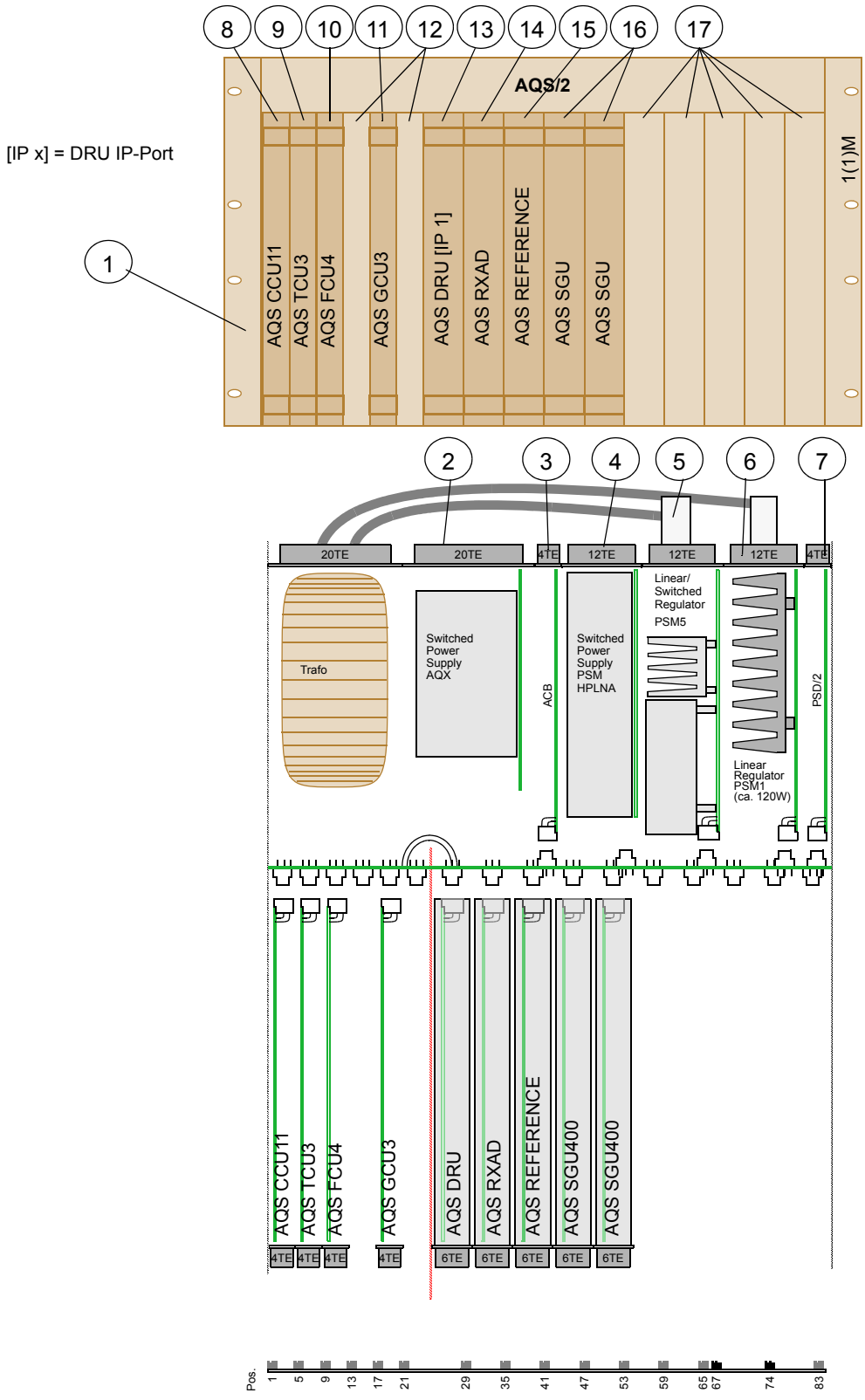
See ***"Rackadress Settings" on page 74***

! ***Pulse Switch Setting:***

Both pulse switches must be closed via AQS controller.

Board location ***3.7.3***

Figure 3.11. AQS/2 for 2 Channel (2TX/1RX) BioSpec AVANCE



A typical 4 to 8 RX Channel AQS/2 BioSpec (2-4TX/4-8RX) 3.8

Bill of Material 3.8.1

Table 3.9. Bill of material: Rack 1

Pos.	Units	Part Number	Description *Units for 3-4TX extension written in italics.*	MP[a]
1	1	Z101618	AQS/2 CHASSIS WIRED ≥ ECL 01 [b]	
2	1	H9520	AQS POWER SUPPLY DIGITAL 450W	
3	1	H9500	AQS ACB EXTENDED BOARD	
4	1	Z104783	AQS PSM HPLNA	
5	1	Z102023	AQS PSM5 POWER SUPPLY MODULE	
6	1	Z003402	AQS PSM1 POWER SUPPLY MODULE	
7	1	H14107	AQS PSD/2 BOARD	
8	1	H9503V1	AQS CCU11 COM CONTR UNIT	
9	1	H5813F2	AQS TCU3/4MB TIMING CONTR BOARD	
10	1	H9773 *H9727*	AQS FCU4/2 CONTROLLER BOARD *AQS FCU4/4 CONTROLLER BOARD*	
11	1	H5817	AQS GCU3 GRAD CONTR UNIT	
12	2	Z2778	BSMS FRONTPLATE BLIND 4TE	MRI
13	2	Z102520	AQS DRU -E ≥ ECL 02	
14	2	Z102116 Z102117	AQS RECEIVER BOARD RXAD 400 AQS RECEIVER BOARD RXAD 600	
15	2	Z003642 Z003831	AQS SGU 400 AQS SGU 600	
16	1	Z003265 Z003936	AQS REFERENCE BOARD 400 AQS REFERENCE BOARD 600	
17	2	Z12489 *see Pos.15*	AQR FRONTPLATE BLIND 6TE *AQS SGU*	MRI
18	1	Z104431	AQS PULSE SPLITTER	
- [c]	6	25958	SCREW RRCH KR M2,5 x 12,3	MRI

a MEC Part: MRI = Part contained in AQS/2 MEC-PARTS MRI (Z105116)

b Chassis ≥ ECL01 necessary for pulse switch setting via software (the required BIS information is only in these chassis available)

c used for pos. 12, and 17

Table 3.10. Bill of material: Rack 2

Pos.	Units	Part Number	Description *Units for 8 RX extension written in italics.*	MP[a]
30	1	Z103493	AQS/2-M CHASSIS WIRED	
31	1	H9489	AQS POWER SUPPLY DIGITAL 350W	
32	1	Z104432	AQS RF-SPLITTER	
33	1	Z12170	BSMS FRONTPLATE BLIND 12TE	MRI
34	1	Z102023	AQS PSM5 POWER SUPPLY MODULE	
35	1	Z003402	AQS PSM1 POWER SUPPLY MODULE	
36	1	Z2778	BSMS FRONTPLATE BLIND 4TE	MRI
37	2*(6)*	Z102520	AQS DRU -E ≥ ECL 02	
38	2*(6)*	Z102116 Z102117	AQS RECEIVER BOARD RXAD 400 AQS RECEIVER BOARD RXAD 600	
39	5*(1)*	Z14119	AQS FRONTPLATE 1MM 12TE	MRI
40	5*(1)*	Z14120	AQS COVERPLATE 8TE	MRI
41	1	Z15357	SCHILD PL GE “AQS RACK ON” Z4K-4466 (Marking Z4K-4466 on ***left*** side)	MRI
42	1	Z15358	SCHILD PL GE “AQS EXT RACK ON” Z4K-4467 (Marking Z4K-4467 on ***right*** side)	MRI
- [b]	6	25958	SCREW RRCH KR M2,5 x 12,3	MRI

a MEC Part: MRI = Part contained in AQS/2 MEC-PARTS MRI (Z105116)

b used for pos. 33, 36 and 39

Jumper Setting *3.8.2*

Rack 1:

The rack address must be set to ‘0x01’ (JU1A on the AQS/2 user bus rear side must be closed).

See ***"Rackadress Settings" on page 74***

! ***Pulse Switch Setting:***

All pulse switches must be opened via AQS controller.

Rack 2:

The rack code must be set to ‘0x102’ (rotary switches SW3..1 on the AQS/2-M user bus rear side).

The power-up delay must be set to ‘1’ (rotary switch on chassis rear side).

See ***"Rackcode Settings" on page 108***

! ***Pulse Switch Setting:***

All pulse switches must be closed via AQS controller.

Guide Rail changes *3.8.3*

Rack 1:

To change the guide rails correctly please follow the exact order as described below.

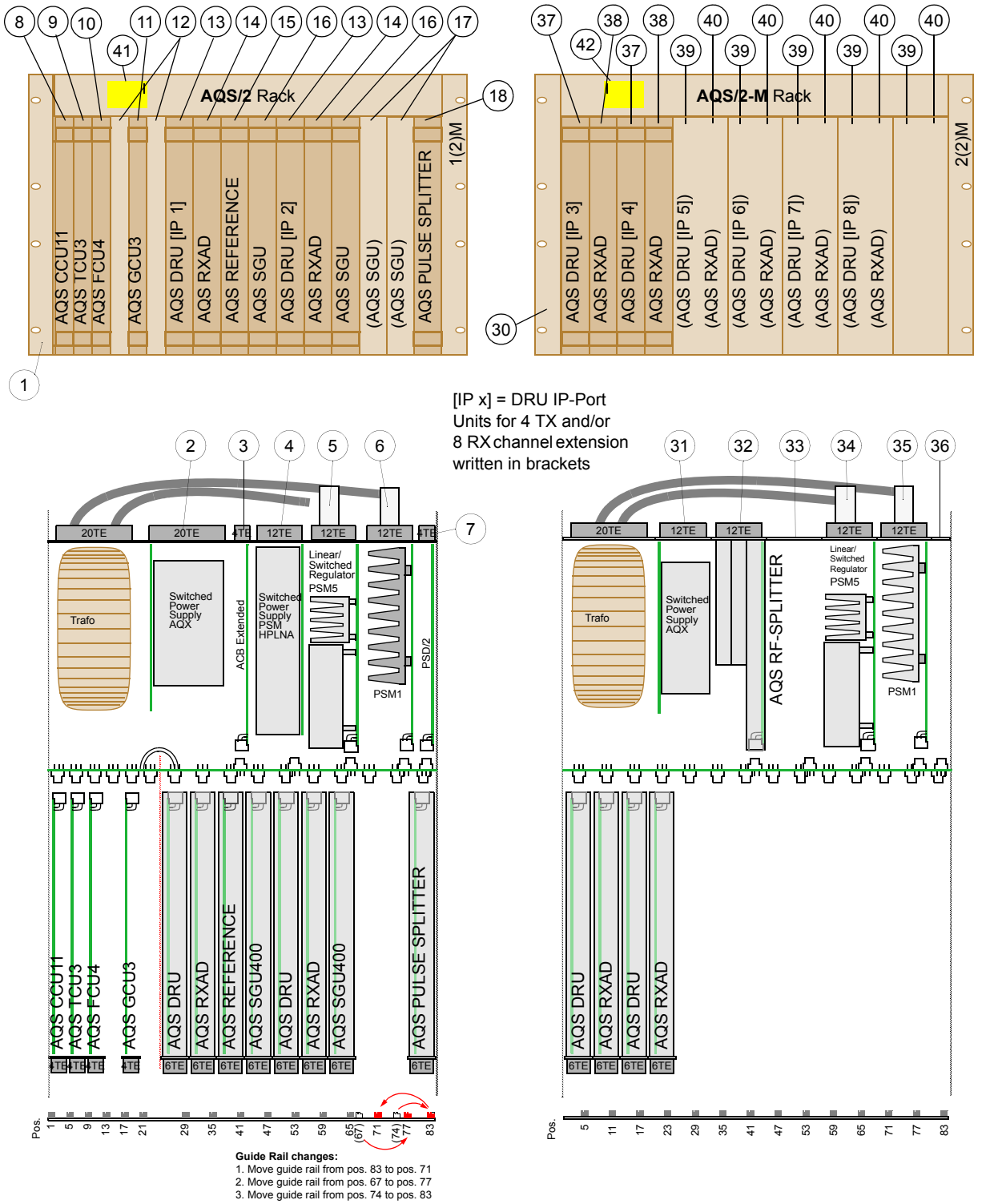
1. Move guide rail from pos. 83 to pos. 71
2. Move guide rail from pos. 67 to pos. 77
3. Move guide rail from pos. 74 to pos. 83

Rack 2:

No changes

Board location **3.8.4**

Figure 3.12. AQS/2 for 4 to 8 RX Channel AQS BioSpec (2-4TX/4-8RX) AVANCE



A typical 1 and 2 Channel AQS FTMS 3.9

Bill of Material 3.9.1

Table 3.11. Bill of material

Pos.	Units	Part Number	Description *Units for 2nd channel extension written in italics.*	MP[a]
1	1	Z101618	AQS/2 CHASSIS WIRED	
2	1	H9489	AQS POWER SUPPLY DIGITAL 350W	
3	2	Z12170	BSMS FRONTPLATE BLIND 12TE	
4	1	Z003403	AQS PSM2 POWER SUPPLY MODULE	
5	1	Z003402	AQS PSM1 POWER SUPPLY MODULE	
6	1	A3144	AQS FTMS PSD	
7	1	H9503	AQS CCU11 COM CONTR UNIT	
8	1	H5813	AQS TCU3 TIMING CONTR BOARD	
9	1	H9773	AQS FCU4/2 CONTROLLER BOARD	
10	3	Z2778	BSMS FRONTPLATE BLIND 4TE	FTMS
11	1	Z102520	AQS DRU -E	
12	1	Z102501	AQS RECEIVER BOARD RXAD FTMS	
13	1	Z003265	AQS REFERENCE BOARD 400	
14	1	Z003643	AQS SGU FTMS	
15	3 *1*	Z12489 *Z003643*	AQR FRONTPLATE BLIND 6TE *AQS SGU FTMS*	FTMS
16	1	Z13955	AQS FRONTPLATE 1MM 18TE	FTMS
17	1	Z13954	AQS COVERPLATE 18TE	FTMS
- [b]	22	25958	SCREW RRCH KR M2,5 x 12,3	FTMS

a MEC Part: FTMS = Part contained in AQS/2 MEC-PARTS FTMS (Z103602)

b used for pos. 3, 10, 15 and 16

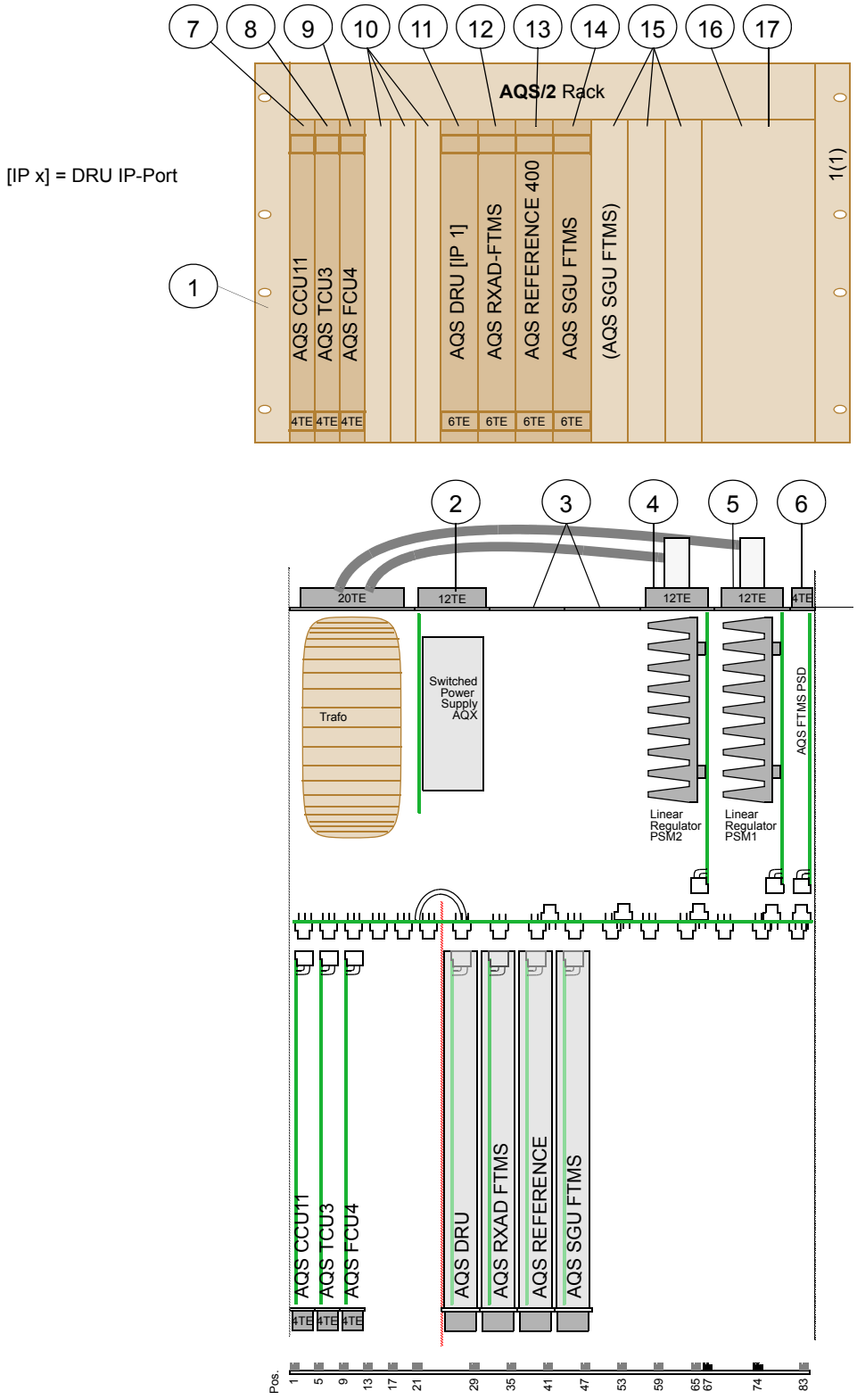
Jumper Setting 3.9.2

The rack address must be set to ‘0x39’ (JU1A and JU1D to JU1F on the AQS/2 user bus rear side must be closed).

See ***"Rackadress Settings" on page 74***

Board location ***3.9.3***

Figure 3.13. AQS for 1 and 2 Channel FTMS AVANCE



AQS/2 Mainframe 4

Introduction 4.1

The AQS/2 mainframe is the new version of the AQS mainframe. It consists of a 6 slot VME bus part (previous AQS: 8 slot) and a 10 slot user bus part (previous AQS: 8 slot).

The VME part can be equipped with VME boards (e.g. CCU, FCU. TCU, GCU). The user bus part is designed to be equipped with AQS RF units (e.g. SGU, Reference Board, RX, RXAD, DRU, AQS Preamp, BLA2BB). Also AQR units such as the 3-Channel Router do fit into the AQS/2 mainframe, however in this case special adapters (see ***"Adapters" on page 94***) are necessary.

On the rear side, linear power supply modules (PSM1, PSM2, PSM3, PSM5) and switched power supply modules for the VME part and for the internal RF power amplifiers are placed. Also different distribution and amplifier control boards (PSD, ACB Standard, ACB Extended) depending on the rack configuration (***"AQS Configurations" on page 25***) fit into the chassis.

The transformer, which feeds the linear power supply modules, is part of the mainframe and is located on the rear side.

The mainframe is cooled with 8 fans, which are located in a fan tray on top of the mainframe. The fan tray is serviceable without removing the mainframe from the spectrometer cabinet. (see ***"Fan Tray Service Instructions" on page 71***)

Monitoring of proper fan operation and over temperature protection is another new feature of the AQS/2 mainframe.

Technical Data 4.2

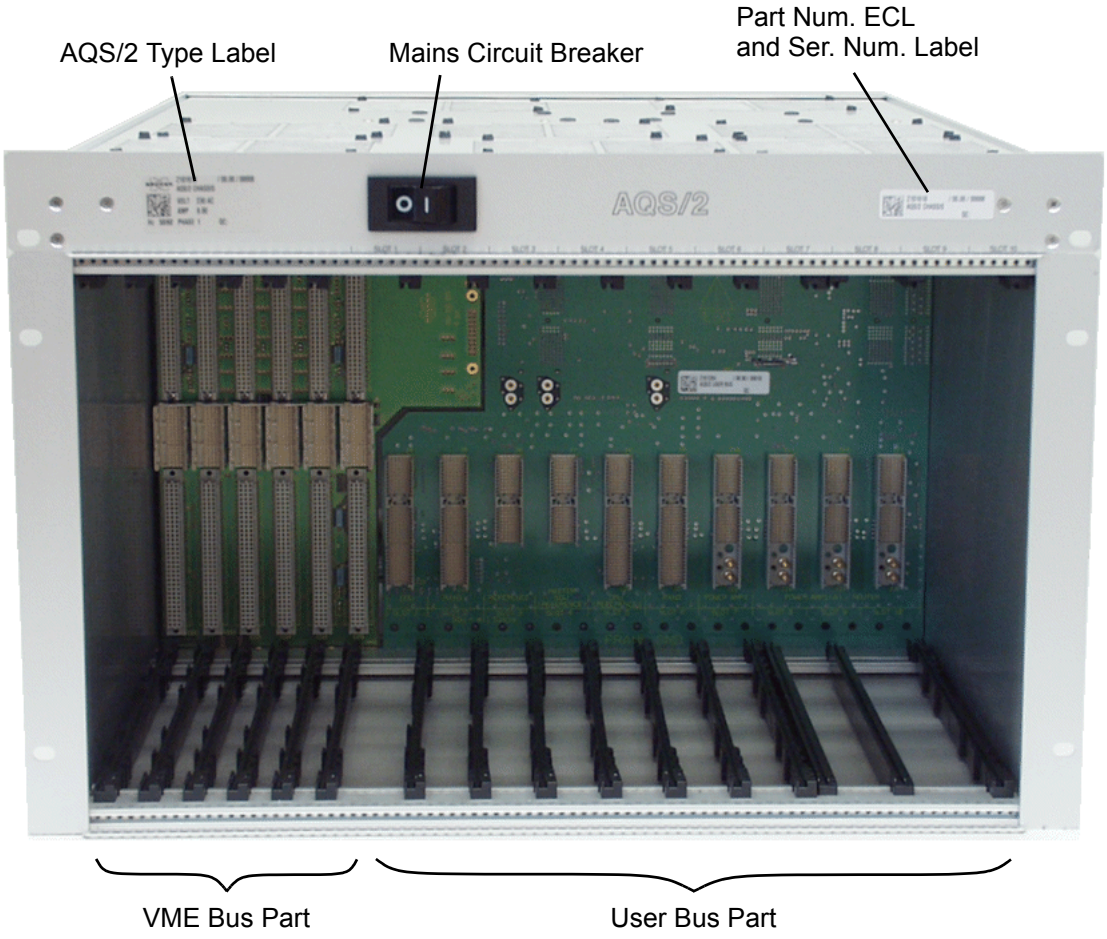
AC Input Voltage (mains selector range)	195-215 / 210-230 / 220-245	Vrms
AC Frequency range	47..63	Hz
AC Input Current	max. 8	Arms
AC Fuse 5x20mm (2pcs. 5x20mm, time-lag T, type H)	8A / 250V	
Dimensions (hight x width x depth)	310 x 483 x 570	mm
Weight (without units)	approx. 20	kg

Environmental conditions:

The AQS/2 mainframe is designed as a subunit in the electronics cabinet of the spectrometer. For the environmental conditions outside the cabinet please refer to the site planning guide of the spectrometer system.

Front View *4.3*

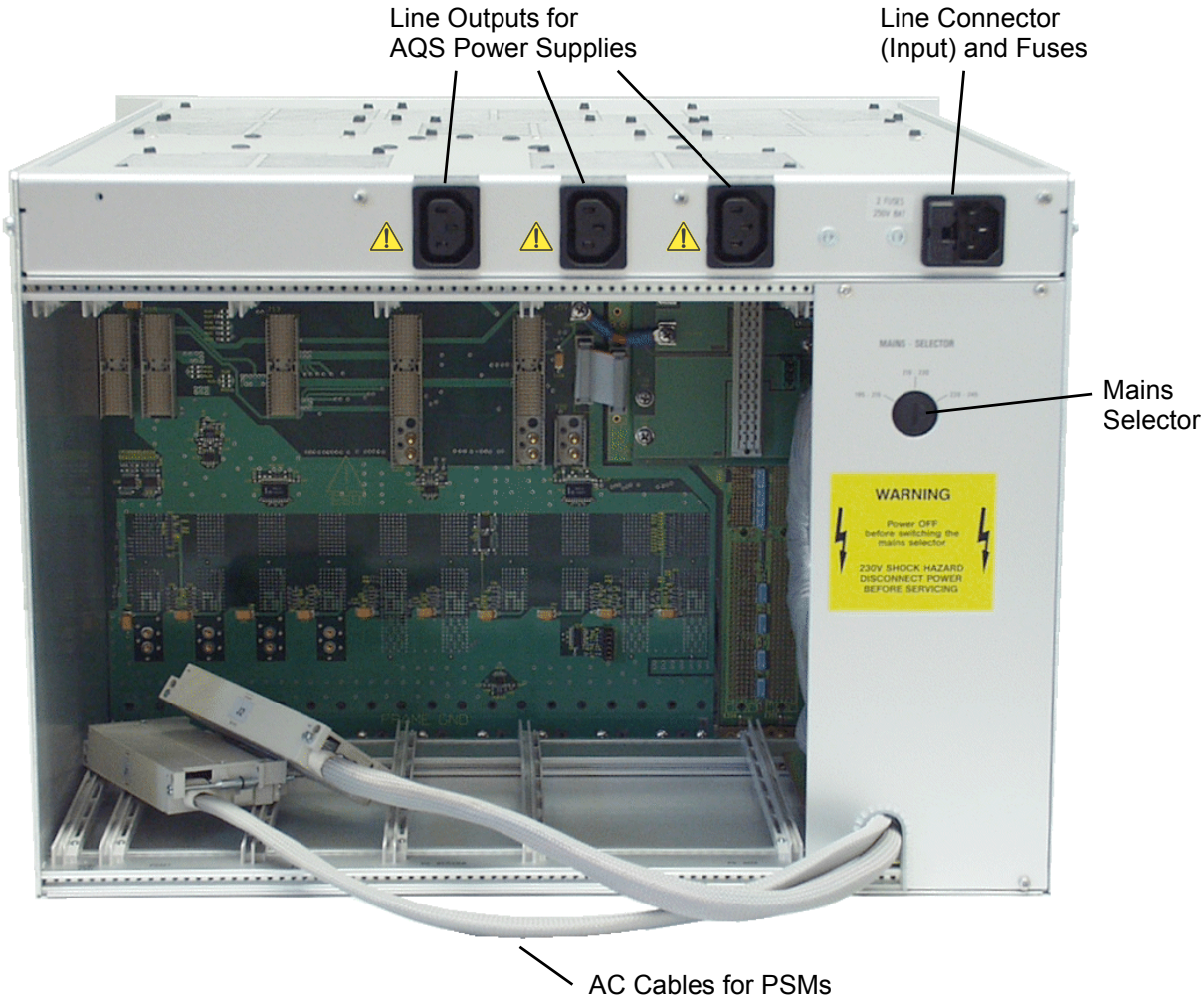
Figure 4.1. AQS/2 Chassis front view



Rear View 4.4

The rear view shows the housing of the power supply boards. On the right hand side is the transformer housing with the appropriate AC cables located.

Figure 4.2. AQS/2 Chassis rear view



Line Outputs:

Only connect AQS POWER SUPPLY units to these connectors.

- AQS POWER SUPPLY DIGITAL 350W (H9489)
- AQS POWER SUPPLY DIGITAL 450W (H9520)
- POWER SUPPLY COMPACT 28V 20A (W1345050)
- AQS PSM5 POWER SUPPLY MODULE (Z102023)
- AQS PSM HPLNA (Z104783)

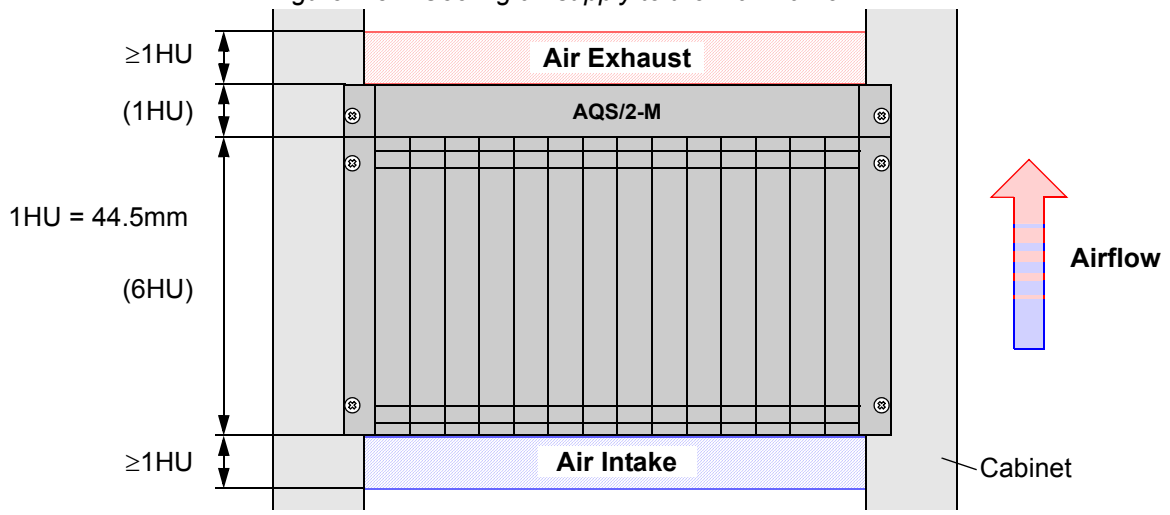
Installation in electronics cabinet 4.5

The AQS/2 mainframe must be installed at it's designated position in the electronics cabinet to ensure proper air ventilation for the cooling fans. The position may vary in different cabinet types and sizes.

! ***At least one height unit (1HU) above and below the mainframe must be reserved for the cooling air supply.***

Special air baffle plates may be used to support efficient ventilation. Typically the air intake is from the front and the exhaust towards the back of the cabinet.

Figure 4.3. Cooling air supply to the mainframe



The mainframe must be fixed by at least 4 screws into the cabinet. The power cable is included in the cabinet wiring.

Preparation for Use 4.6

Prior to the first power-up of the AQS/2 mainframe, it must be ensured that the mains selection switch is in the correct position. (see selector on the back side of the AQS/2)

The size of the linear power supply modules is designed for minimal power dissipation; therefore the transformer input voltage should be matched to the mains voltage at the installation site.

Generally, the mains selection switch should be set to the corresponding voltage range, even if the mains power is weak (max. fluctuations ± 6%).

- Factory setting for 230V mains supply = 220-245V

Selector Setting for combined Voltages 4.6.1

In countries with 110-120V mains supply such as USA and Canada combined line voltages may be used. In this case set the selector switch to 195-215V.

AC Power Line Fuses 4.7

The AQS/2 is protected by two fuses as specified on the power supply nameplate. The fuses are located in a removable fuse holder next to the AC power connector. Always use time-lag T fuse types with high breaking capacity H.

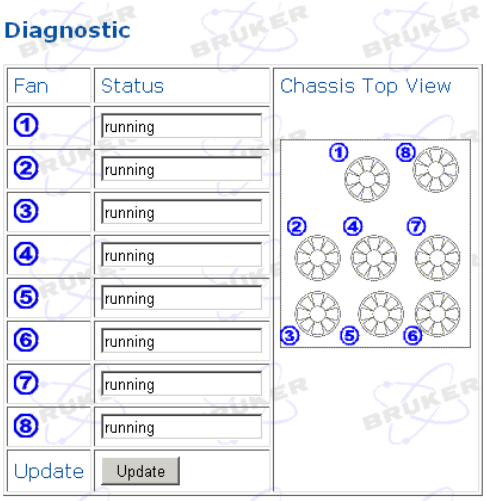
Mains Circuit Breaker 4.8

The mains circuit breaker on the front can only be turned on when a life AC power line is connected to the mainframe. In the event of an AC power loss in the spectrometer cabinet, the mains circuit breaker resets automatically into the off position.

Fan Control and Over Temperature Protection (ECL ≥ 01 only) 4.9

The operation of all fans is individually controlled by the AQS controller and the control circuit on the AQS/2 user bus. If a fan fails to operate, a corresponding error message will occur after reading the fan status by UniTool or by the DRU.

Figure 4.4. DRU Service Web: AQS Chassis Diagnostic



If the temperature inside the mainframe exceeds the absolute maximum limit of save operation, the mains circuit switch is turned off automatically to prevent permanent damage to the AQS units.

Figure 4.5. AQS/2 AC Wiring

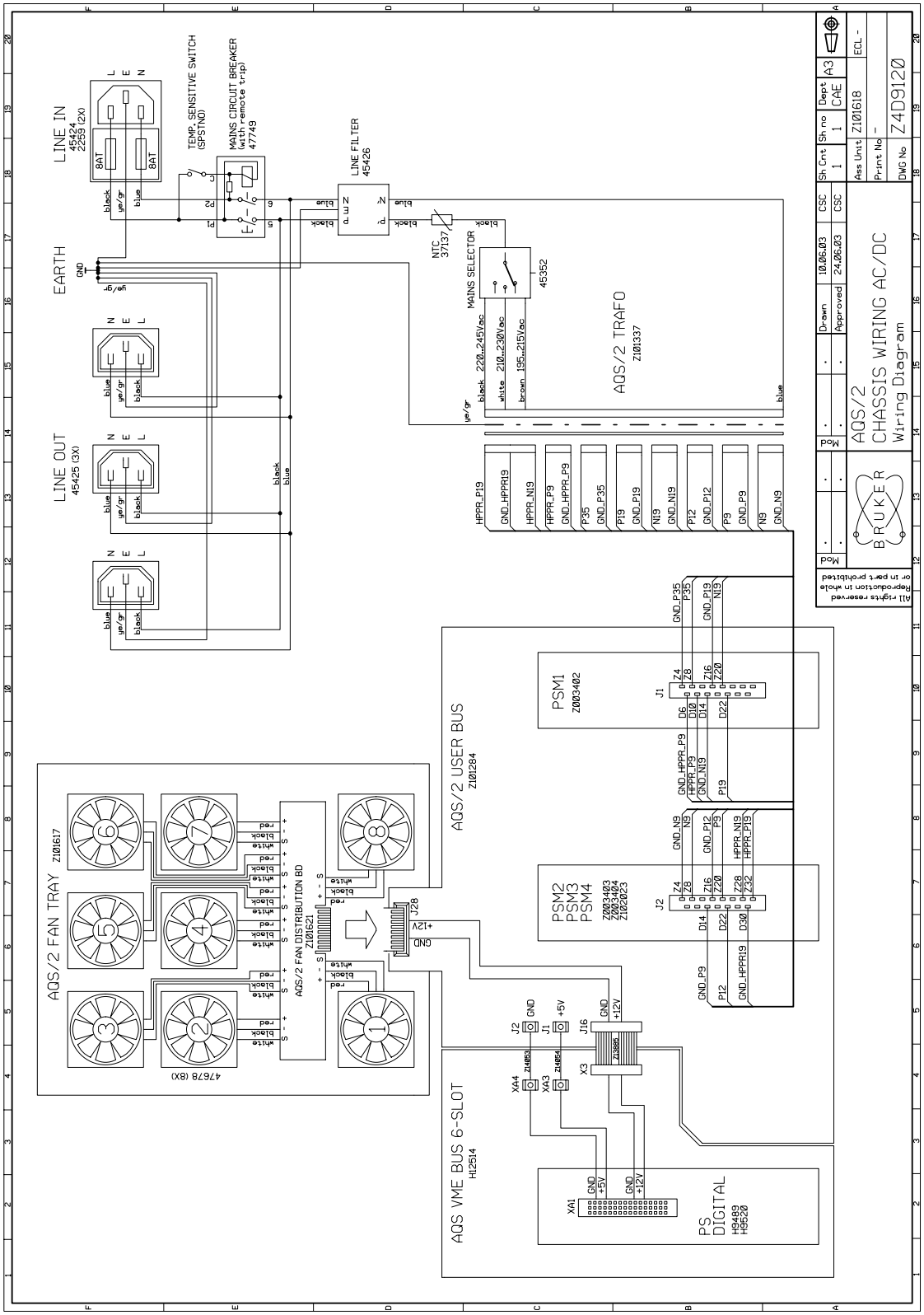
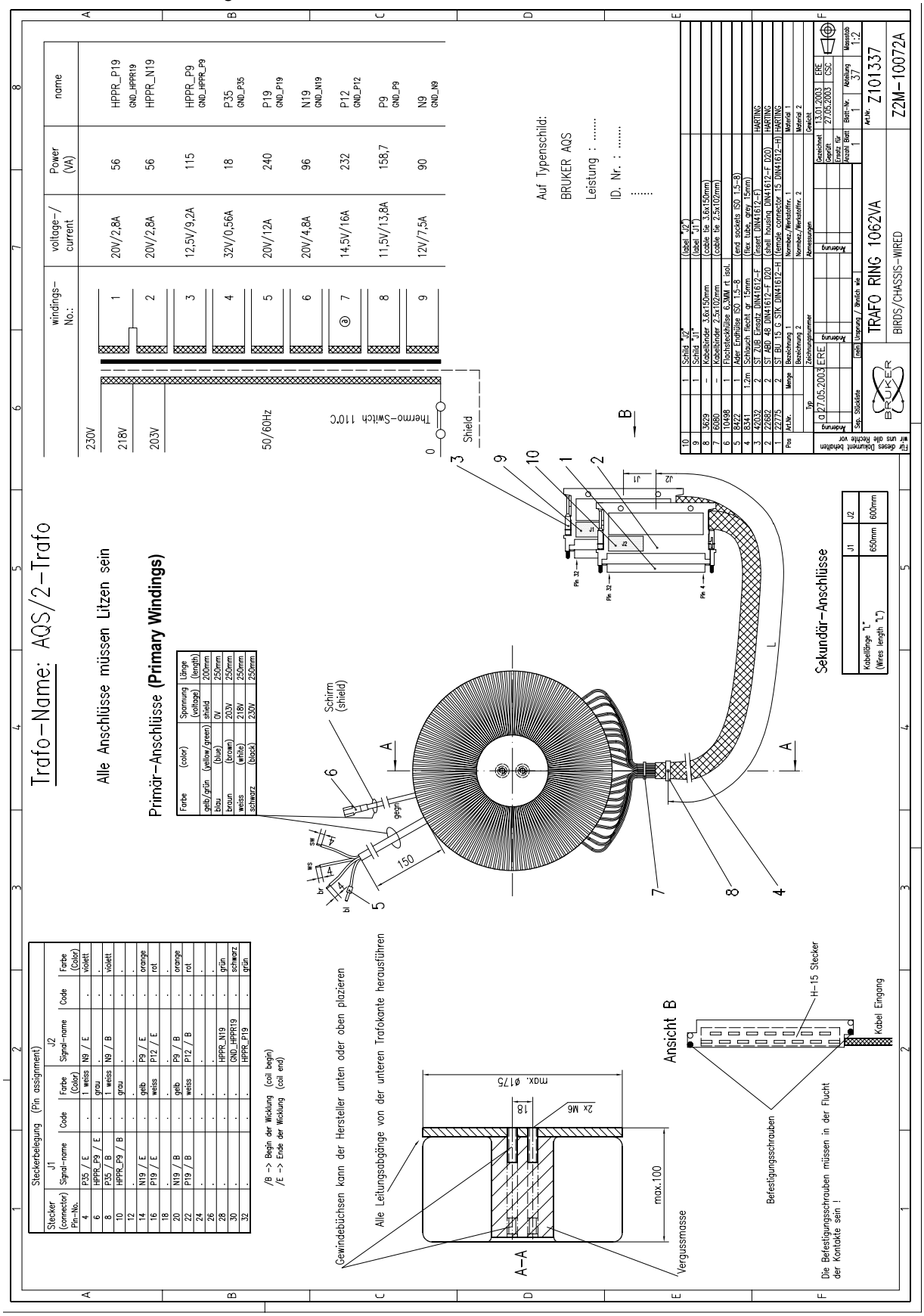


Figure 4.6. AQS/2 Transformer

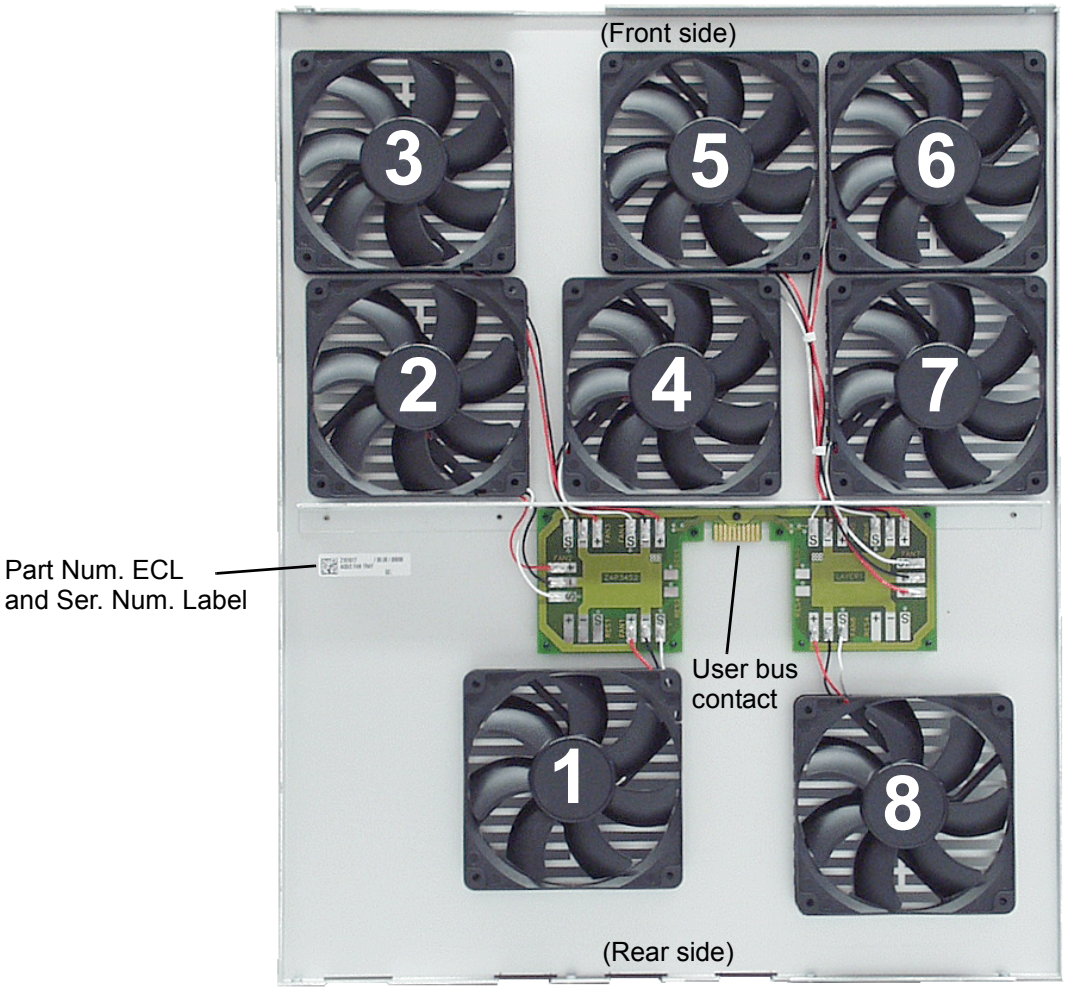


Fans *4.11*

The fans are located in the fan tray on top of the mainframe. They are supplied and controlled via the AQS/2 user bus.

The fan tray is serviceable without removing the mainframe from the spectrometer cabinet. (see ***"Fan Tray Service Instructions" on page 71***)

Figure 4.7. AQS/2 Fan Tray (Bottom view)



Fan Tray Service Instructions 4.12

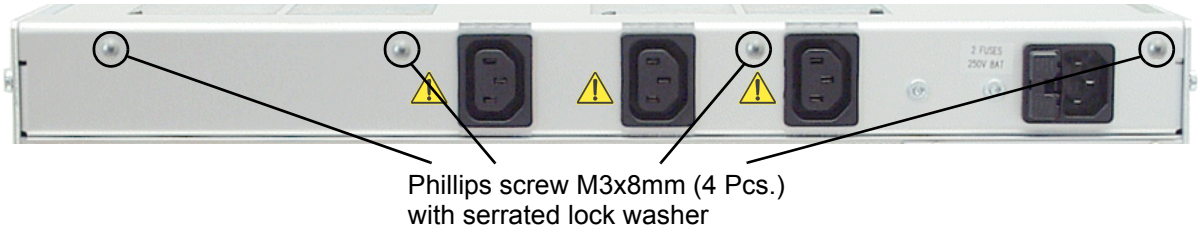
! ***Only qualified Bruker personnel are allowed to service the AQS/2 mainframe.***

Fan Tray removal 4.12.1

To remove the Fan Tray from the AQS/2 mainframe please follow the steps exactly as described below:

1. Turn of chassis with mains circuit breaker
2. Remove AC power line (rear side)
3. Remove 4 screws on the rear side

Figure 4.8. Fan Tray screws rear side

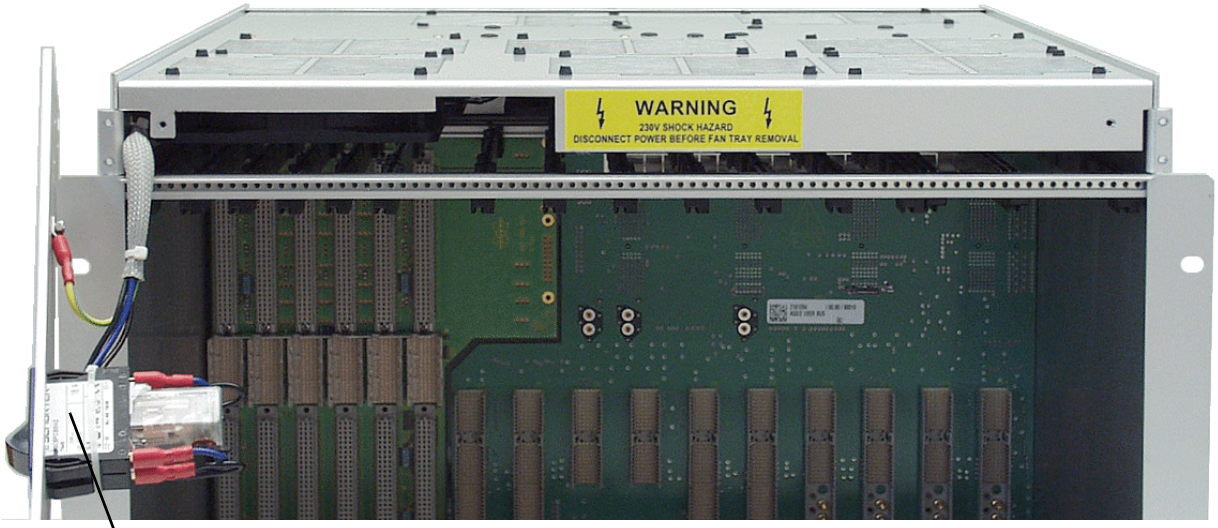


4. Remove 6 screws on the front side

Figure 4.9. Fan Tray screws front side

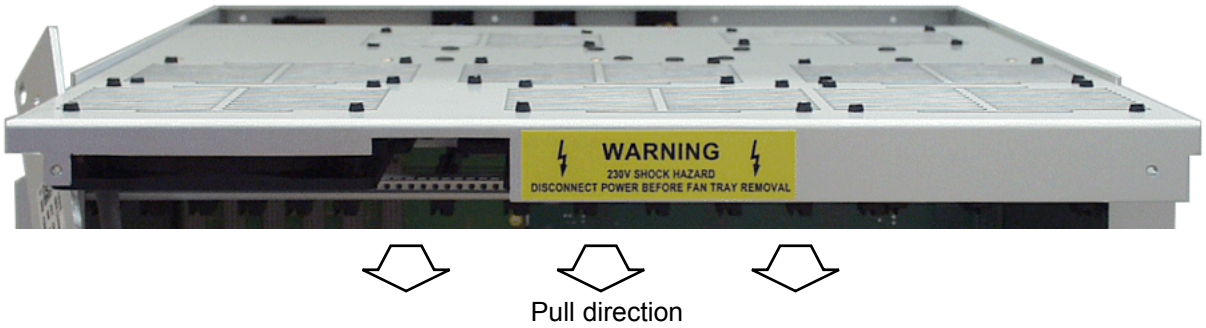
5. Carefully pull the front panel away from the mainframe and place it towards the left side (dangling from the cable)

Figure 4.10. Front panel removal



6. Remove the fan tray by pulling it gently towards the front

Figure 4.11. Fan Tray removal



Fan Tray reassembly *4.12.2*

To replace the fan tray in the AQS/2 mainframe follow the steps as described above in ***reverse order***.

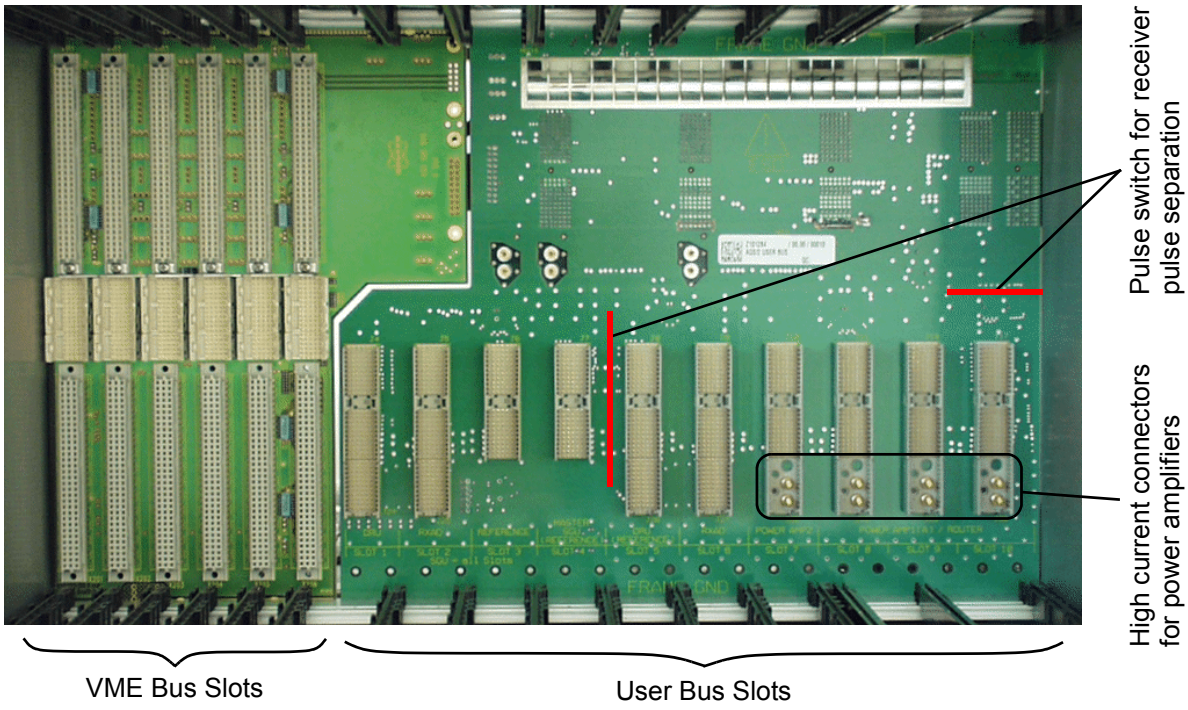
Make sure that:

- the fan tray sits flat on the guide rails on either side of the mainframe before final insertion
- no wires are squeezed in between the front panel and the fan tray
- all screws are secured and fastened properly (rear side screws with serrated lock washers)
- all fans turn freely after power up

Backplane (User Bus) 4.13

The User Bus is designed to route all specific signals and power supplies to the specific boards. It represents the ground point of the AQS/2 and is connected to the chassis frame. For detailed information about user bus signals see ***"AQS/2 signal and information paths" on page 15***, ***"Synchronous signals" on page 20*** and***"20MHz Clock Distribution" on page 29***.

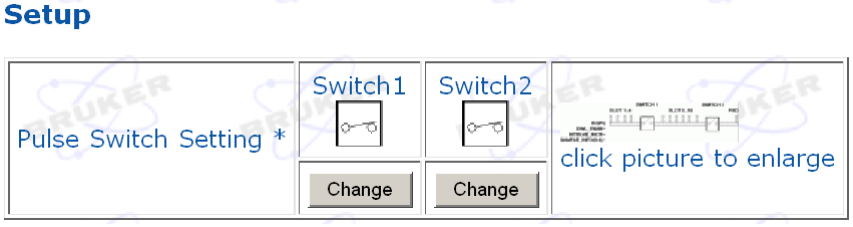
Figure 4.12. AQS/2 VME and User Bus (front view)



Pulse switch for receiver pulse separation 4.13.1

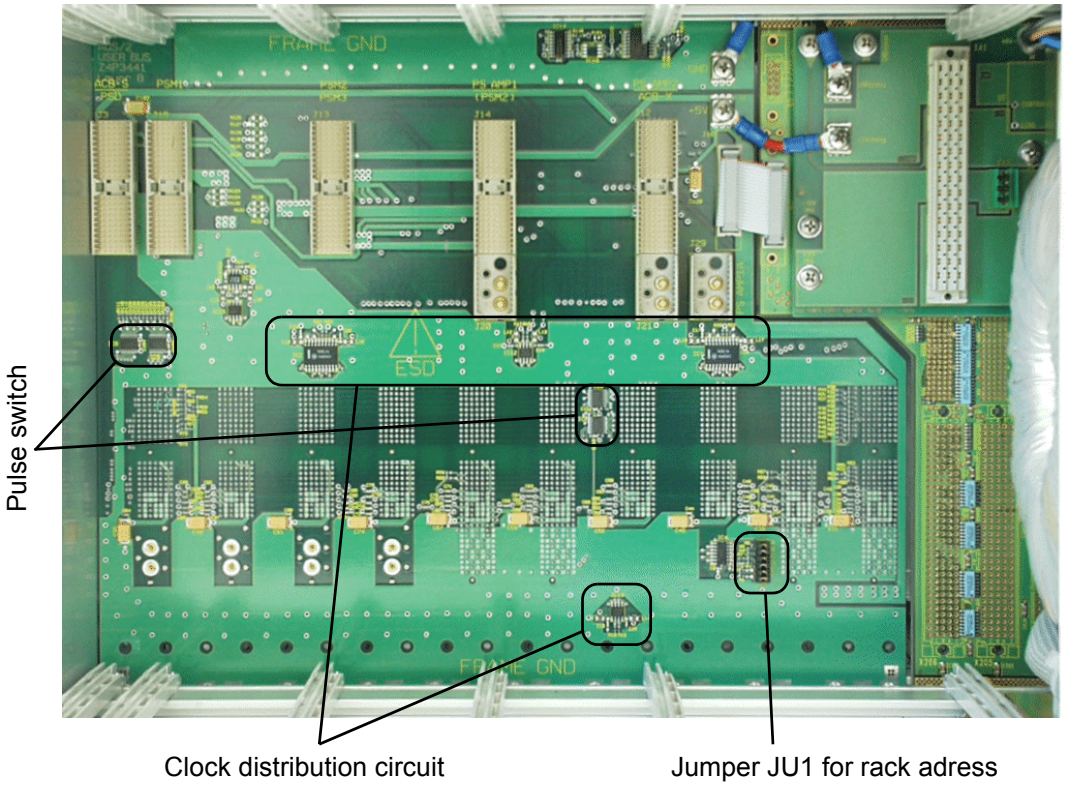
The User Bus is equipped with two pulse switches. One is located between slots 4 and 5, the other between slot 10 and the ACB-S/PSD slot. Both switches are either controlled by jumper JU1 E and F or via AQS controller (I2C).

Figure 4.13. DRU Service Web: AQS Chassis Setup



! ***To enable control via AQS controller both jumpers must be left open.***

Figure 4.14. AQS/2 VME and User Bus (rear view)



Rackadress Settings *4.13.2*

- JU1 A..D = AQS controller setting or chassis type (HEX number)
- JU1 E = pulse switch between slots 4 and 5
- JU1 F = pulse switch between slot 10 and PSD

Table 4.1. Rack Adress Setting Jumper JU1

0x	N		N				Rack Adress
Jumper JU1	F (2)	E (1)	D (8)	C (4)	B (2)	A (1)	Configuration
0x 3..	■	■					Single RX
0x 0..	-	-					Multi-RX or pulse switch controlled by AQS controller
0x ..1			-	-	-	■	AQS controller = DRU1 in Slot 1
0x ..9			■	-	-	■	AQS controller = SGU1 in Slot 4
0x ..8			■	-	-	-	AQS controller = SGU1 in Slot 5
0x ..7			-	■	■	■	AQS controller = SGU1 in Slot 6
0x ..6			-	■	■	-	2nd Chassis

■ = Jumper closed [-] = Jumper open

User Bus Schematics *4.13.3*

Figure 4.15. User Bus Block Diagram

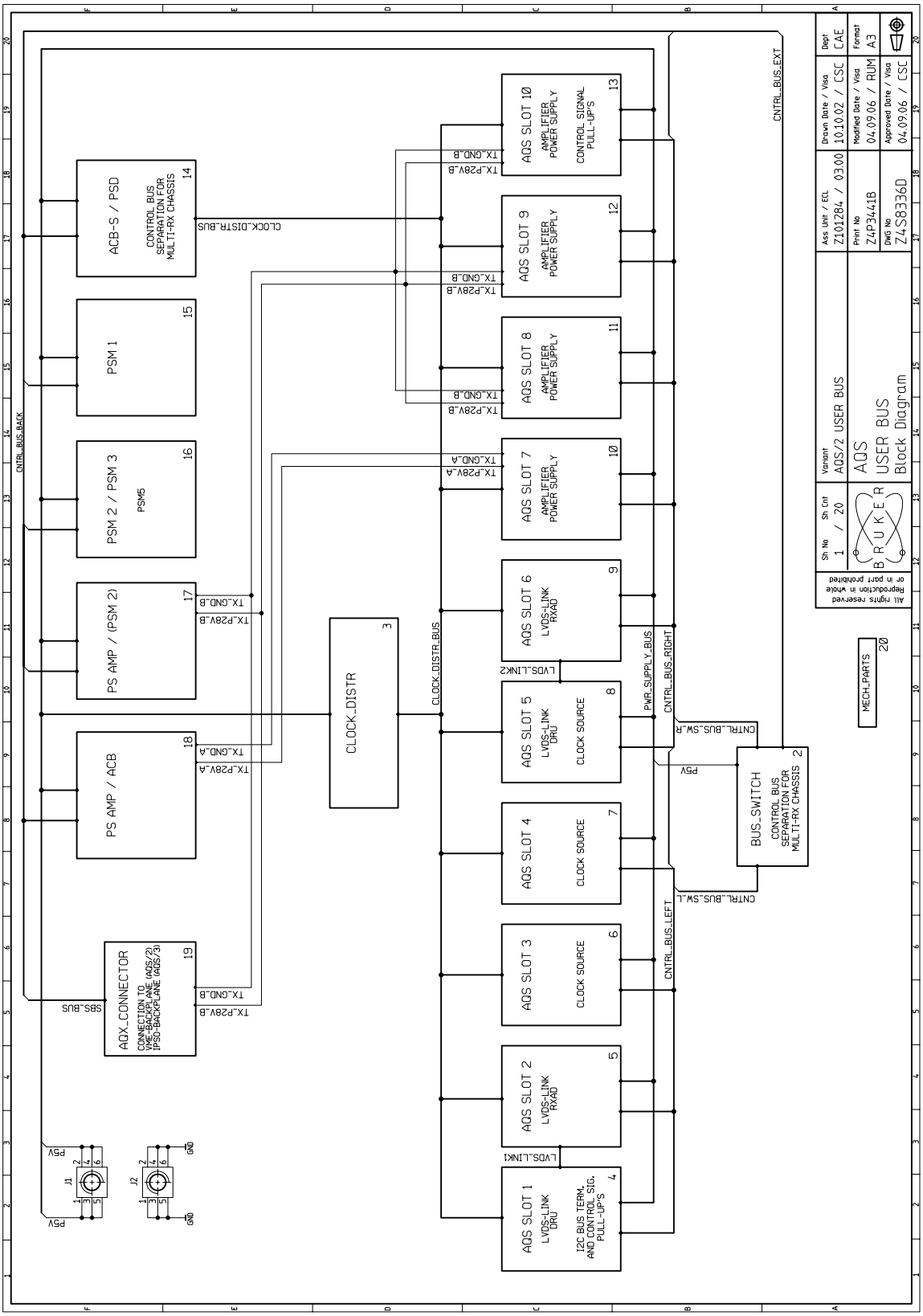


Figure 4.16. Fan Control & Pulse Switch

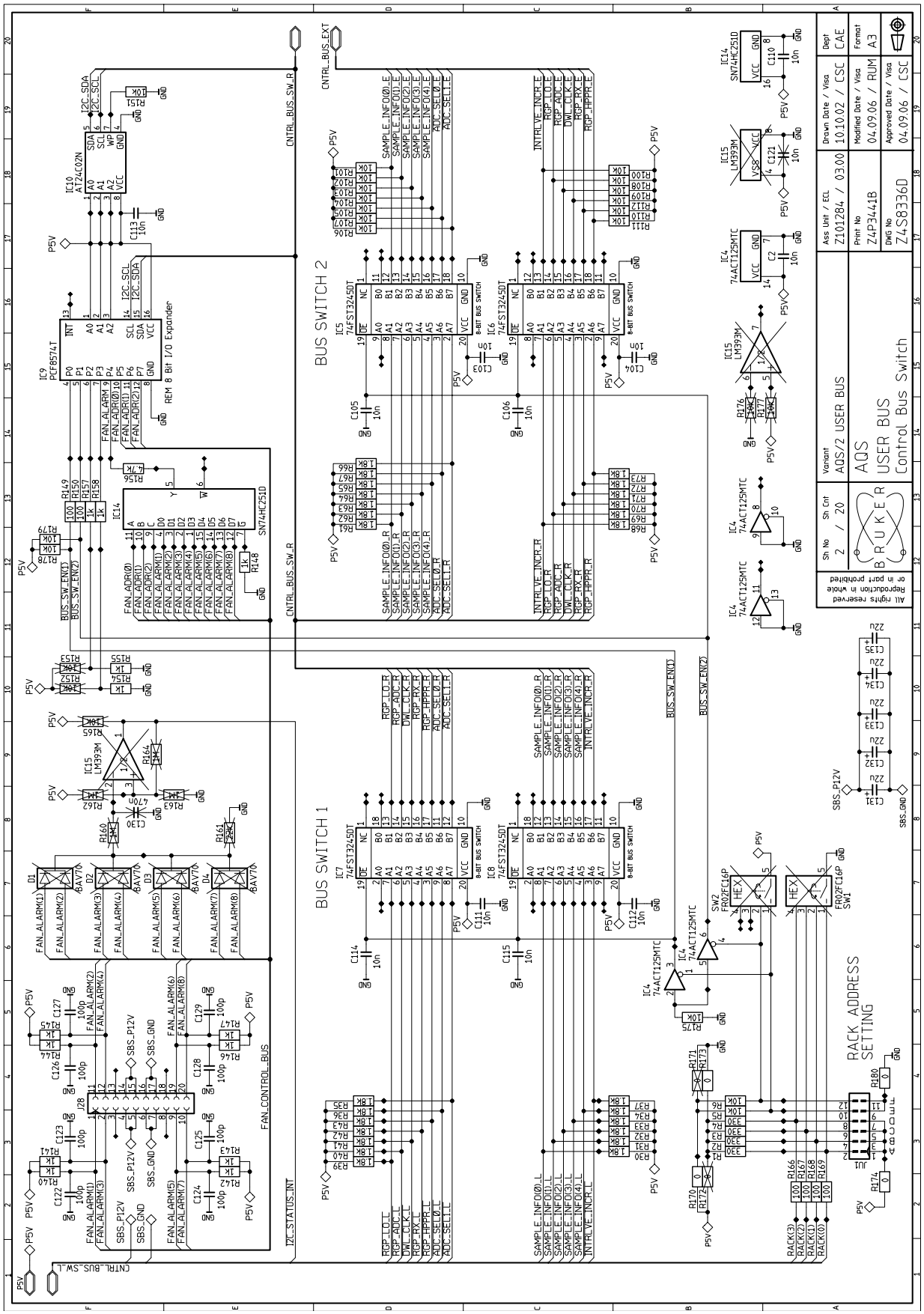


Figure 4.17. Clock Distribution

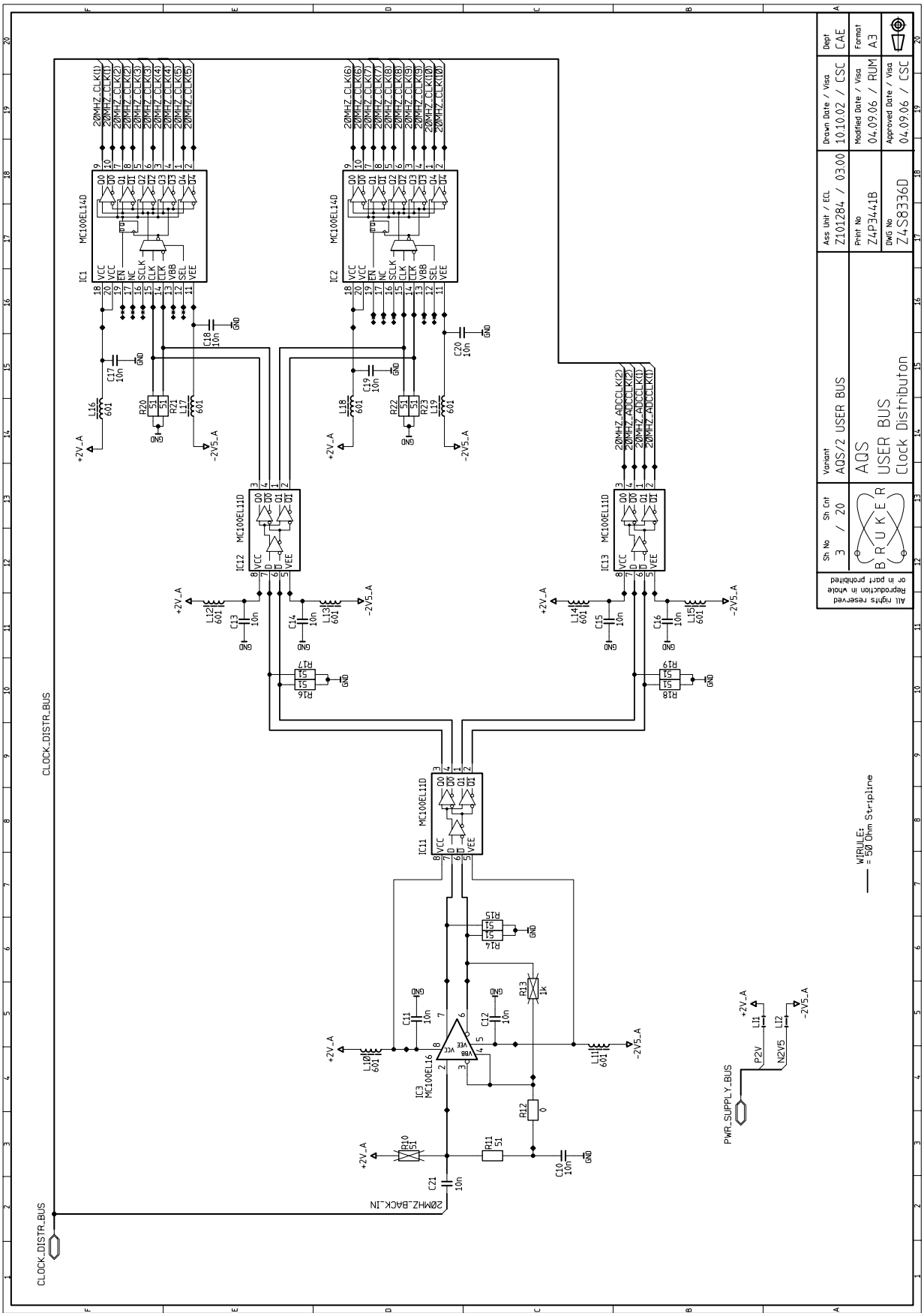


Figure 4.18. User Bus Slot 1

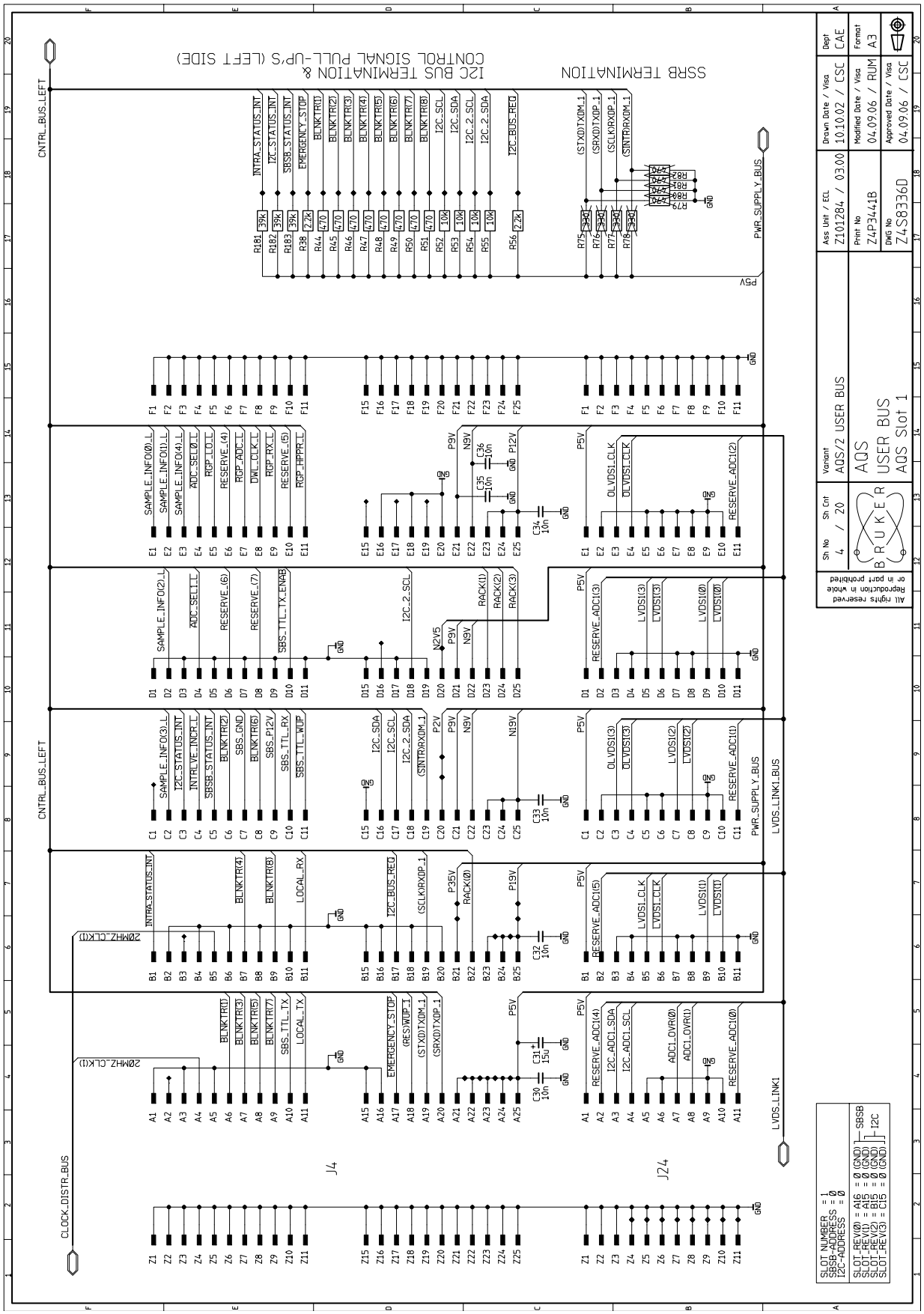


Figure 4.19. User Bus Slot 2

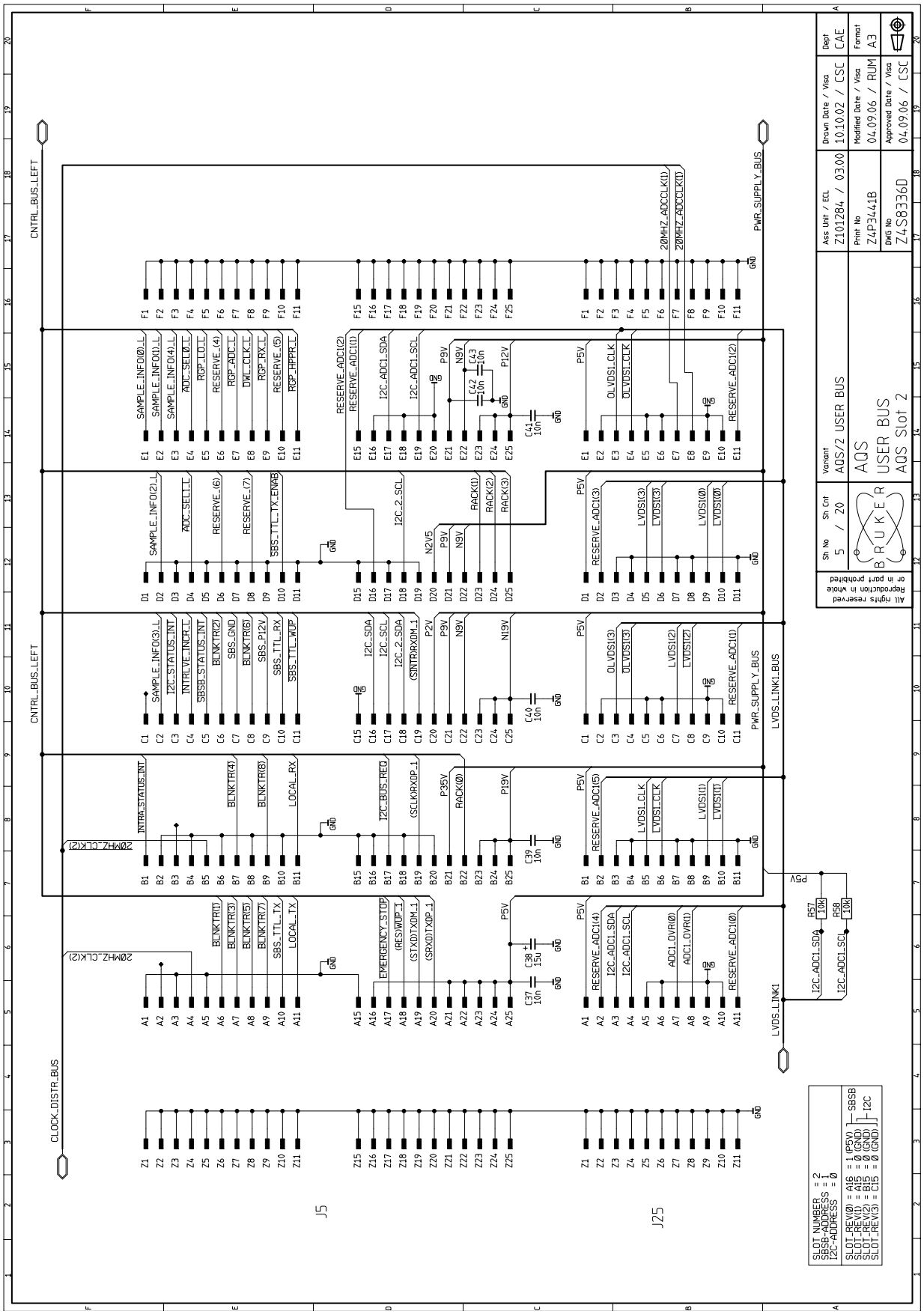


Figure 4.20. User Bus Slot 3

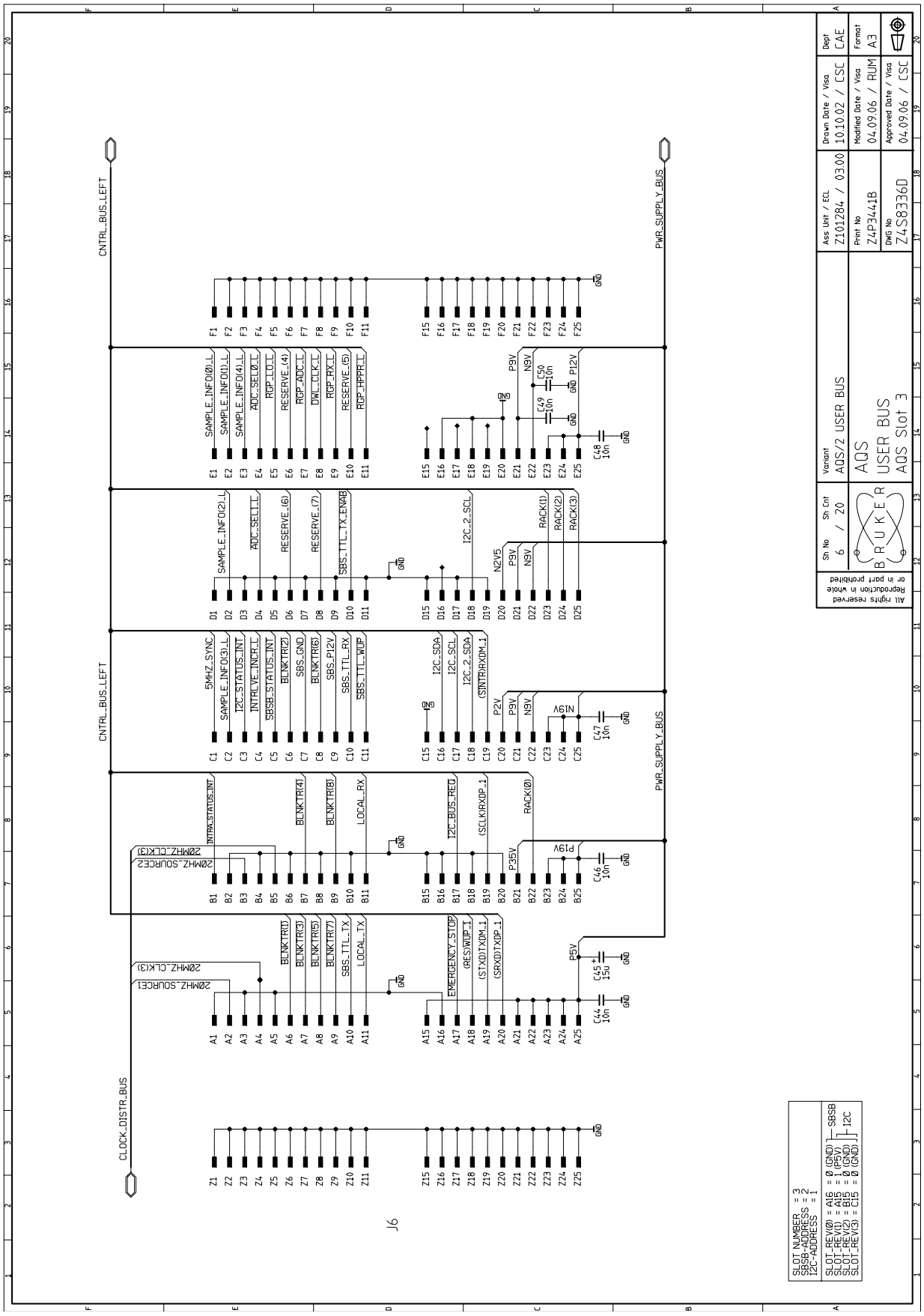


Figure 4.21. User Bus Slot 4

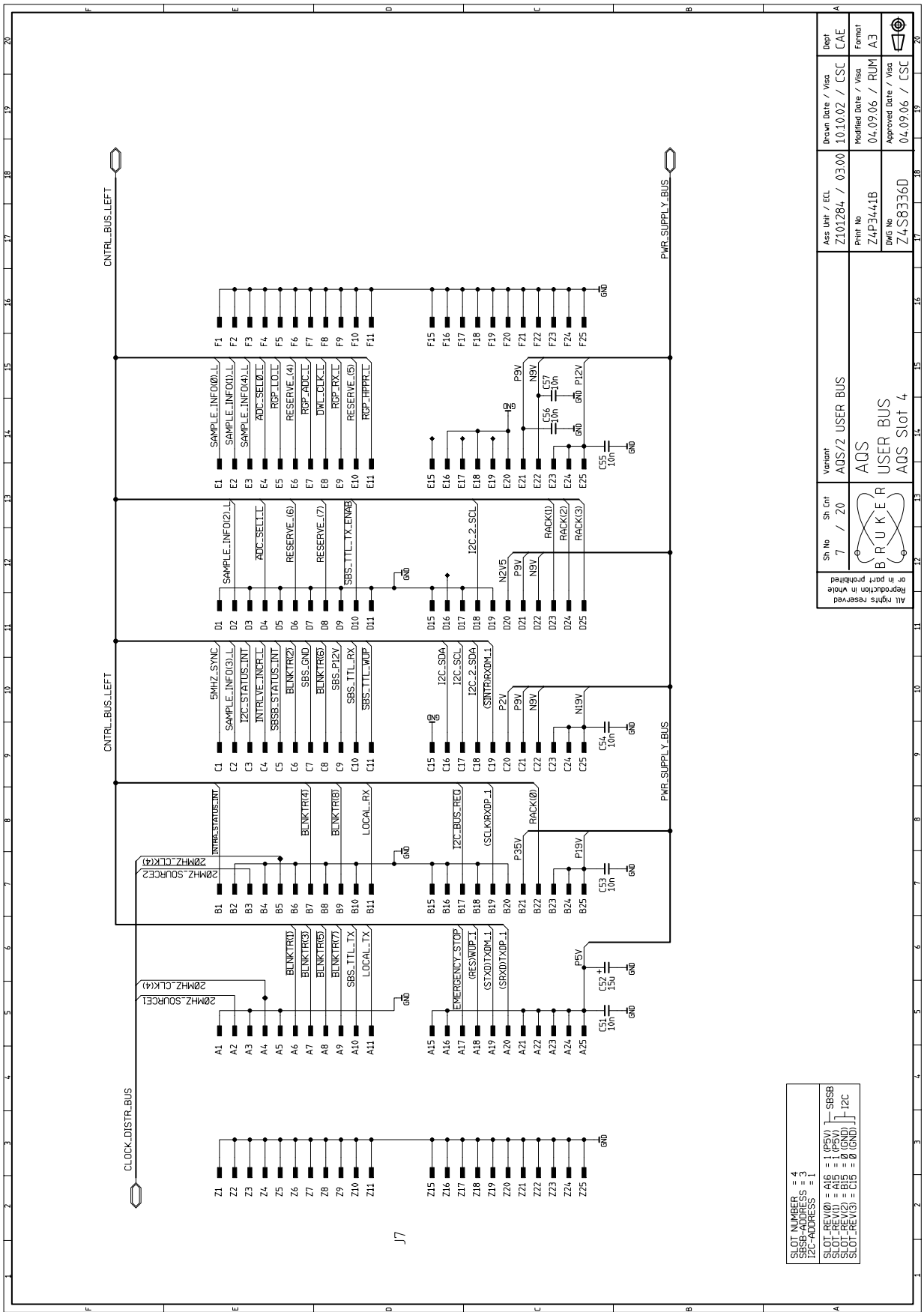


Figure 4.22. User Bus Slot 5

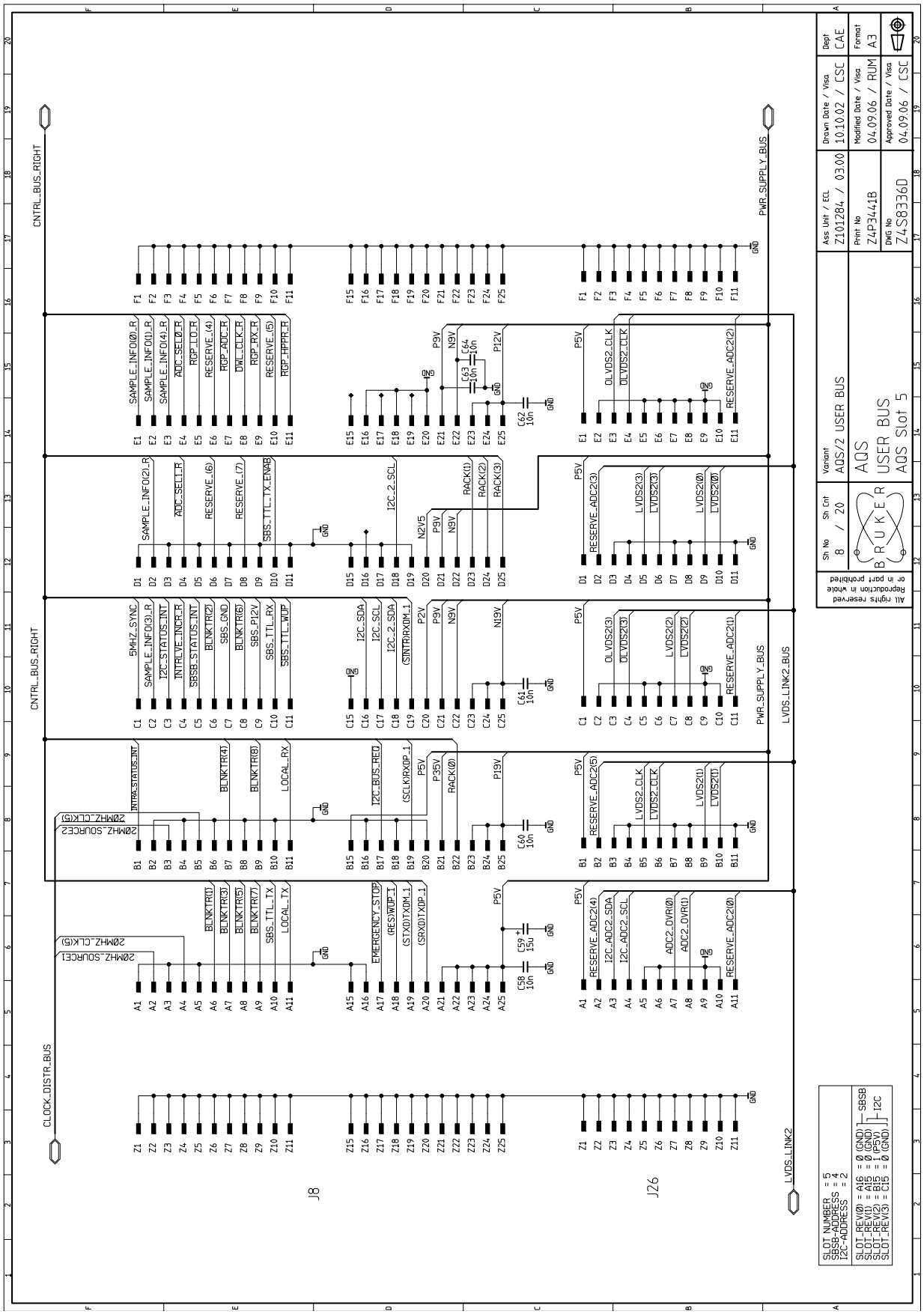


Figure 4.23. User Bus Slot 6

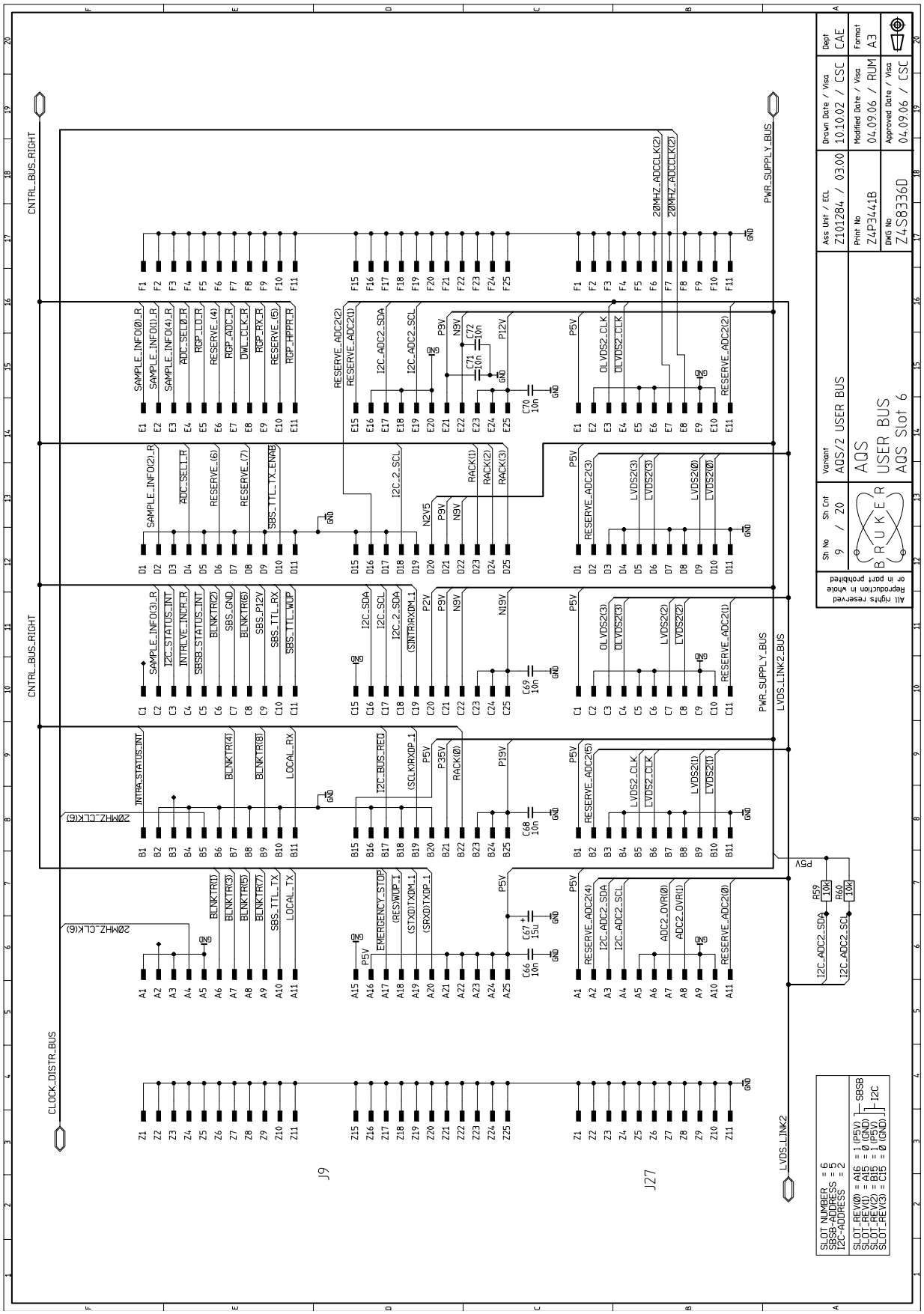


Figure 4.24. User Bus Slot 7

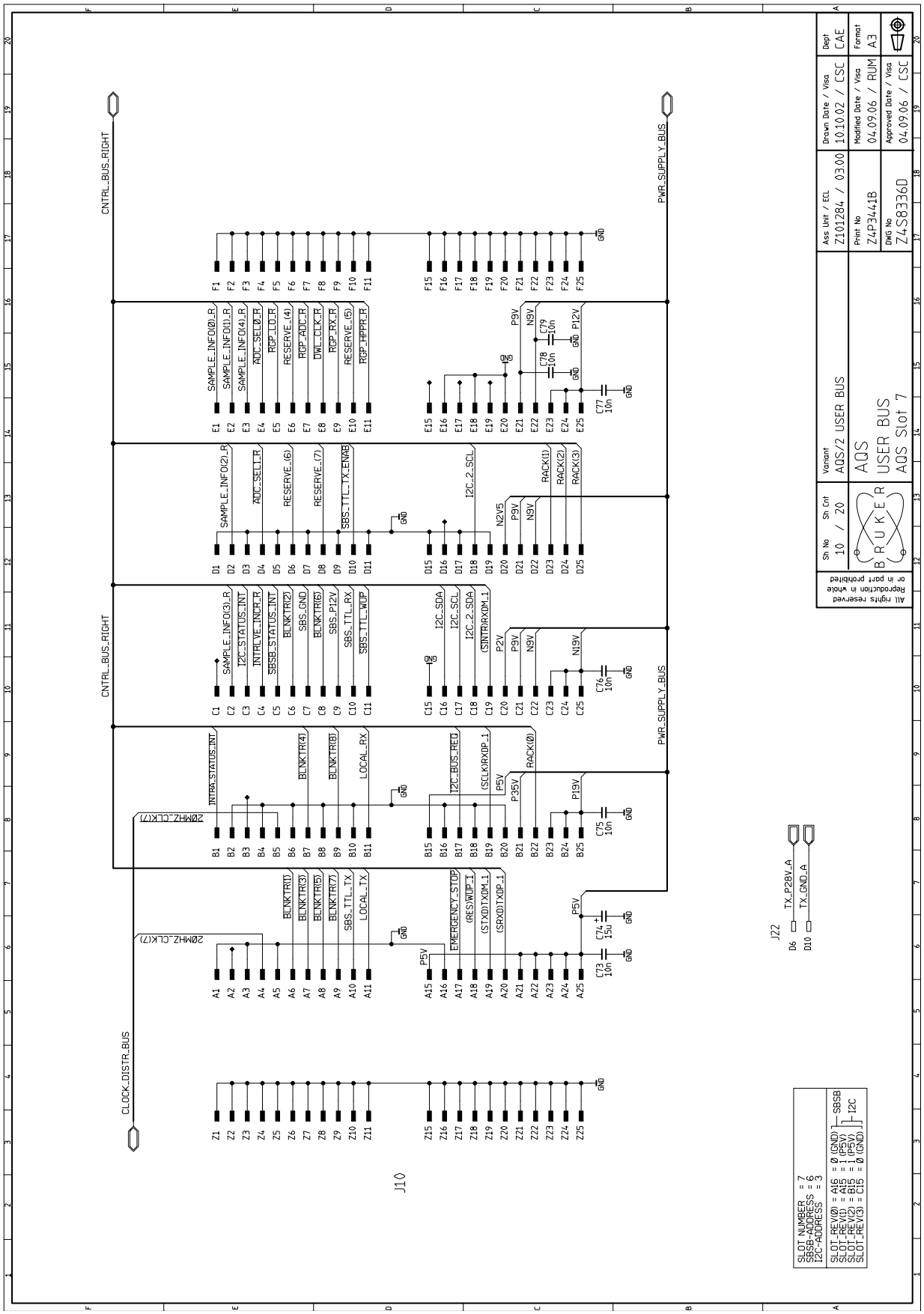


Figure 4.25. User Bus Slot 8

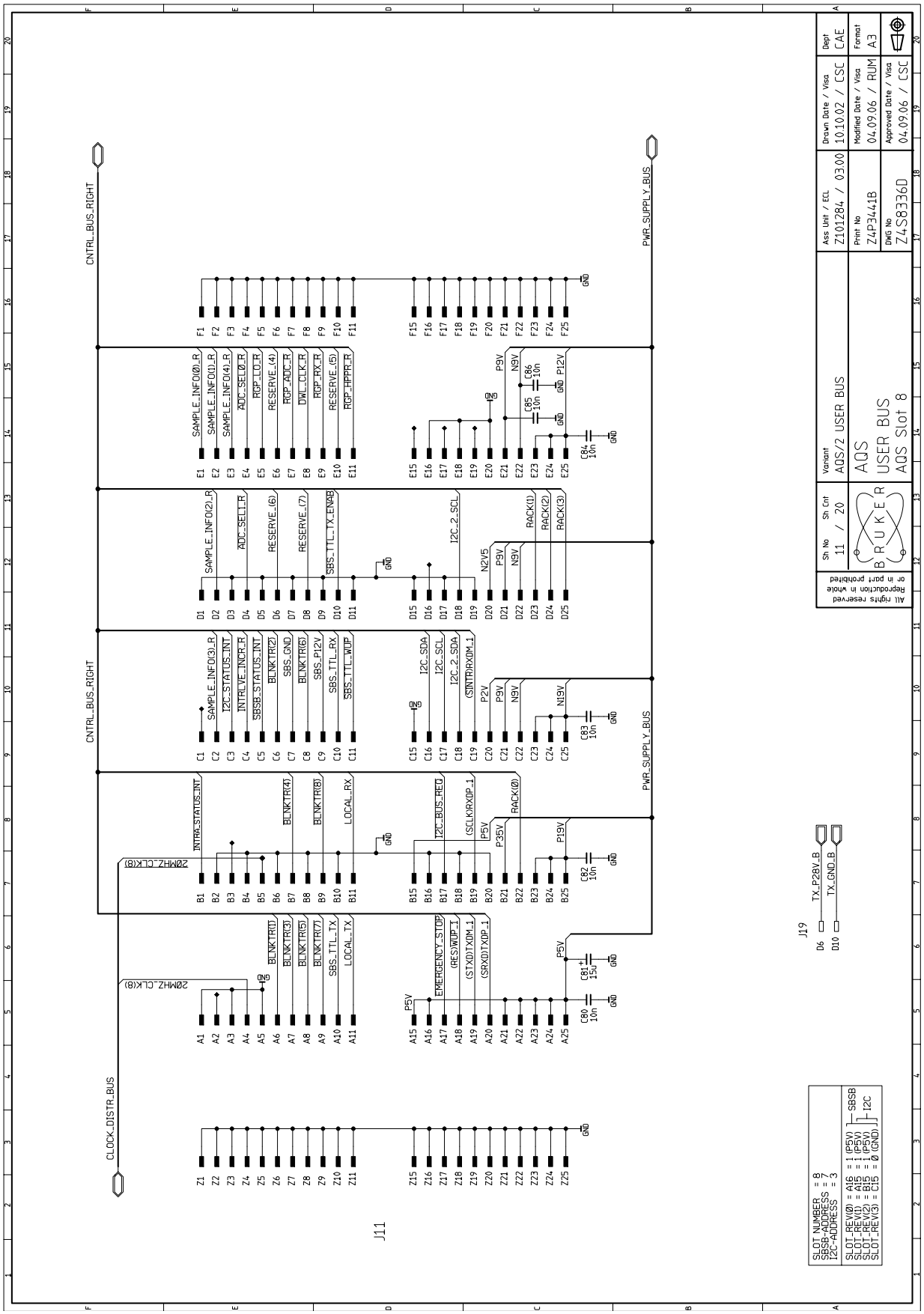


Figure 4.26. User Bus Slot 9

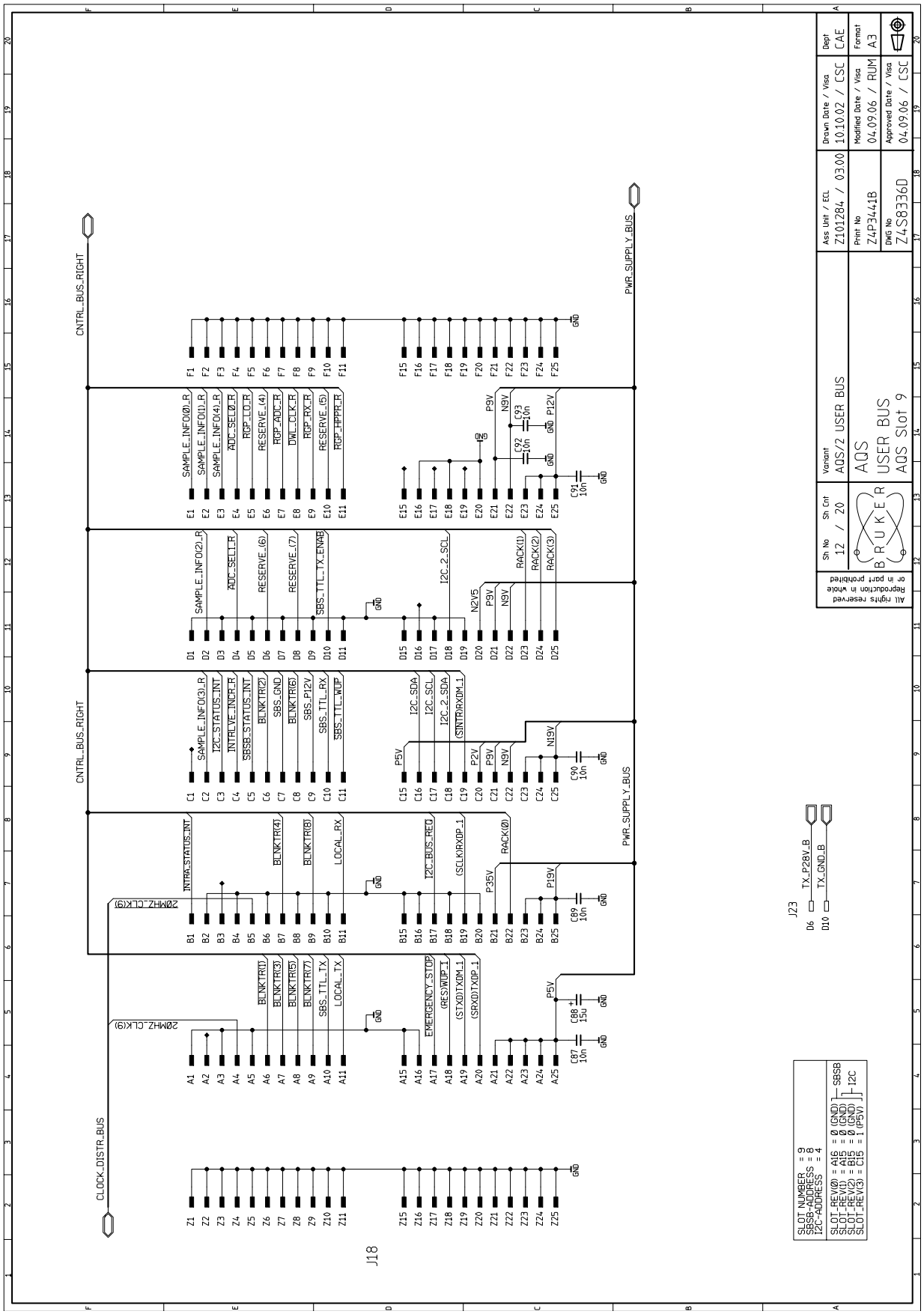


Figure 4.27. User Bus Slot 10

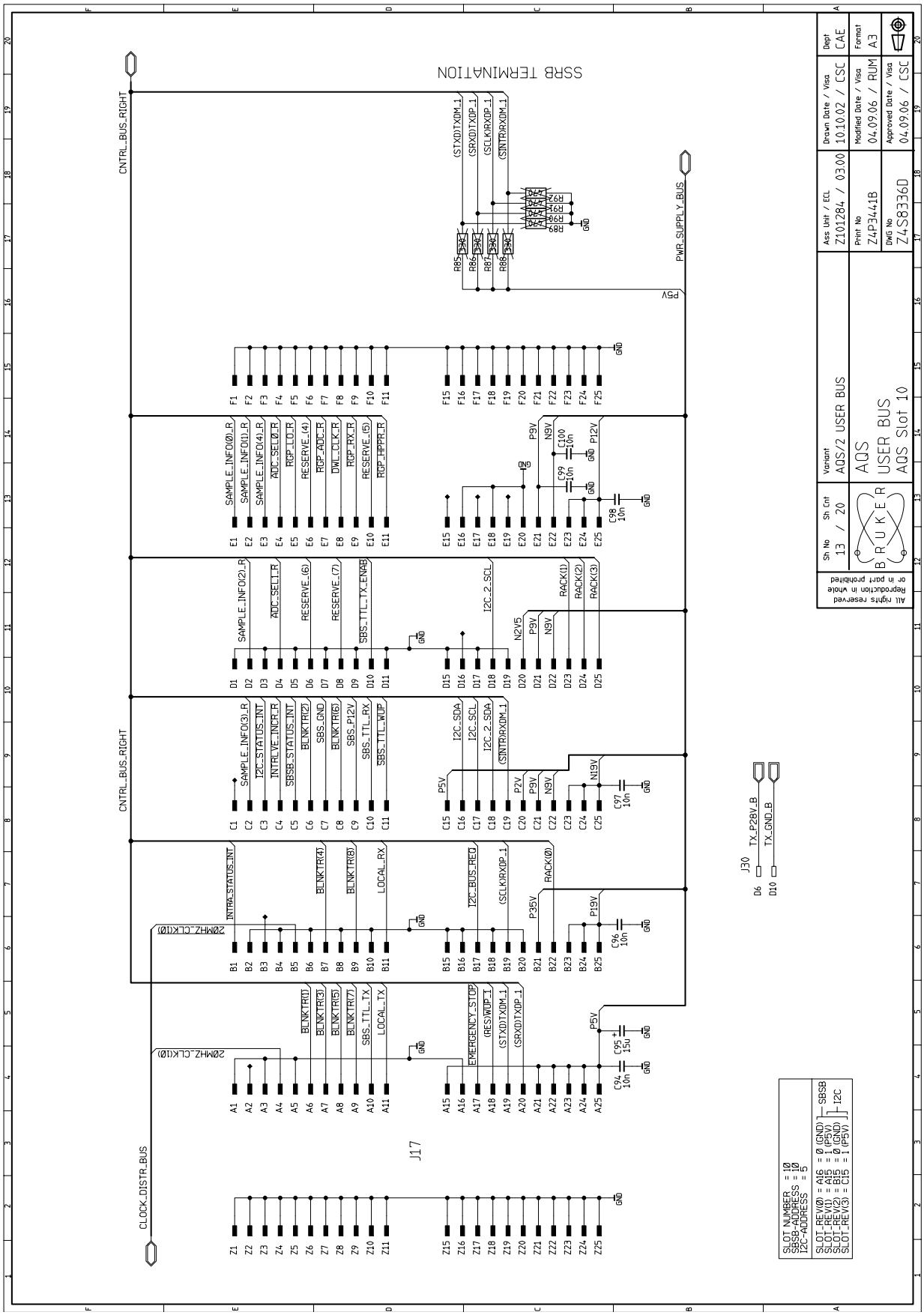


Figure 4.28. ACB Standard/ PSD Slot

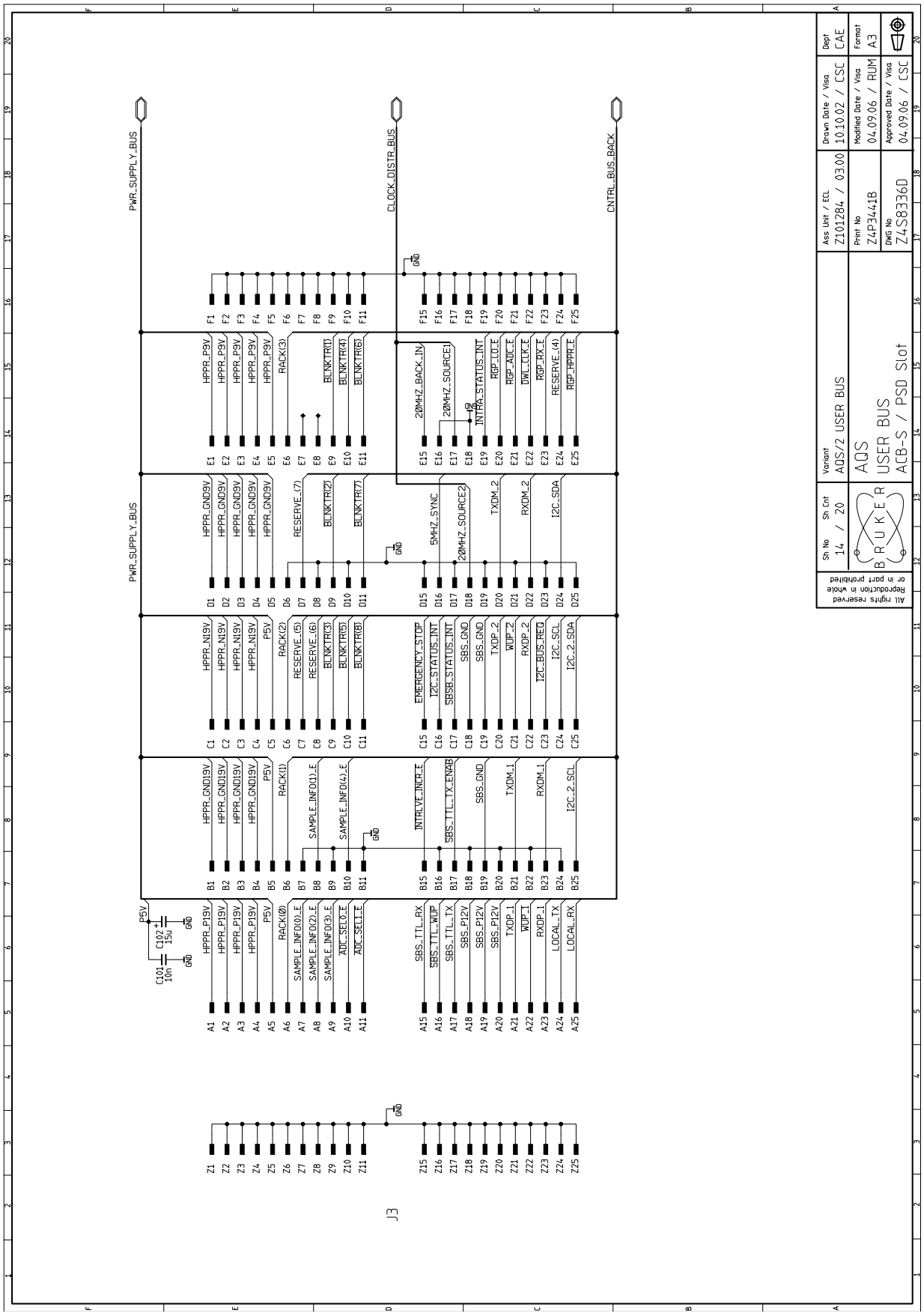


Figure 4.29. Power Supply Slot 1

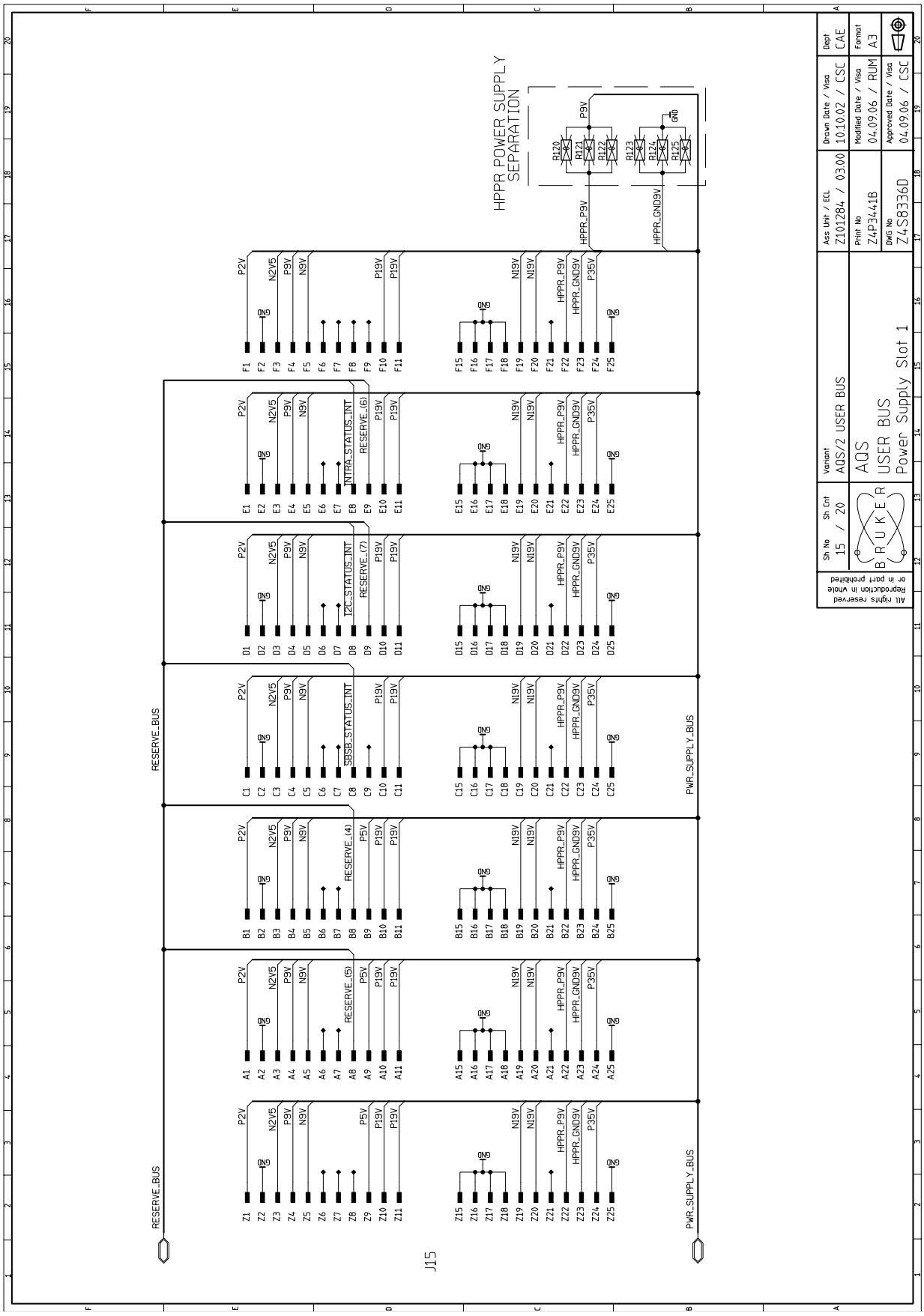


Figure 4.30. Power Supply Slot 2

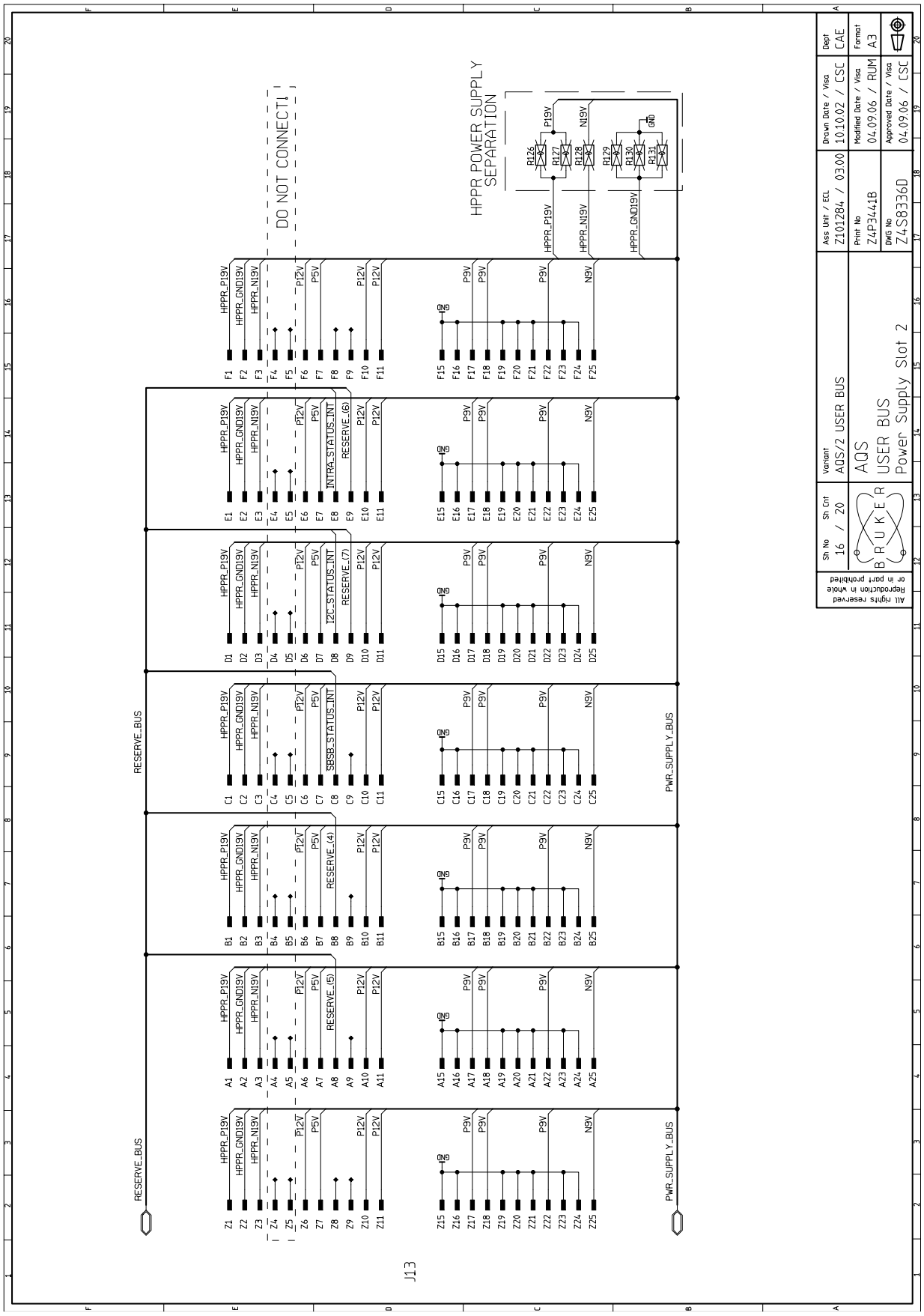


Figure 4.31. Power Supply Slot 3

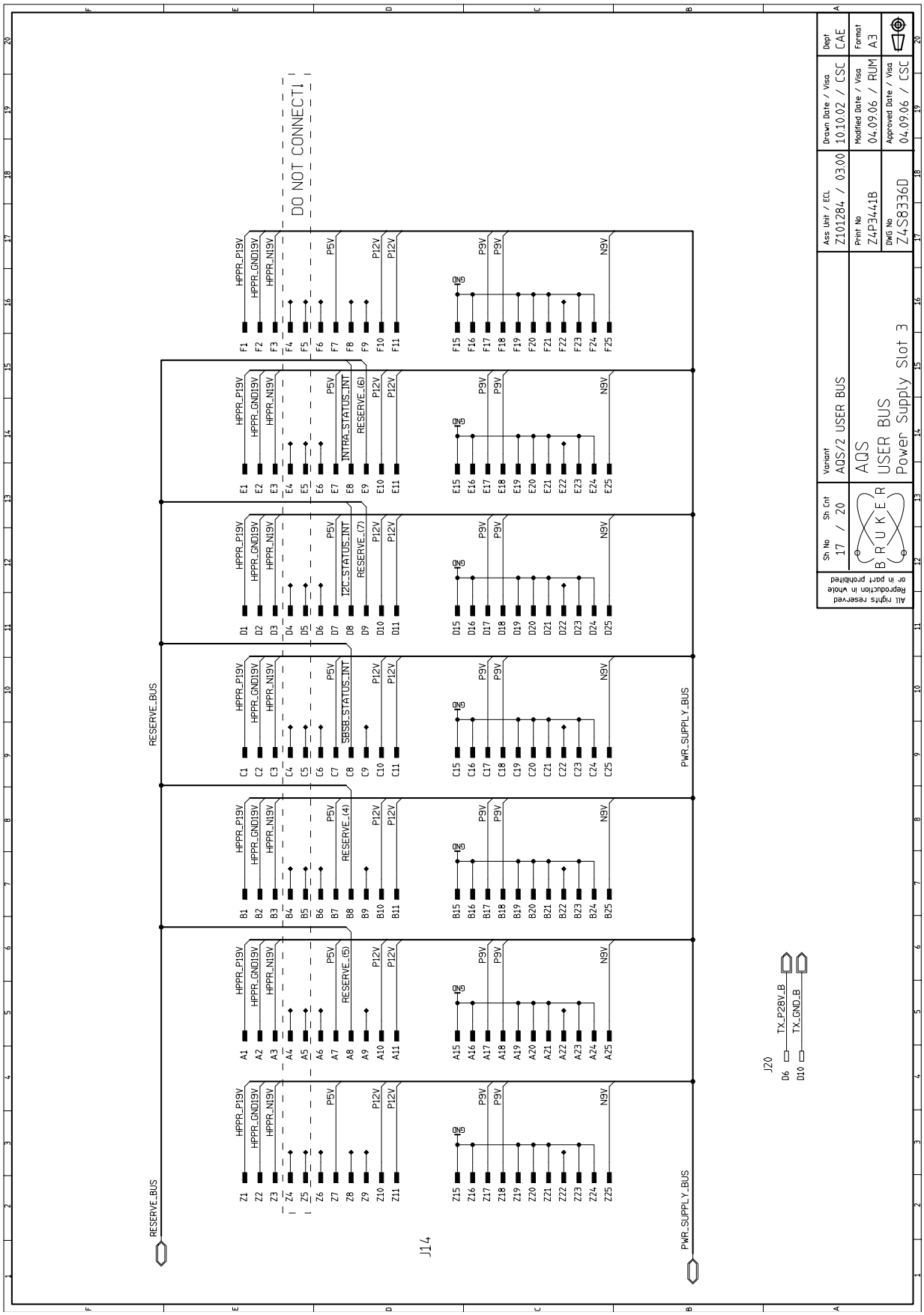


Figure 4.32. ACB Extended Slot

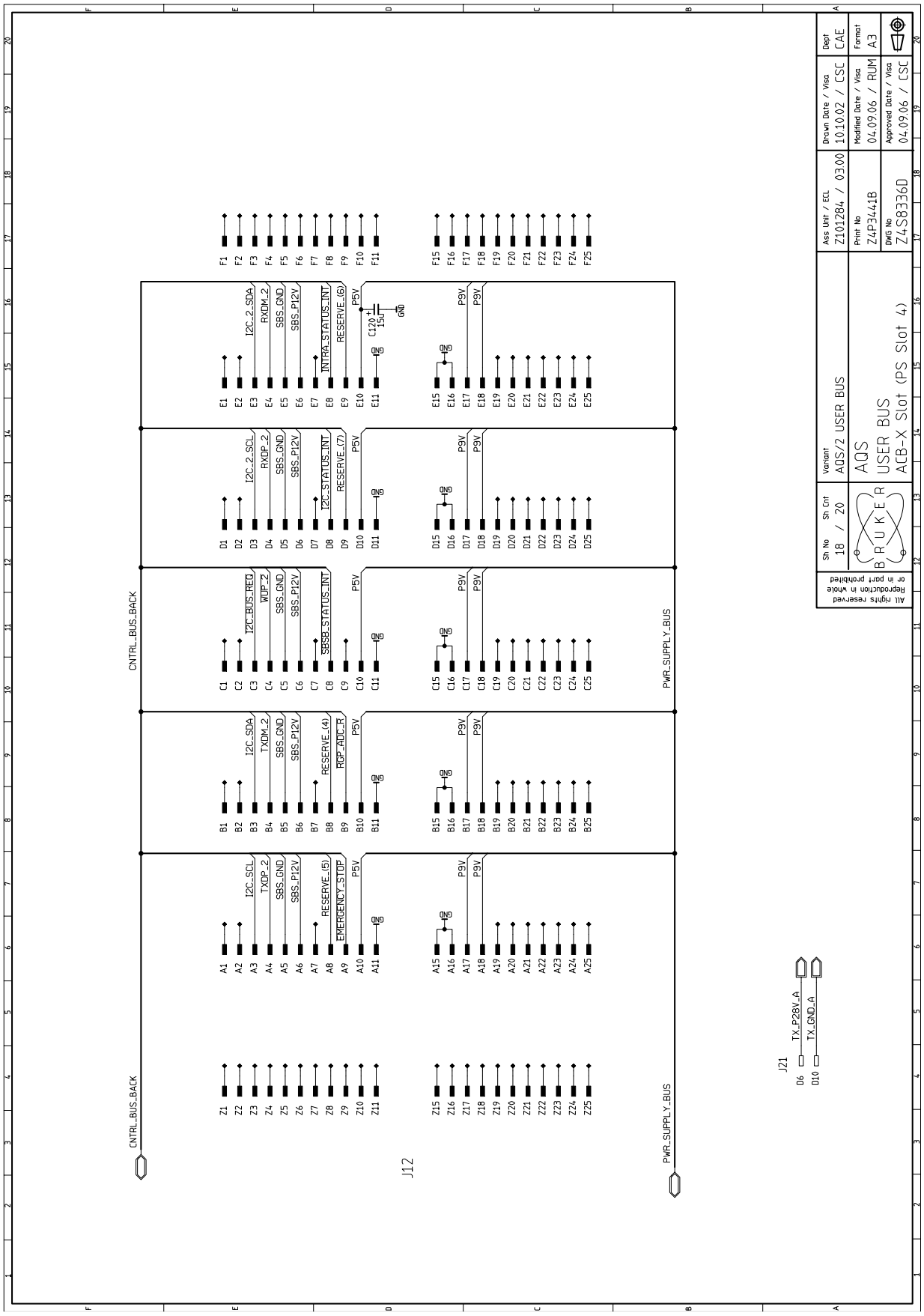
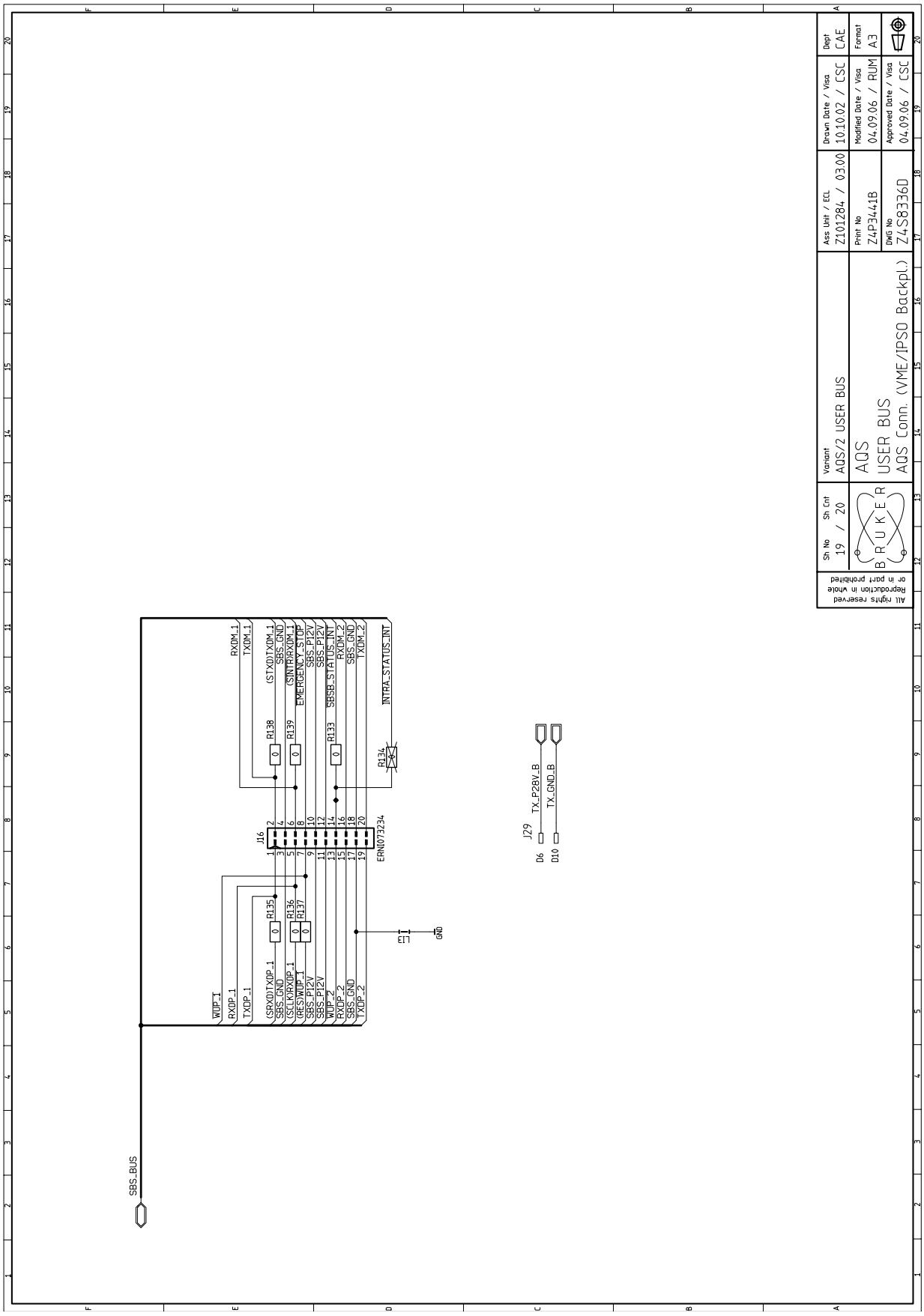
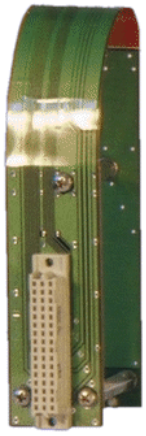


Figure 4.33. AQS Connector (to VME Backplane)

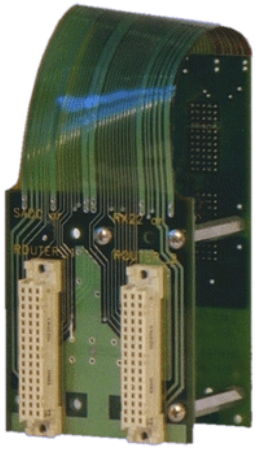


Adapters *4.14*

The adapters are necessary to install 3-Channel Router in the AQS/2.



Z003575
AQS ADAPTER ROUTER / RX22-BB



Z003349
AQS ADAPTER ROUTER DUAL

AQS/2-M Mainframe 5

Introduction 5.1

The AQS/2-M mainframe is a variant version of the AQS/2 mainframe. One chassis may contain up to 7 receiver channels. It has 14 aqs-slot on the user bus and no VME-bus.

The user bus is designed to be equipped with AQS RF receiver units (DRU and RXAD). For special configurations other units like SGU, Reference Board, 1-4 Router or AQS Preamp may be used. Units like 3-Channel Router, SADC, HADC/2, RX-22 Receiver or power amplifiers such as BLA2BB or 2H-TX cannot be used in this chassis.

On the rear side, linear power supply modules (PSM1 &PSM5) and the switched power supply (PS Digital) are placed. One slot (AUX2) is reserved for the AQS RF-SPLITTER board.

The transformer, which feeds the linear power supply modules, is part of the mainframe and is located on the rear side.

The mainframe is cooled with 8 fans, which are located in a fan tray on top of the mainframe. The fan tray is serviceable without removing the mainframe from the spectrometer cabinet. (see ***"Fan Tray Service Instructions" on page 105***)
The fan tray is the same as in the AQS/2 chassis.

Technical Data 5.2

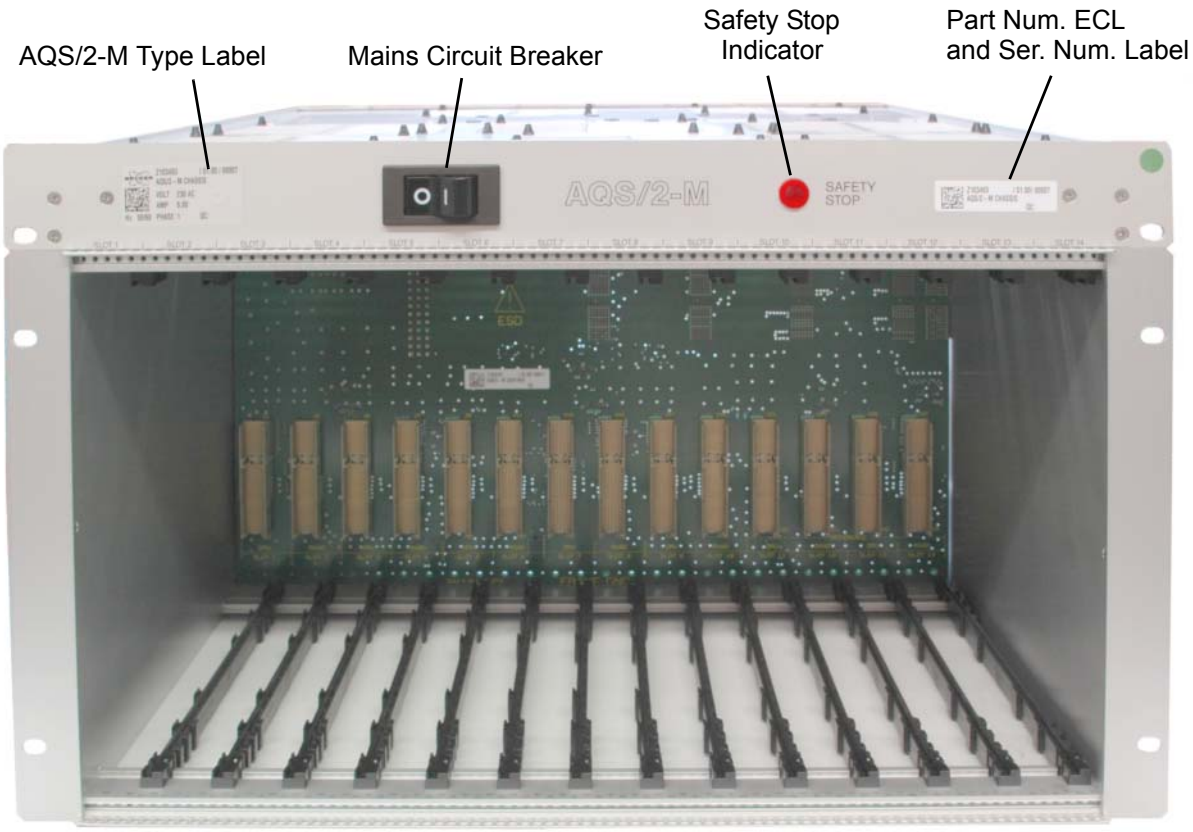
AC Input voltage (mains selector range)	195-215 / 210-230 / 220-245	Vrms
AC Frequency range	47..63	Hz
AC Input current	max. 8	Arms
AC Input inrush current	limited to approx. 20	Apk
AC Fuse (2pcs. 5x20mm, time-lag T, type H)	8A / 250V	
Dimensions (hight x width x depth)	310 x 483 x 570	mm
Weight (without units)	approx. 20	kg

Environmental conditions:

The AQS/2-M mainframe is designed as a subunit in the electronics cabinet of the spectrometer. For the environmental conditions outside the cabinet please refer to the site planning guide of the spectrometer system.

Front View *5.3*

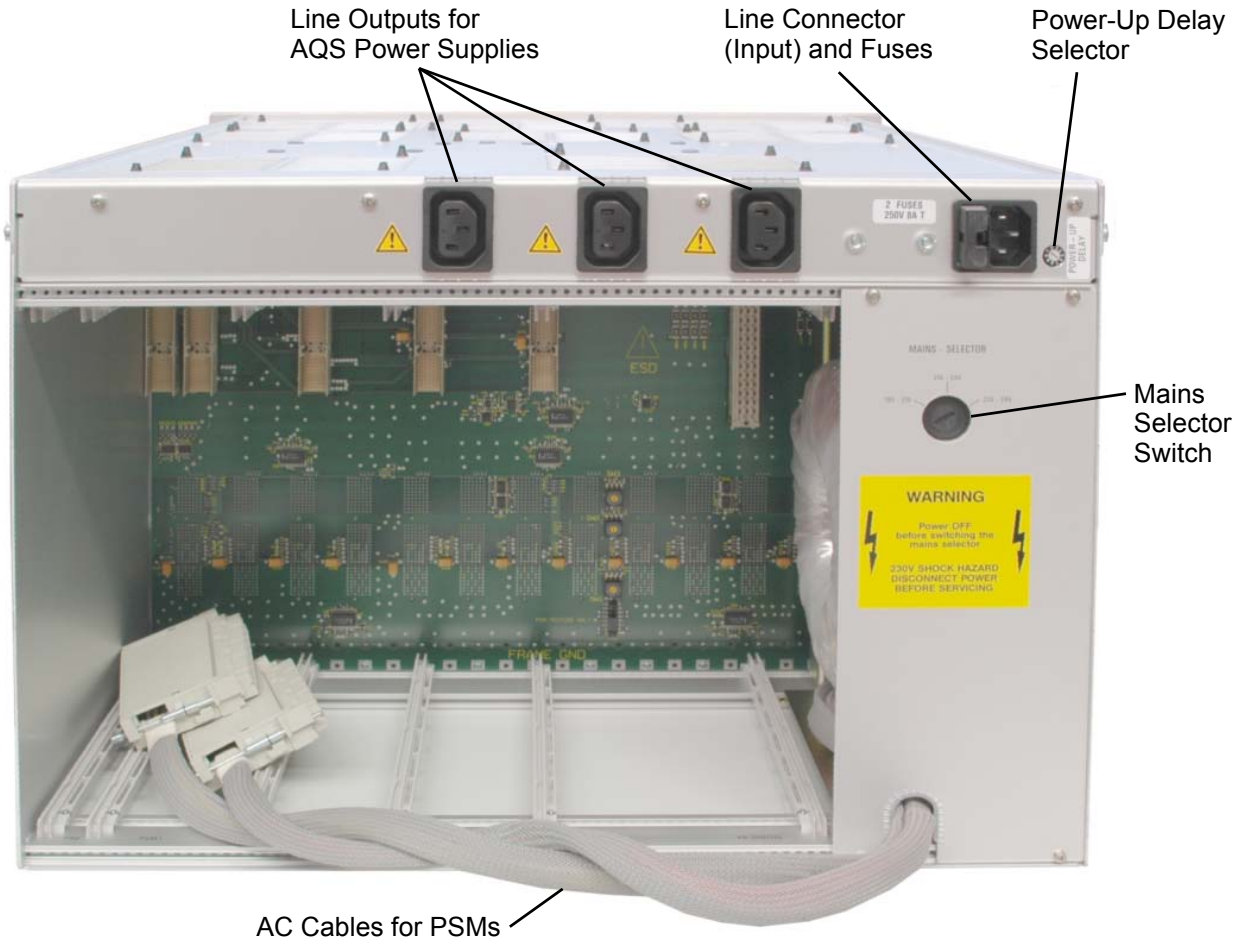
Figure 5.1. AQS/2-M Chassis front view



Rear View 5.4

The rear view shows the housing of the power supply boards. On the right hand side is the transformer housing with the appropriate AC cables.

Figure 5.2. AQS/2-M Chassis rear view



Line Outputs:

Only connect AQS POWER SUPPLY units to these connectors.

- AQS POWER SUPPLY DIGITAL 350W (H9489)
- AQS PSM5 POWER SUPPLY MODULE (Z102023)
- AQS PSM HPLNA (Z104783)

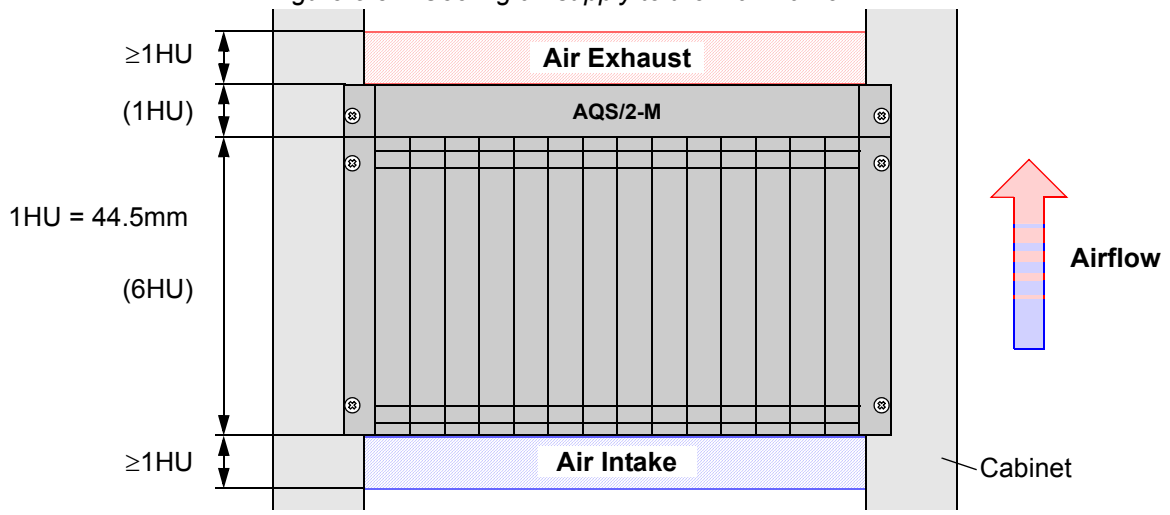
Installation in electronics cabinet 5.5

The AQS/2-M mainframe must be installed at it's designated position in the electronics cabinet to ensure proper air ventilation for the cooling fans. The position may vary in different cabinet types and sizes.

! ***At least one height unit (1HU) above and below the mainframe must be reserved for the cooling air supply.***

Special air baffle plates may be used to support efficient ventilation. Typically the air intake is from the front and the exhaust towards the back of the cabinet.

Figure 5.3. Cooling air supply to the mainframe



The mainframe must be fixed by at least 4 screws into the cabinet. The power cable is included in the cabinet wiring.

Preparation for Use 5.6

Prior to the first power-up of the AQS/2-M mainframe, it must be ensured that the mains selection switch is in the correct position. (see selector on the back side of the AQS/2-M)

The size of the linear power supply modules are designed for minimal power dissipation; therefore the transformer input voltage should be matched to the mains voltage at the installation site.

Generally, the mains selection switch should be set to the corresponding voltage range, even if the mains power is weak (max. fluctuations ± 6%).

- Factory setting for 230V mains supply = 220-245V

Selector Setting for combined Voltages 5.6.1

In countries with 110-120V mains supply such as USA and Canada combined line voltages may be used. In this case set the selector switch to 195-215V.

AC Power Line Fuses 5.7

The AQS/2-M is protected by two fuses as specified on the power supply nameplate. The fuses are located in a removable fuse holder next to the AC power connector. Always use time-lag T fuse types with high breaking capacity H.

Power-Up Delay 5.8

The power-up delay can be selected with a rotary switch next to the power connector at the back of the mainframe. Please set the switch according to your configuration as described in the configurations section within this manual. The minimal power-up delay is 0.5s due to the inrush current limiter circuit.

Table 5.1. Power-Up Delay

Setting	Delay
0	0.5 s
1	2 s
2	4 s
3	6 s

Setting	Delay
4	8 s
5	10 s
6	12 s

Setting	Delay
7	14 s
8	16 s
9	18 s

Inrush Current Limiter 5.9

The mainframe is equipped with an inrush current limiter which limits the peak current to approx. 20A. The limiter is always active, even after a „hot start“ when the chassis is switched OFF and ON within a short timespan.

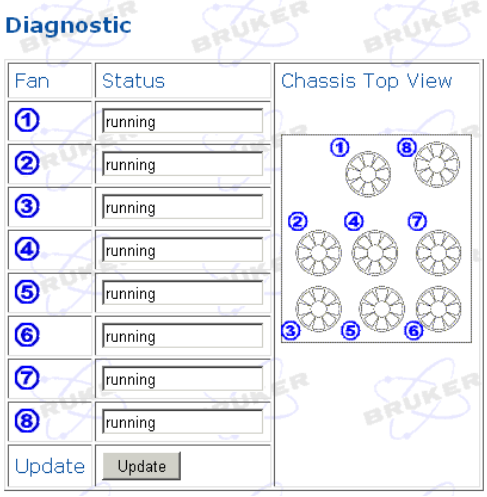
AC Power Loss 5.10

In the event of an AC power loss in the spectrometer cabinet, the chassis turns itself of and restarts automatically when the power is restored. To prevent a short time power loss an external UPS (uninterruptible power supply) must be used.

Fan Control *5.11*

The operation of all fans is individually controlled by the AQS controller and the control circuit on the AQS/2-M user bus. The fan status can be checked via the AQS chassis page in the DRU service web.

Figure 5.4. DRU Service Web: AQS Chassis Diagnostic



Safety Stop *5.12*

If the temperature inside the mainframe exceeds the absolute maximum limit of save operation, the mains supply to the chassis is switched off automatically (and without warning) to prevent permanent damage to the AQS units. This „Safety Stop“ condition is indicated with a red lamp on the front panel as long as the mains supply is present at the power connector.

! ***Make sure to establish and remove the cause of the Safety Stop condition before you use the spectrometer again.***

The Safety Stop can be caused by a fan or power supply failure within the mainframe. Other causes can be inefficient cooling air supply to the mainframe or exceeding ambient air temperatures within or around the spectrometer cabinet.

Please contact Bruker service personnel if you cannot establish the cause of the failure.

The chassis can be returned to its normal working state by switching the mains circuit breaker manually OFF and ON. An AC power loss also resets the chassis to its working state (see ***"AC Power Loss"***).

Figure 5.5. Safety Stop State Diagram

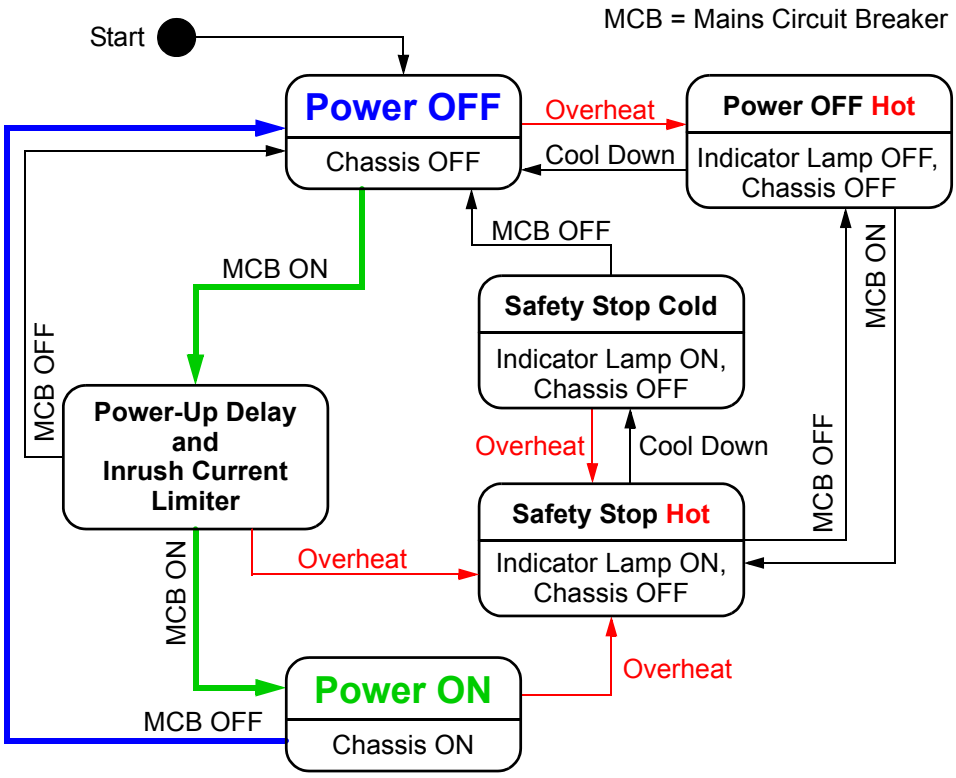


Figure 5.6. AQS/2-M AC Wiring

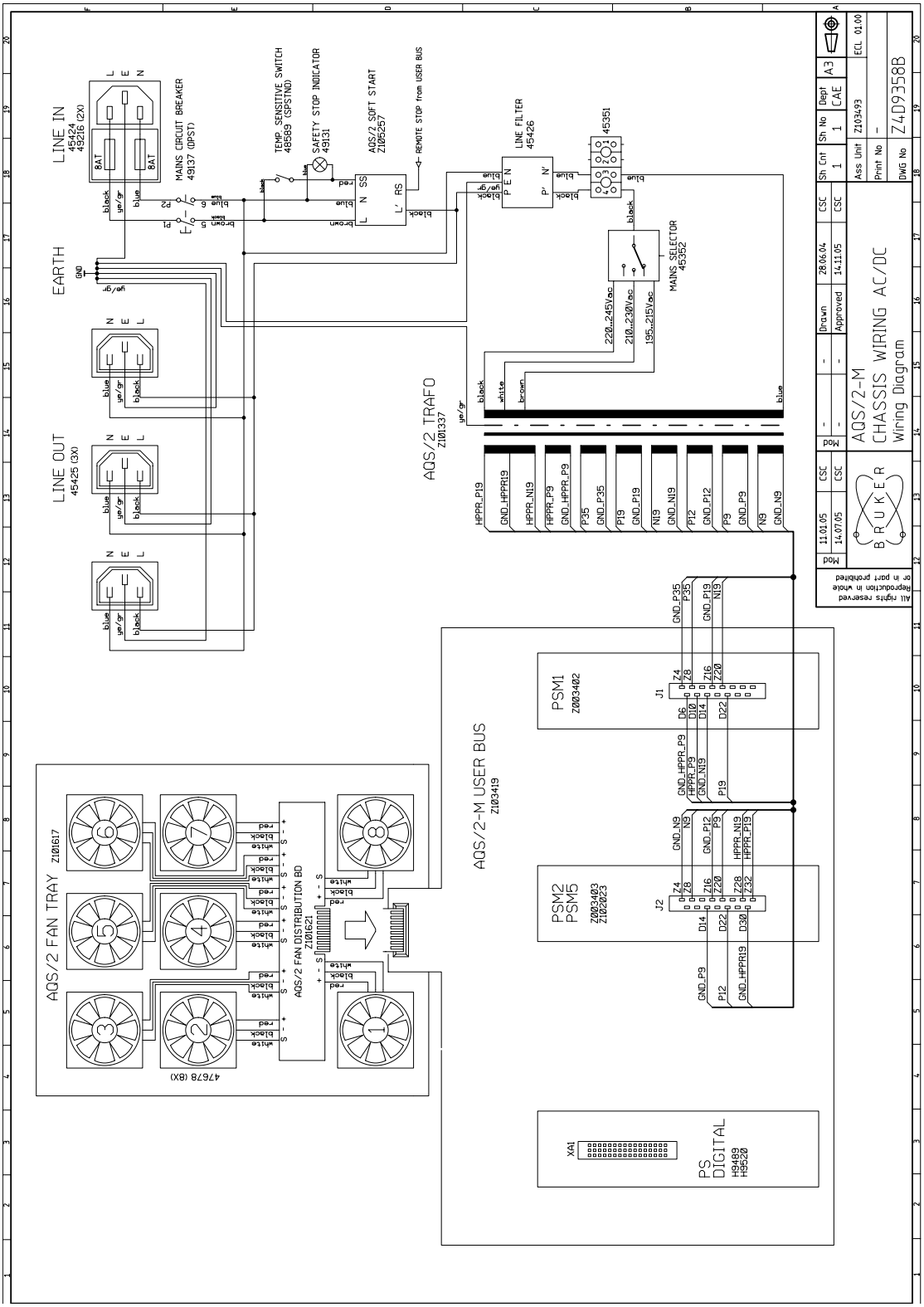
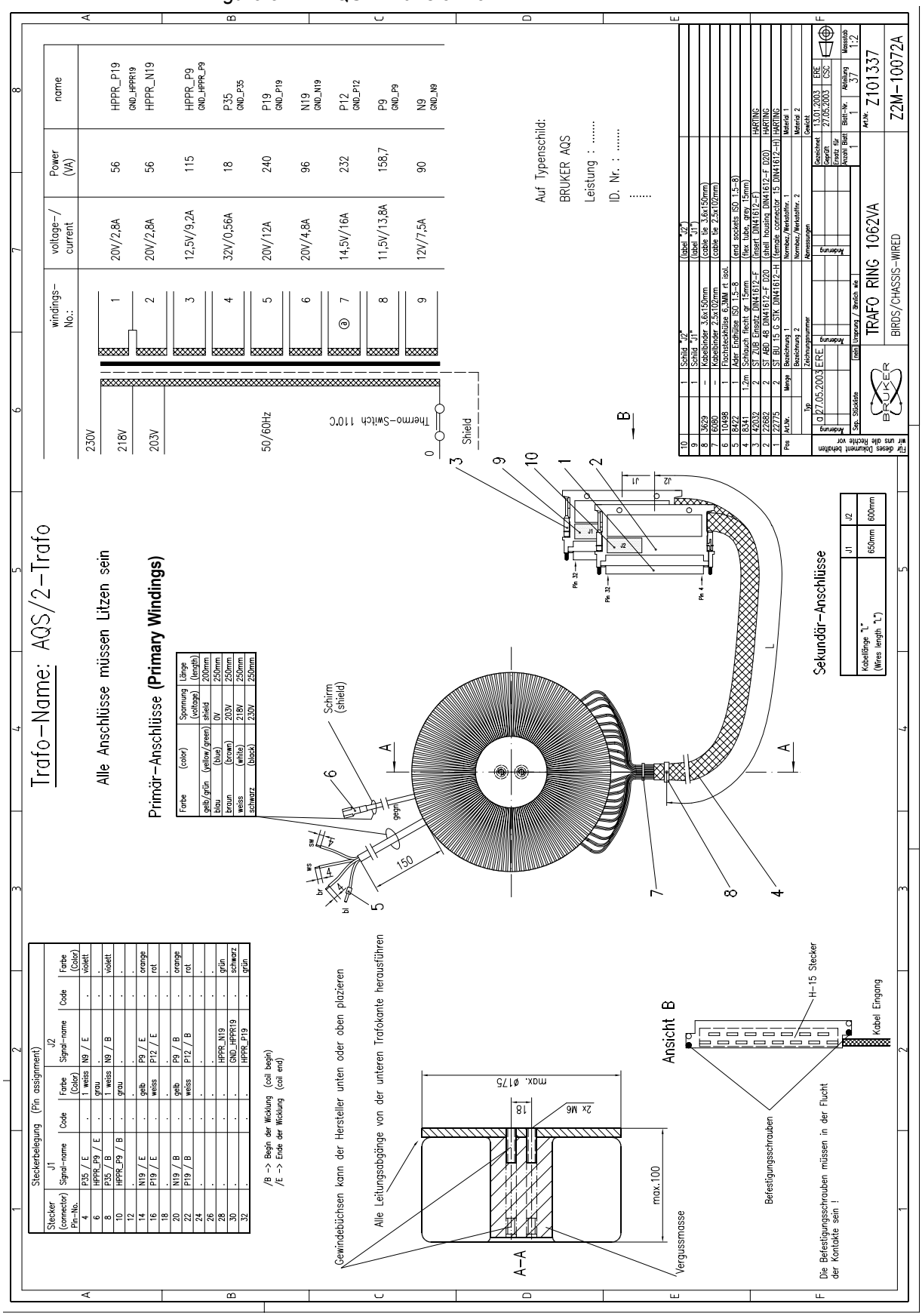


Figure 5.7. AQS/2 Transformer



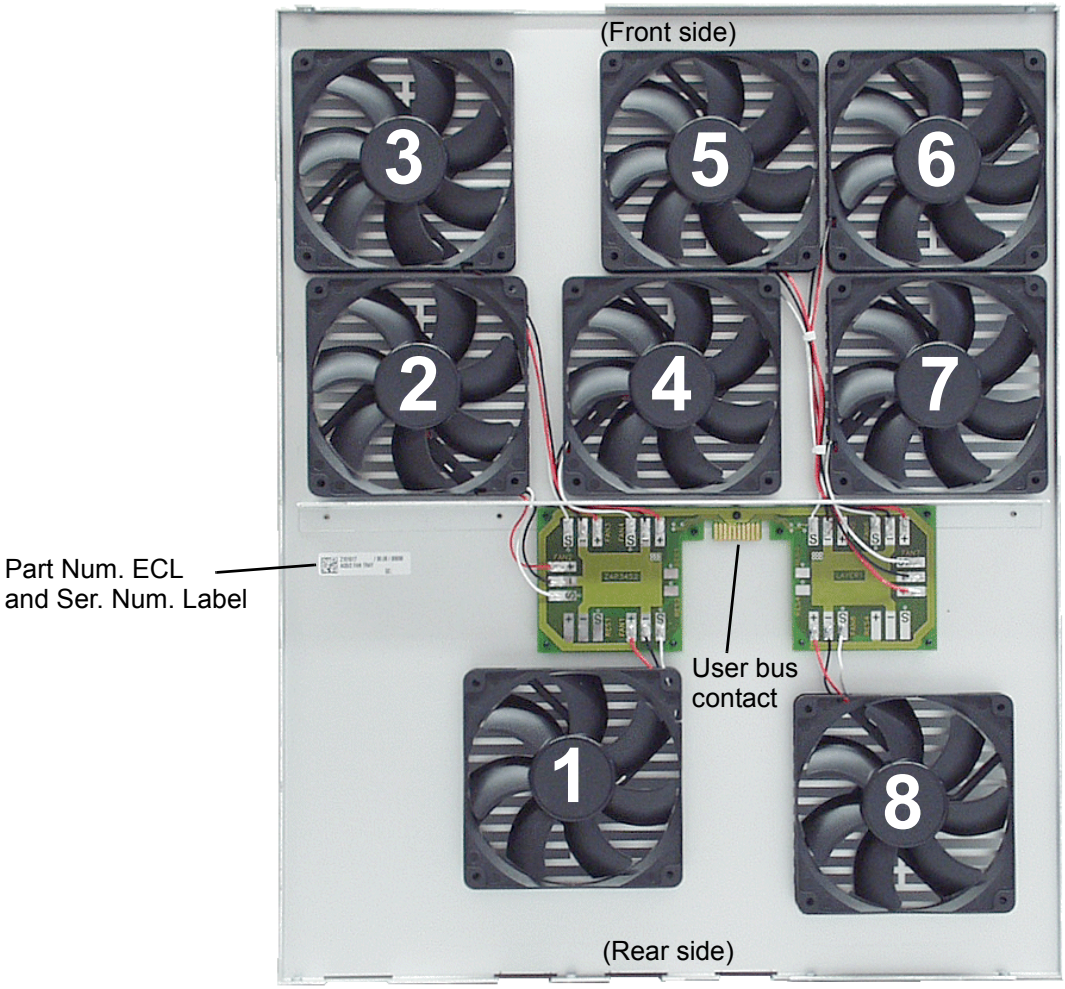
Fans *5.14*

The fans are located in the fan tray on top of the mainframe. They are supplied and controlled via the AQS/2-M user bus.

The fan tray is serviceable without removing the mainframe from the spectrometer cabinet. (see ***"Fan Tray Service Instructions" on page 105***)

! ***Only use AQS/2 FAN TRAY (Z101617) with ECL02 or higher as a replacement.***

Figure 5.8. AQS/2 Fan Tray (Bottom view)



Fan Tray Service Instructions 5.15

! ***Only qualified Bruker personnel are allowed to service the AQS/2-M mainframe.***

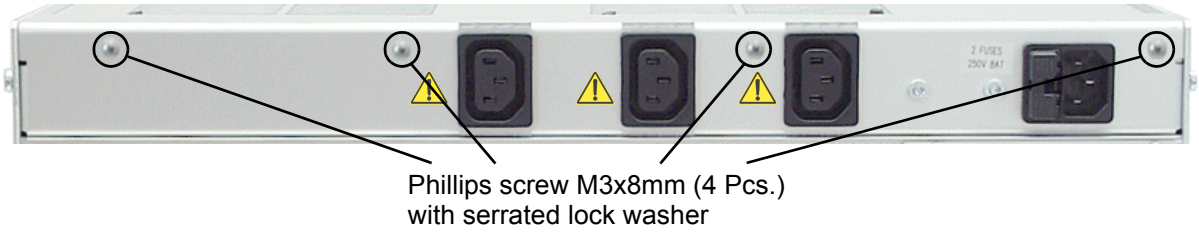
The fan tray removal and reassembly is the same as in the AQS/2 chassis. Please do not be confused if the pictures of the AQS/2 chassis are used in the following instructions.

Fan Tray removal 5.15.1

To remove the fan tray from the AQS/2-M mainframe please follow the steps exactly as described below:

1. Turn of chassis with mains circuit breaker
2. Remove AC power line (rear side)
3. Remove 4 screws on the rear side

Figure 5.9. Fan Tray screws rear side

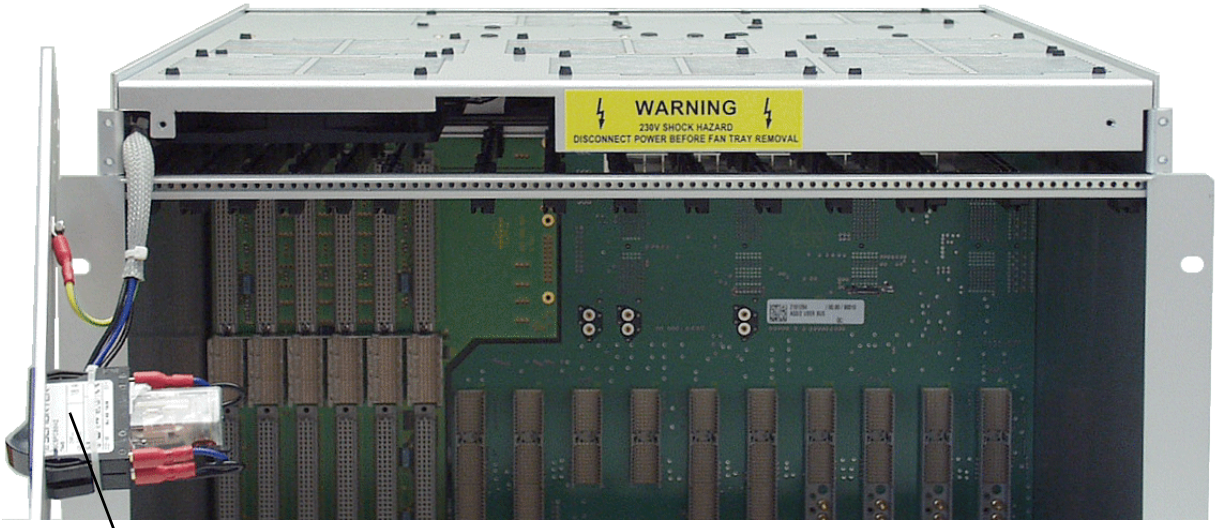


4. Remove 6 screws on the front side

Figure 5.10. Fan Tray screws front side

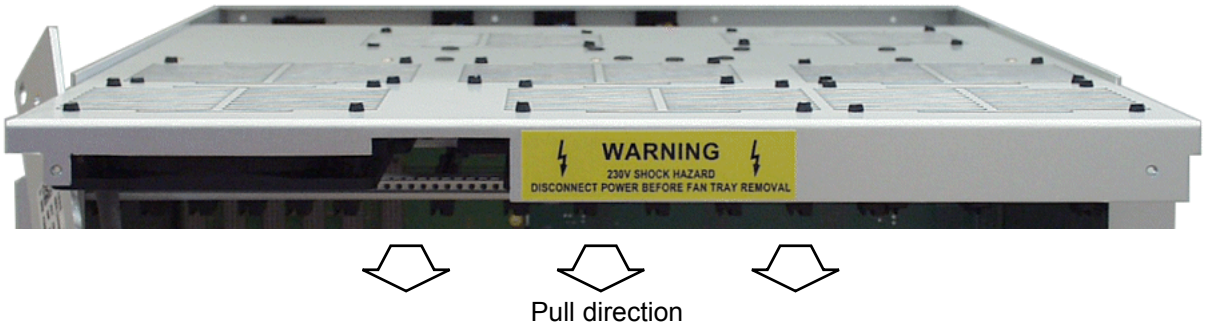
5. Carefully pull the front panel away from the mainframe and place it towards the left side (dangling from the cable)

Figure 5.11. Front panel removal



6. Remove the fan tray by pulling it gently towards the front

Figure 5.12. Fan Tray removal



Fan Tray reassembly *5.15.2*

To replace the fan tray in the AQS/2-M mainframe follow the steps as described above in ***reverse order***.

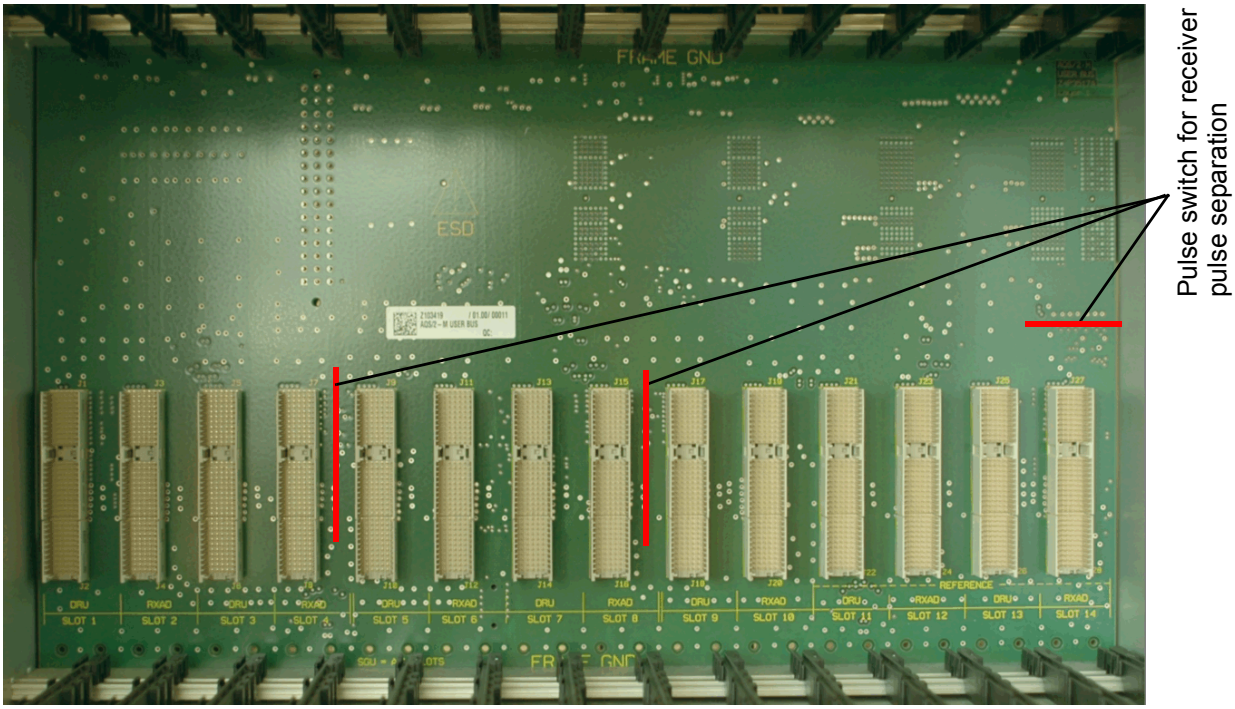
Make sure that:

- the fan tray sits flat on the guide rails on either side of the mainframe before final insertion
- no wires are squeezed in between the front panel and the fan tray
- all screws are secured and fastened properly (rear side screws with serrated lock washers)
- all fans turn freely after power up

Backplane (User Bus) 5.16

The user bus is designed to route all specific signals and power supplies to the specific boards. It represents the ground point of the AQS/2-M and is connected to the chassis frame. For detailed information about user bus signals see ***"AQS signal path" on page 13***, ***"Synchronous signals" on page 17*** and ***"20MHz Clock Distribution" on page 23***

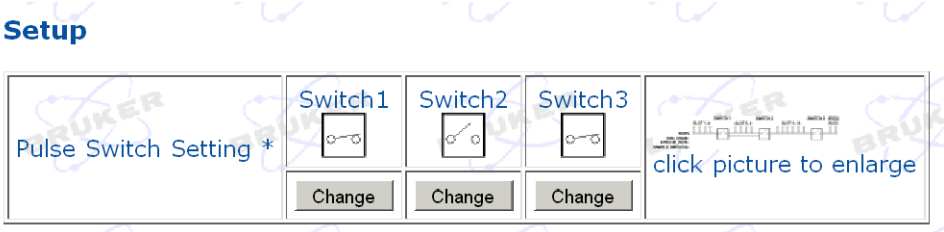
Figure 5.13. AQS/2-M User Bus (front view)



Pulse switch for receiver pulse separation 5.16.1

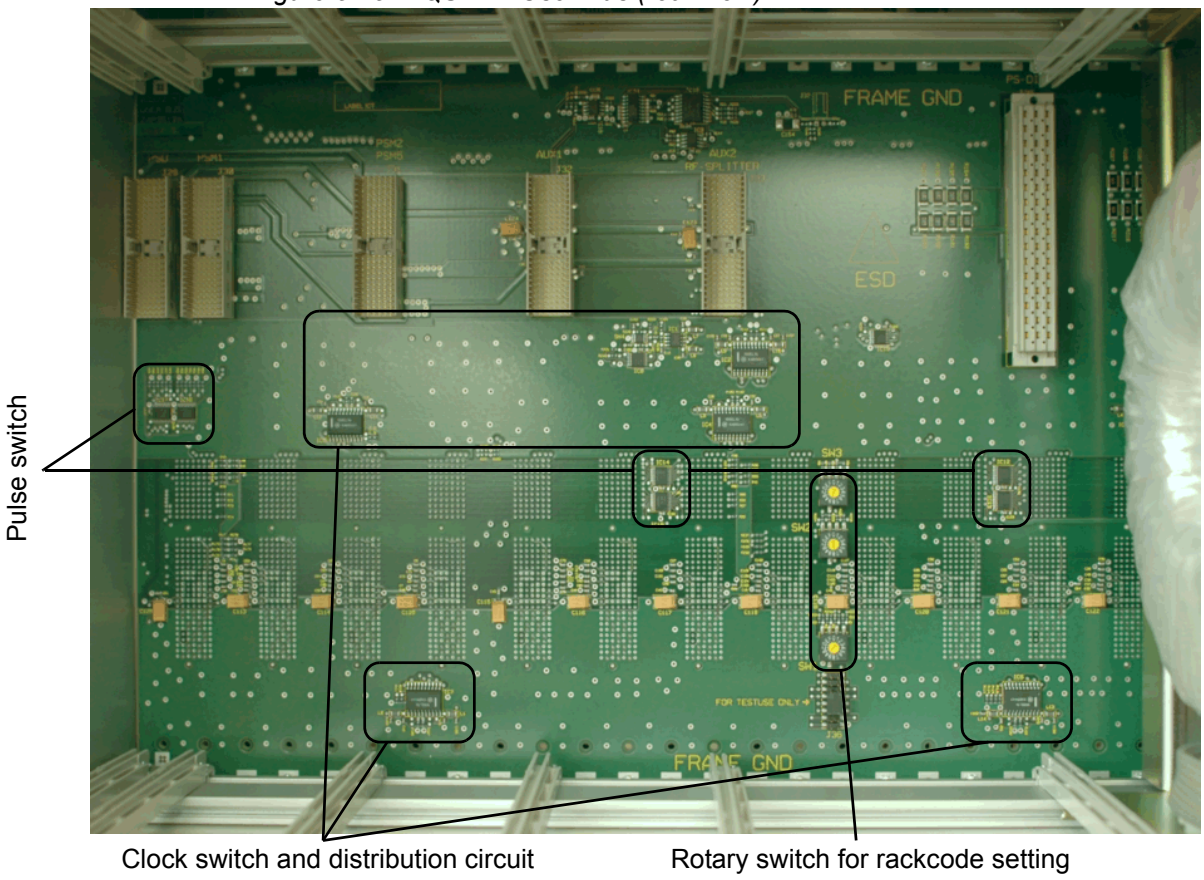
The user bus is equipped with three pulse switches. One is located between slots 4 and 5, another between slots 8 and 9 and the last between slot 14 and the PSD slot. All switches are either controlled via the AQS controller or with a rotary switch (SW2) on the rear side of the user bus. The switch status can be checked and set via the AQS chassis page in the DRU service web.

Figure 5.14. DRU Service Web: AQS Chassis Setup



For a detailed description of the SW2 switch functions see ***"Rackcode Switch Function" on page 108***.

Figure 5.15. AQS/2-M User Bus (rear view)



Rackcode Settings *5.16.2*

The rackcode must be set according to the chassis configuration as described in the configurations section of this manual.

Table 5.2. Rackcode Switch Function

Switch [a,b]	Function	Setting							
SW3	Chassis Number	**Chassis Number - 1**							
SW2	Clk Source BACK = RF-Splitter Clk Source FRONT = REF-Board	**0** 8	1 9	2 A	3 B	4 C	5 D	6 E	7 F
	Pulse Switch 1 = Slot 4 // 5 [c] Pulse Switch 2 = Slot 8 // 9 Pulse Switch 3 = Slot 14 // PSD	O O O	X O O	O X O	X X O	O O X	X O X	O X X	X X X
SW1	AQS Controller	**2** = DRU in Slot 1							

a Only chassis with ECL01 or higher have rotary switch. ECL00 uses jumpers.

b Example setting: Rackcode 0x102 = Chassis no. is 2, clock source is RF-Splitter, all pulse switches are remote controlled and the DRU in Slot 1 is AQS controller.

c O = open or remote controlled, X = permanently closed

User Bus Schematics *5.16.3*

Figure 5.16. User Bus Block Diagram

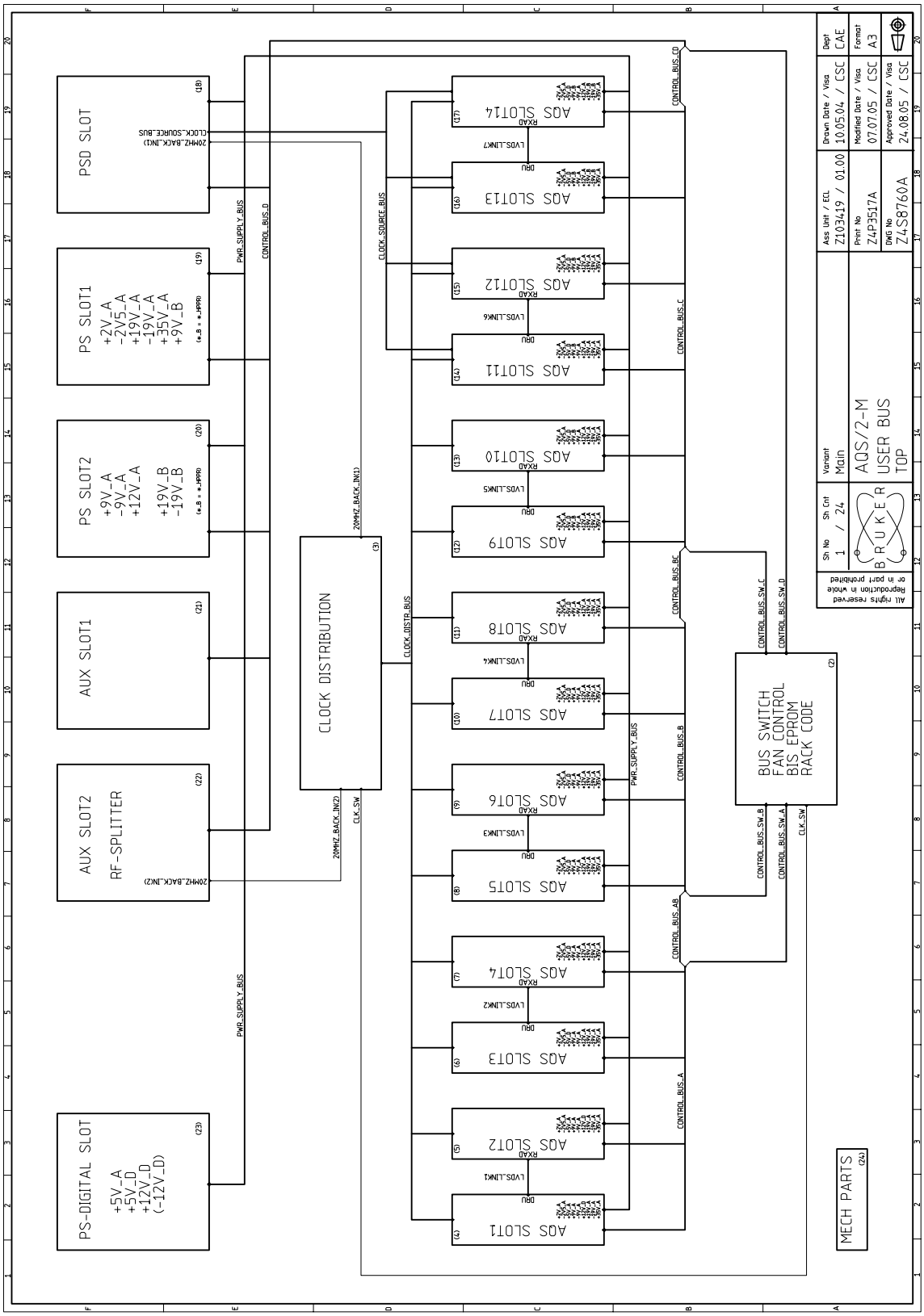


Figure 5.17. Pulse Switch, Fan Control & Rackcode

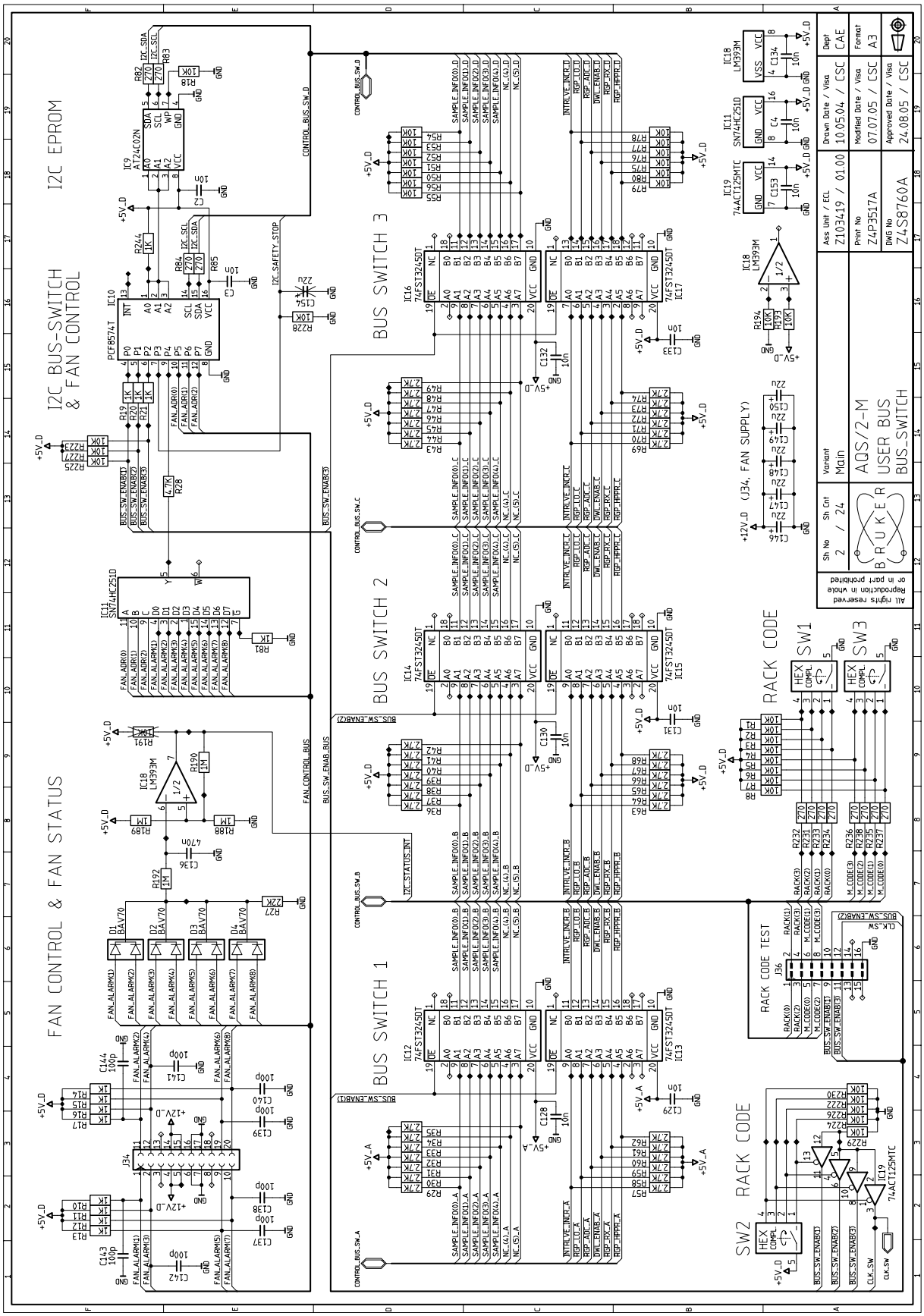


Figure 5.18. Clock Distribution

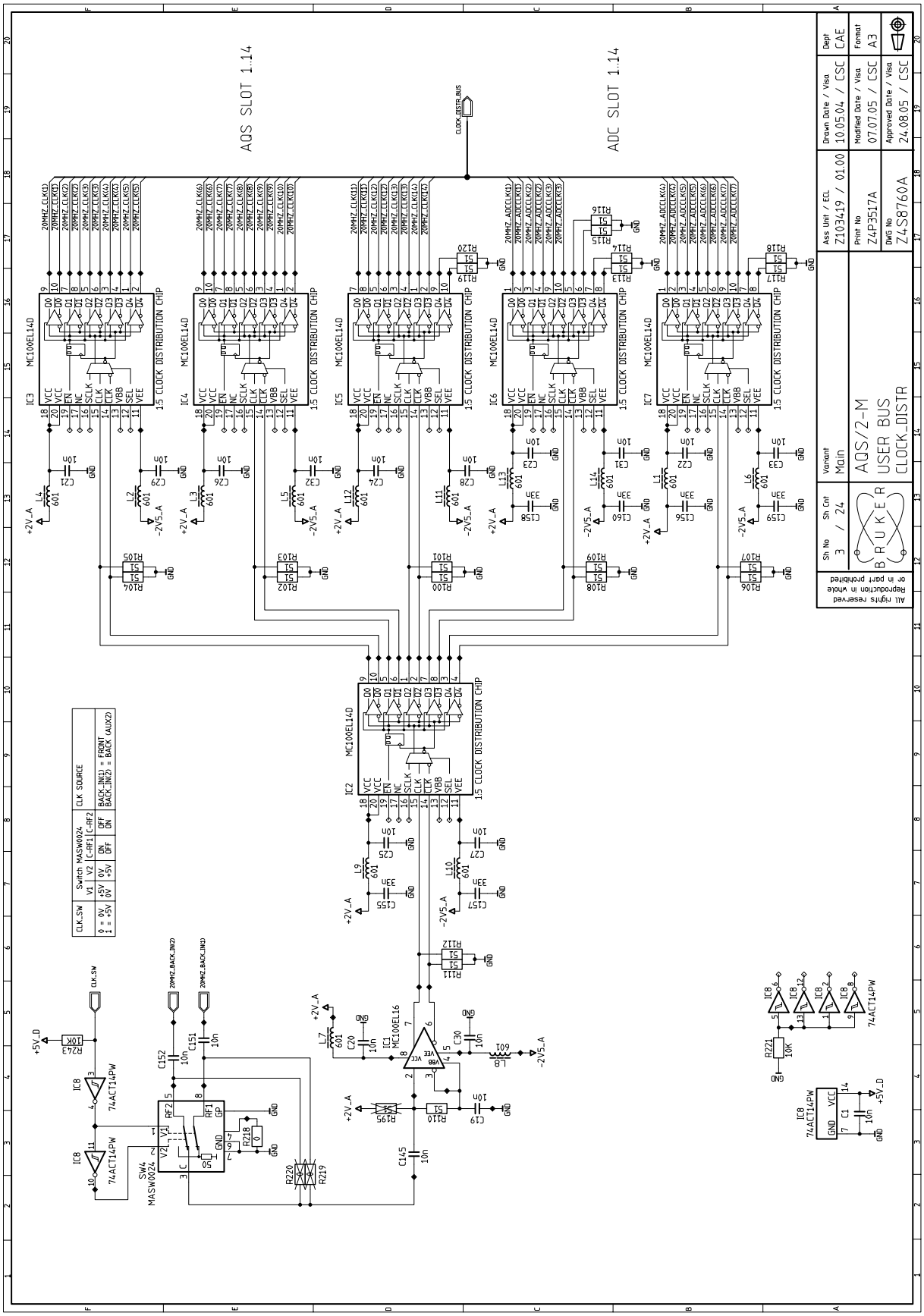


Figure 5.19. User Bus Slot 1

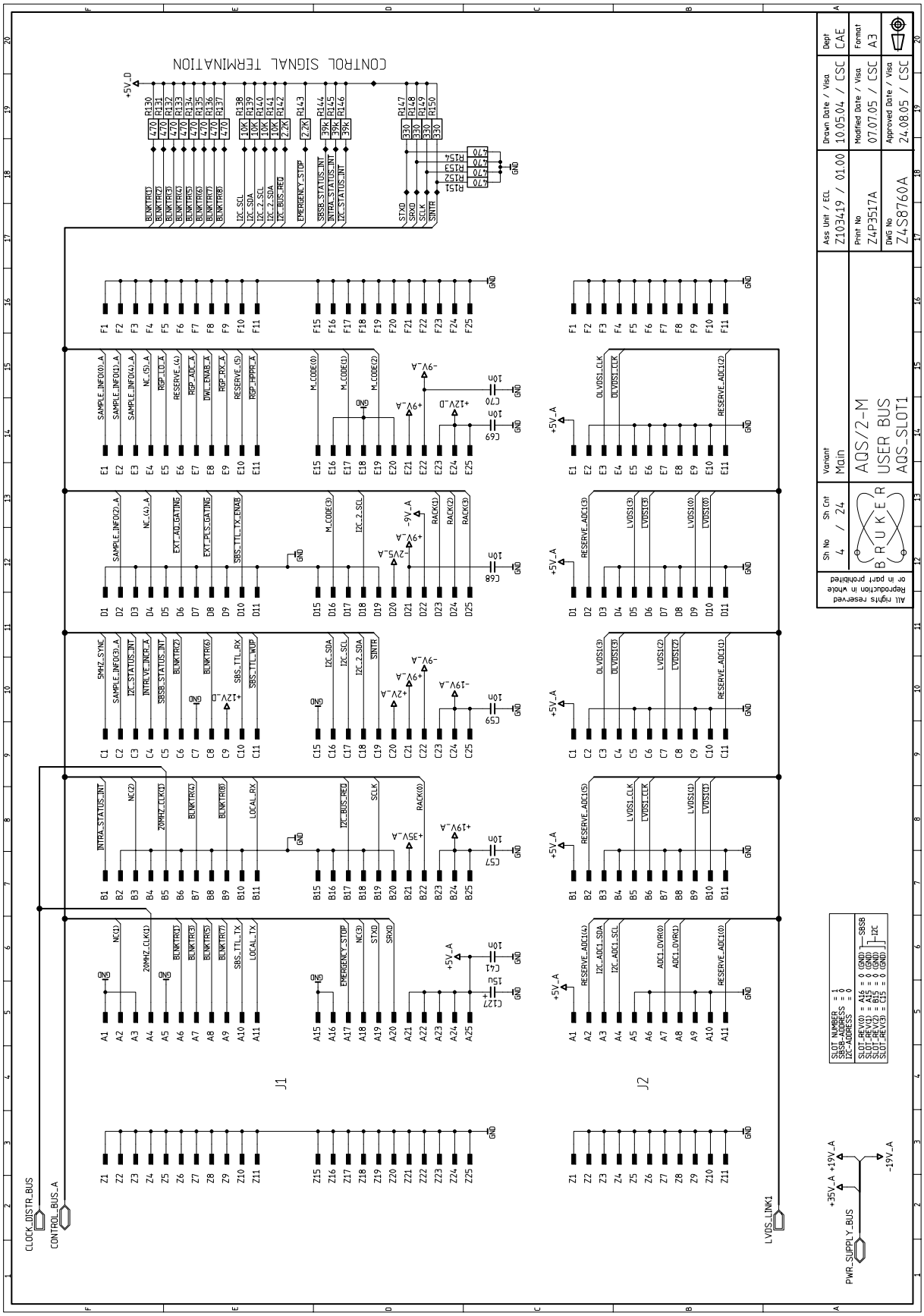


Figure 5.20. User Bus Slot 2

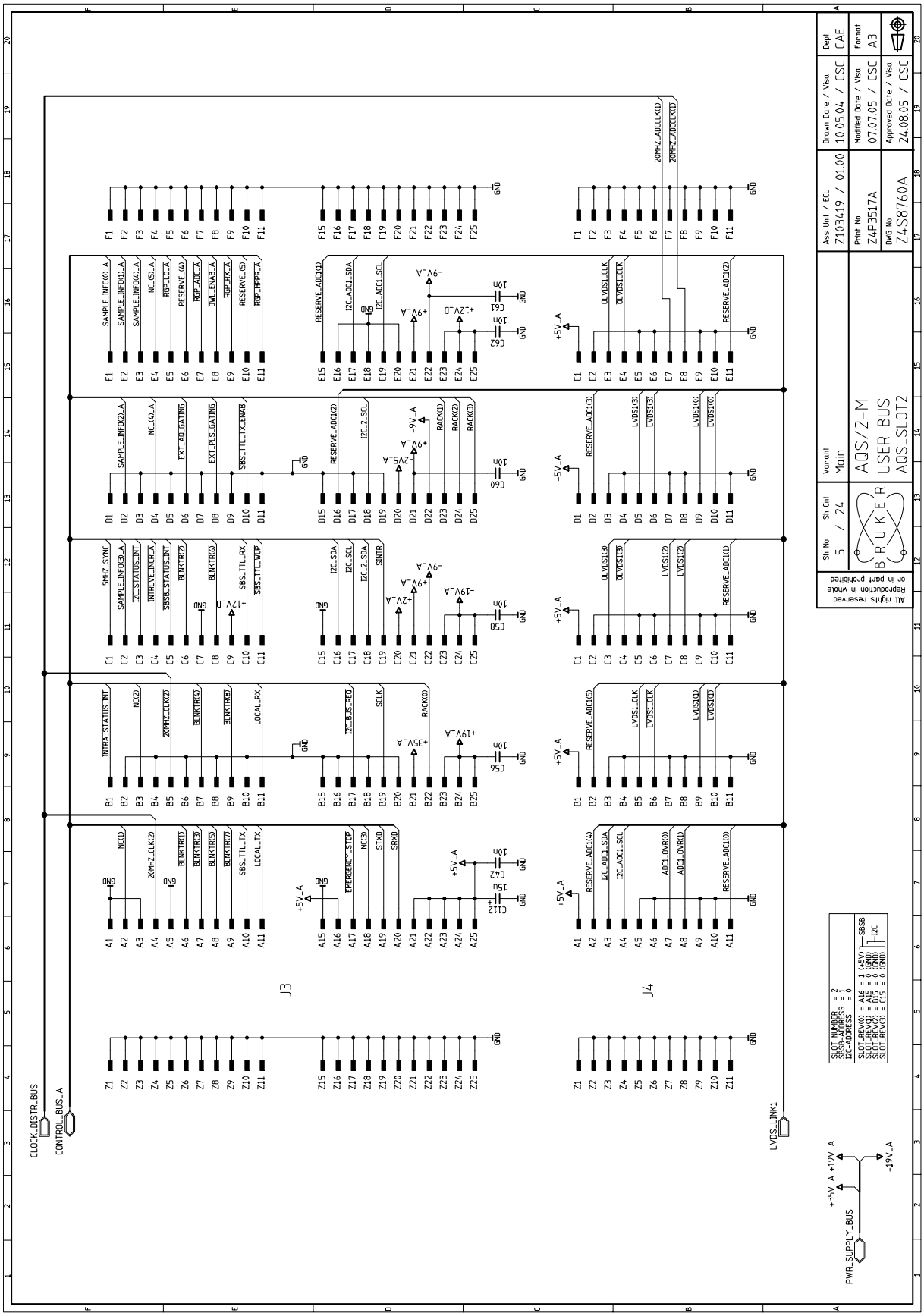


Figure 5.21. User Bus Slot 3

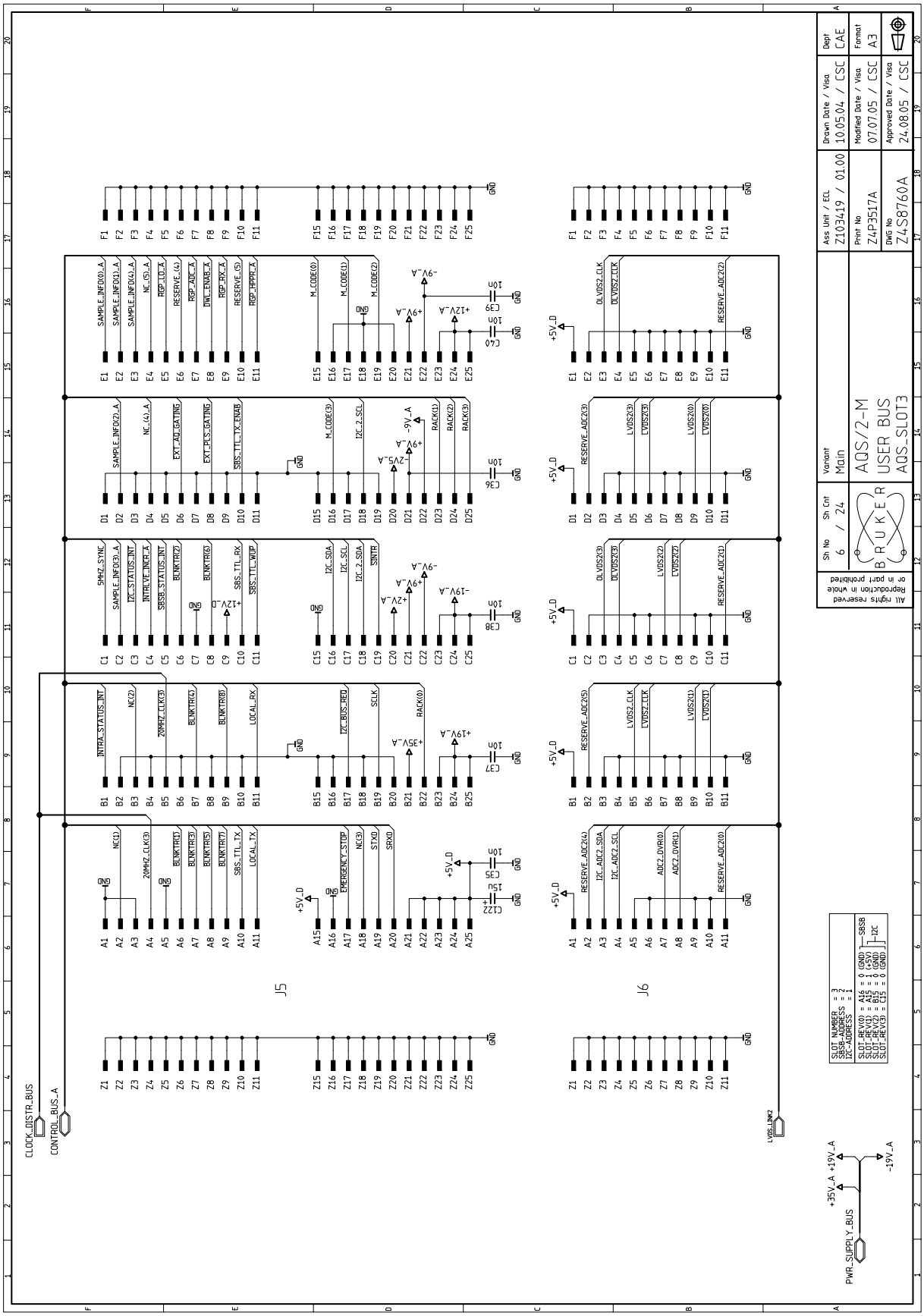


Figure 5.22. User Bus Slot 4

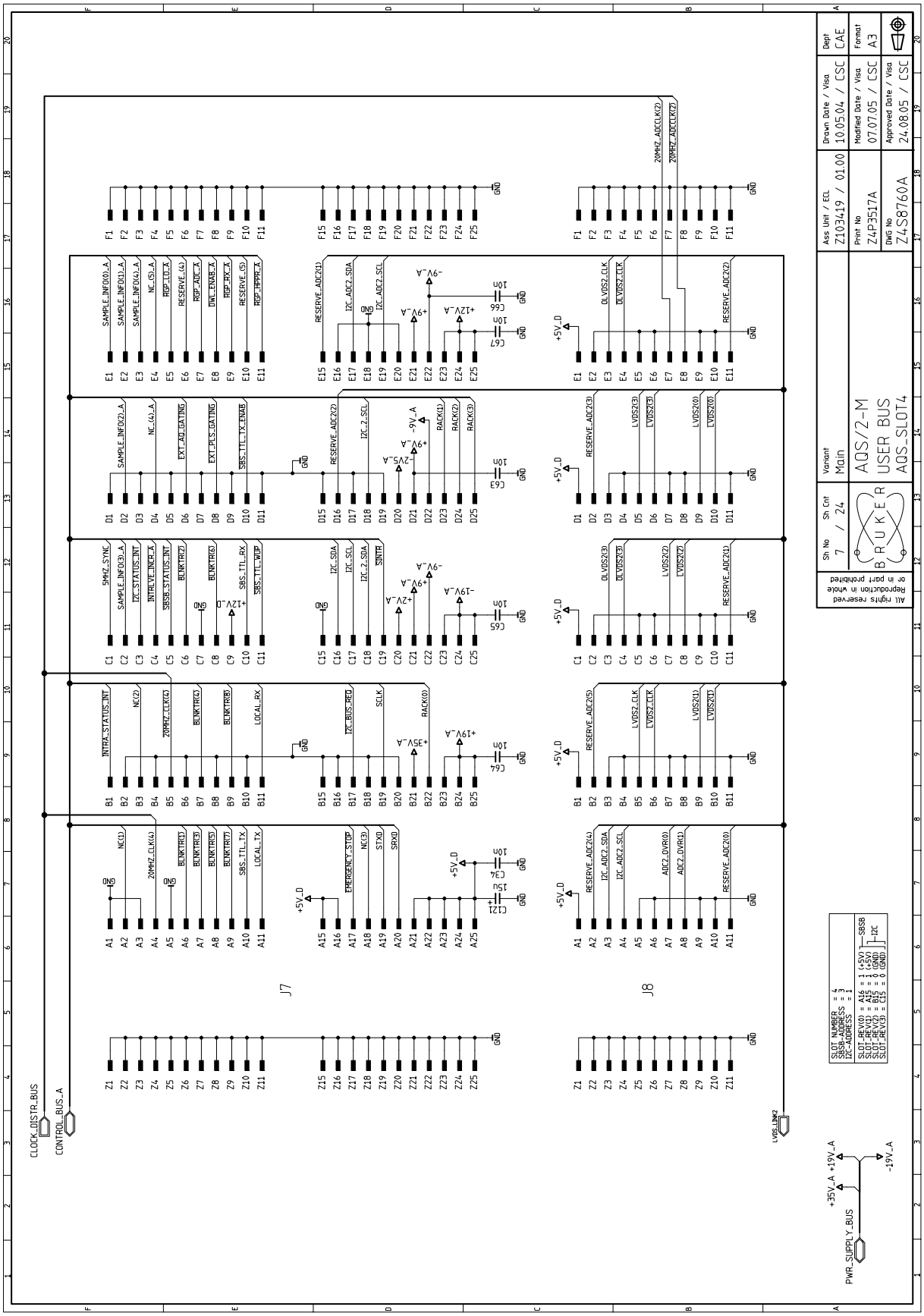


Figure 5.23. User Bus Slot 5

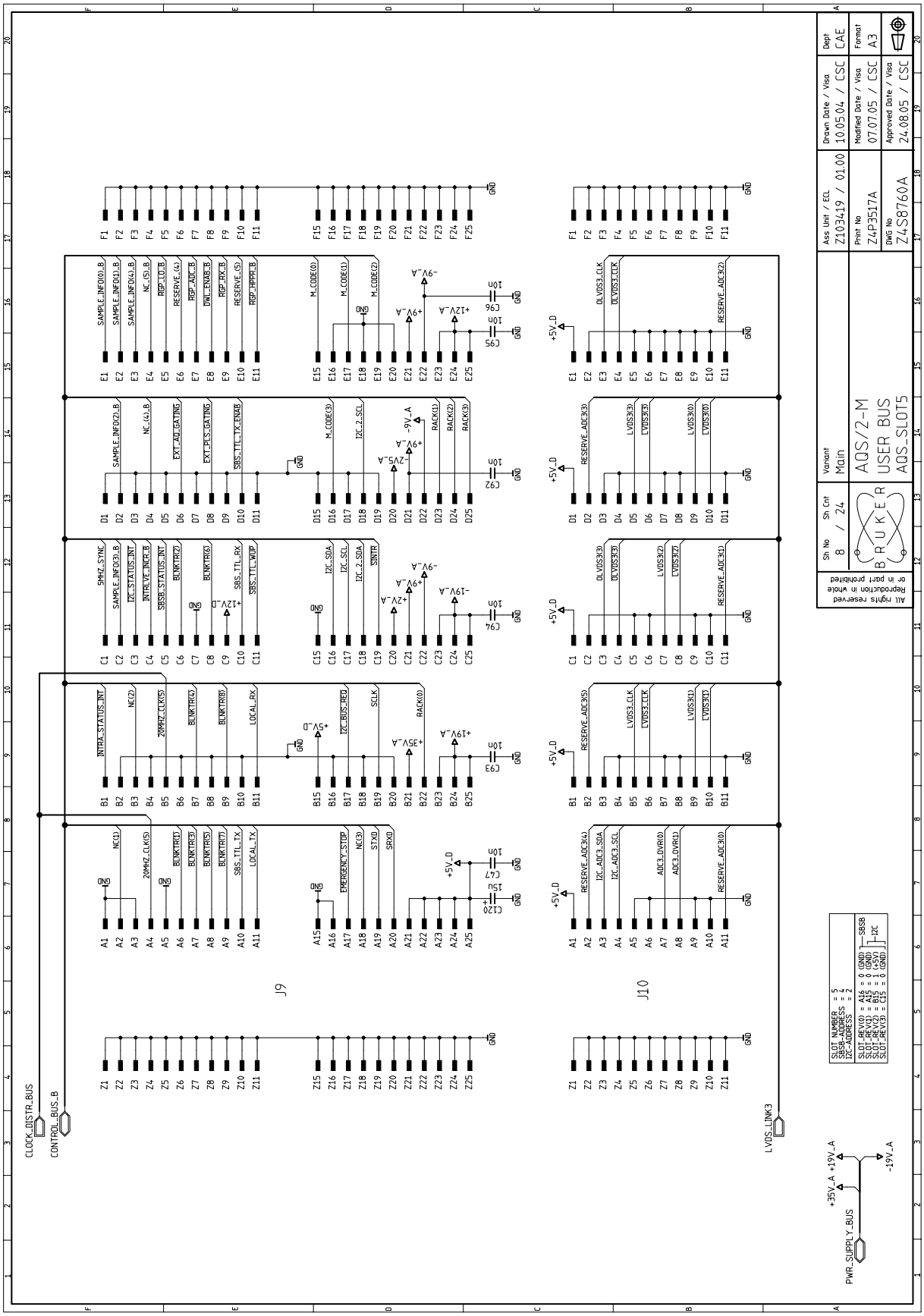


Figure 5.24. User Bus Slot 6

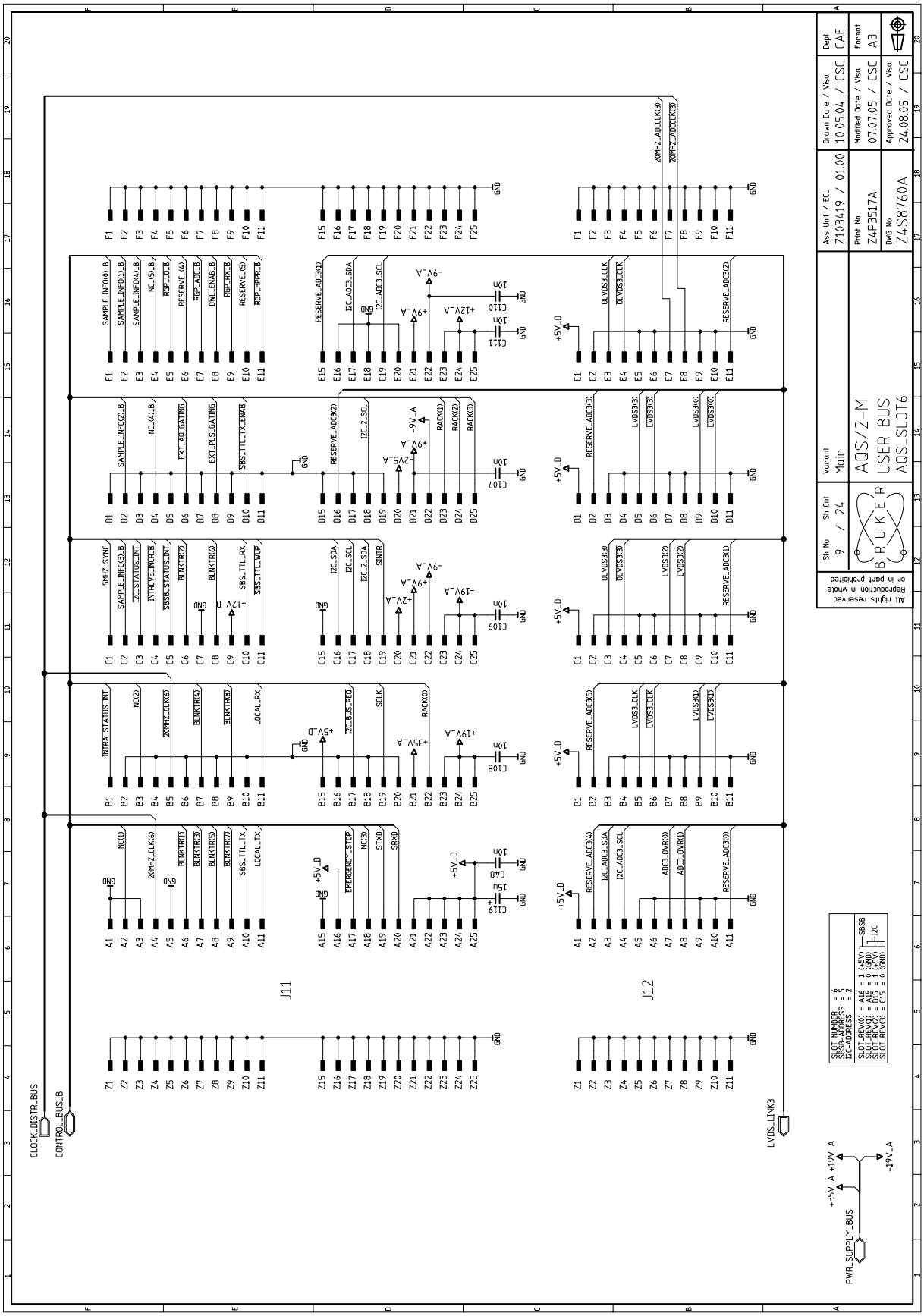


Figure 5.25. User Bus Slot 7

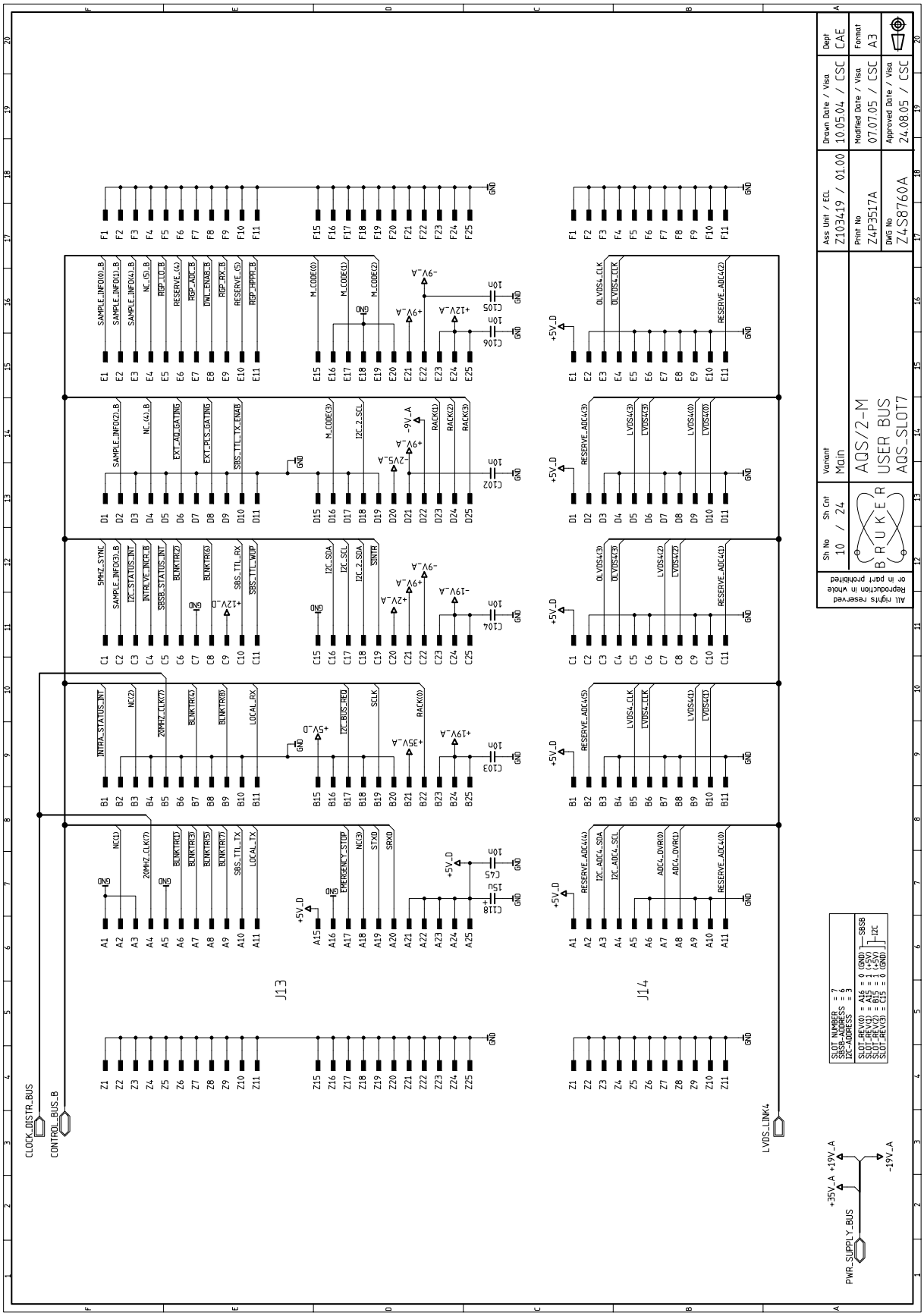


Figure 5.26. User Bus Slot 8

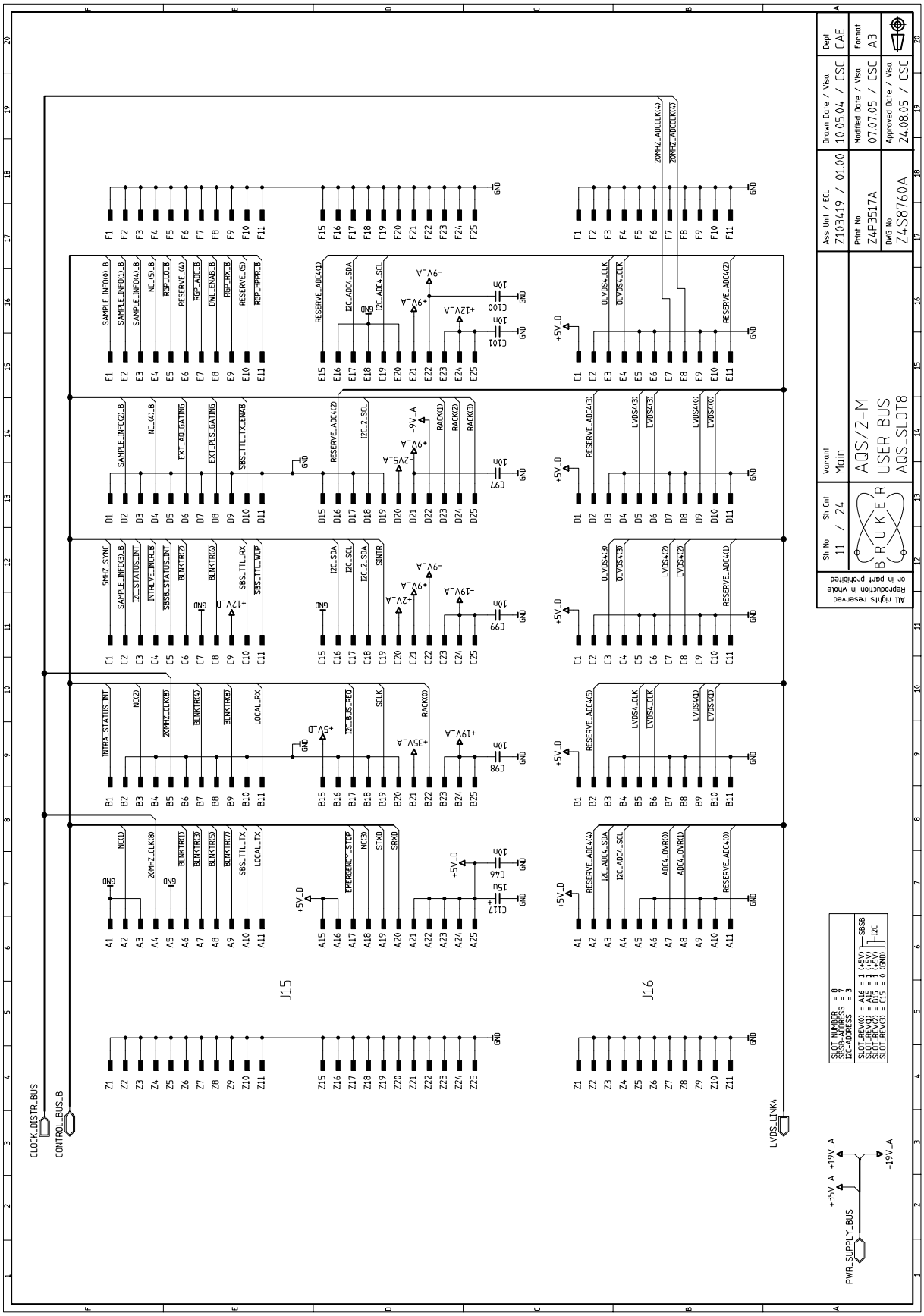


Figure 5.27. User Bus Slot 9

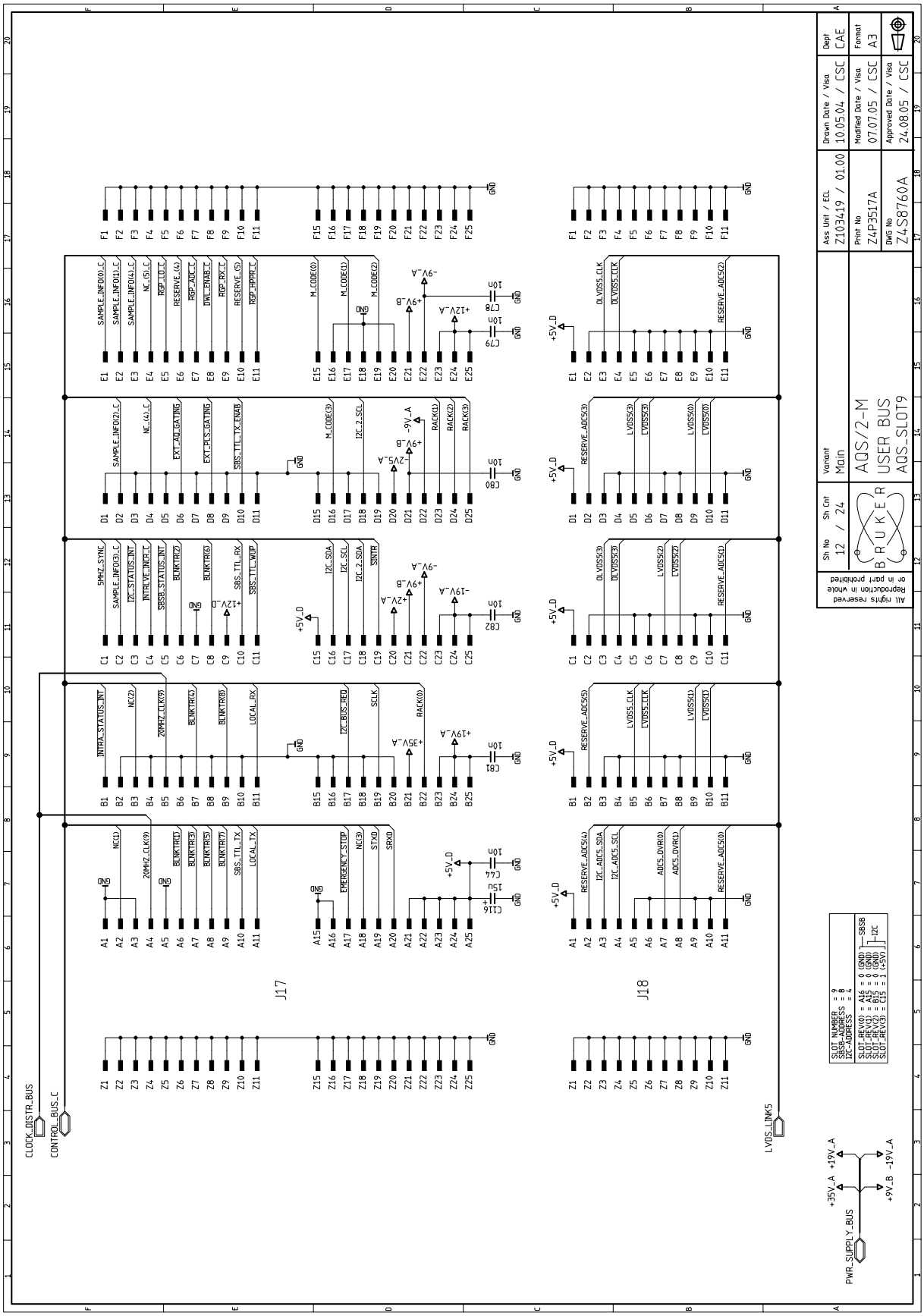


Figure 5.28. User Bus Slot 10

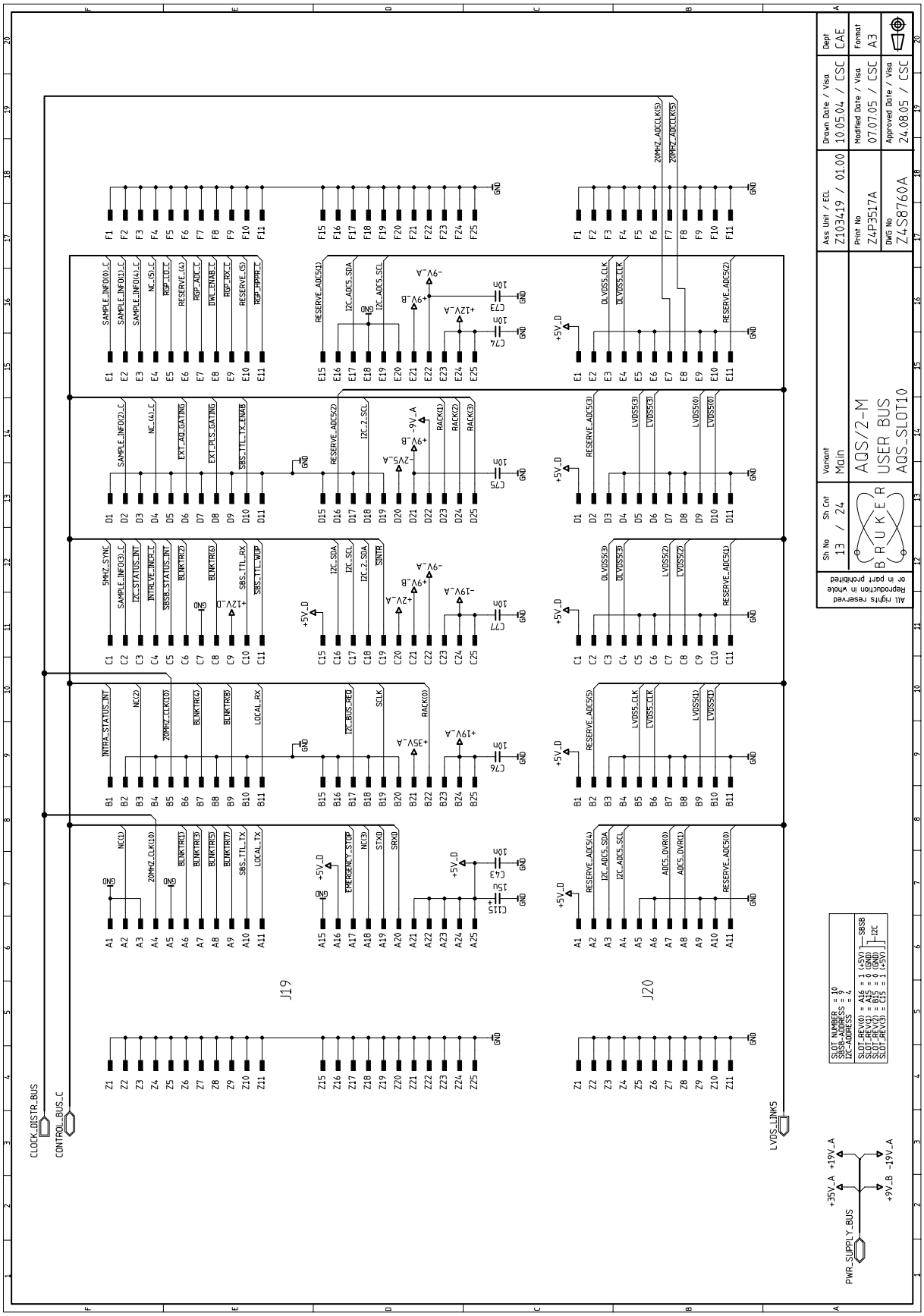


Figure 5.29. User Bus Slot 11

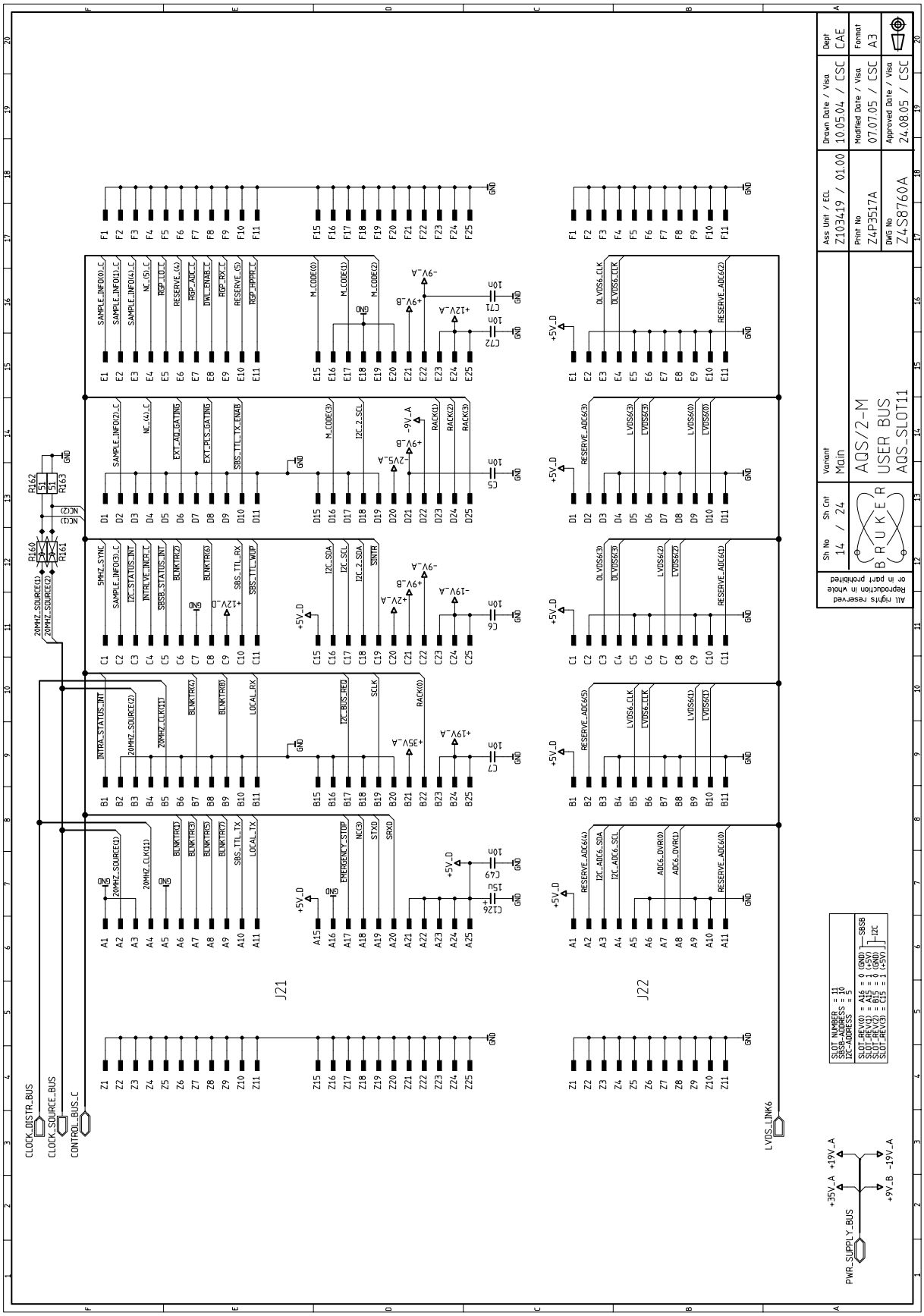


Figure 5.30. User Bus Slot 12

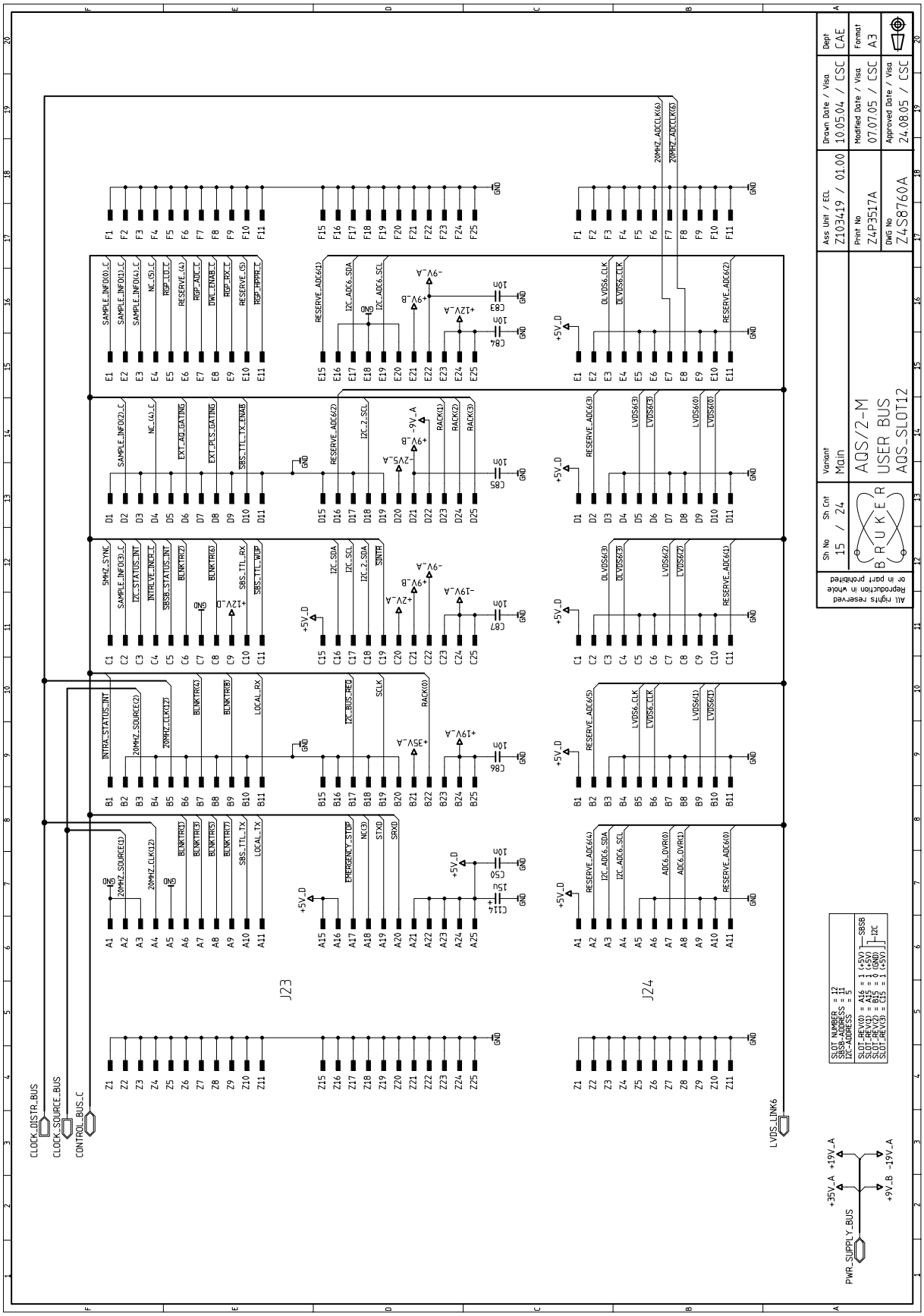


Figure 5.31. User Bus Slot 13

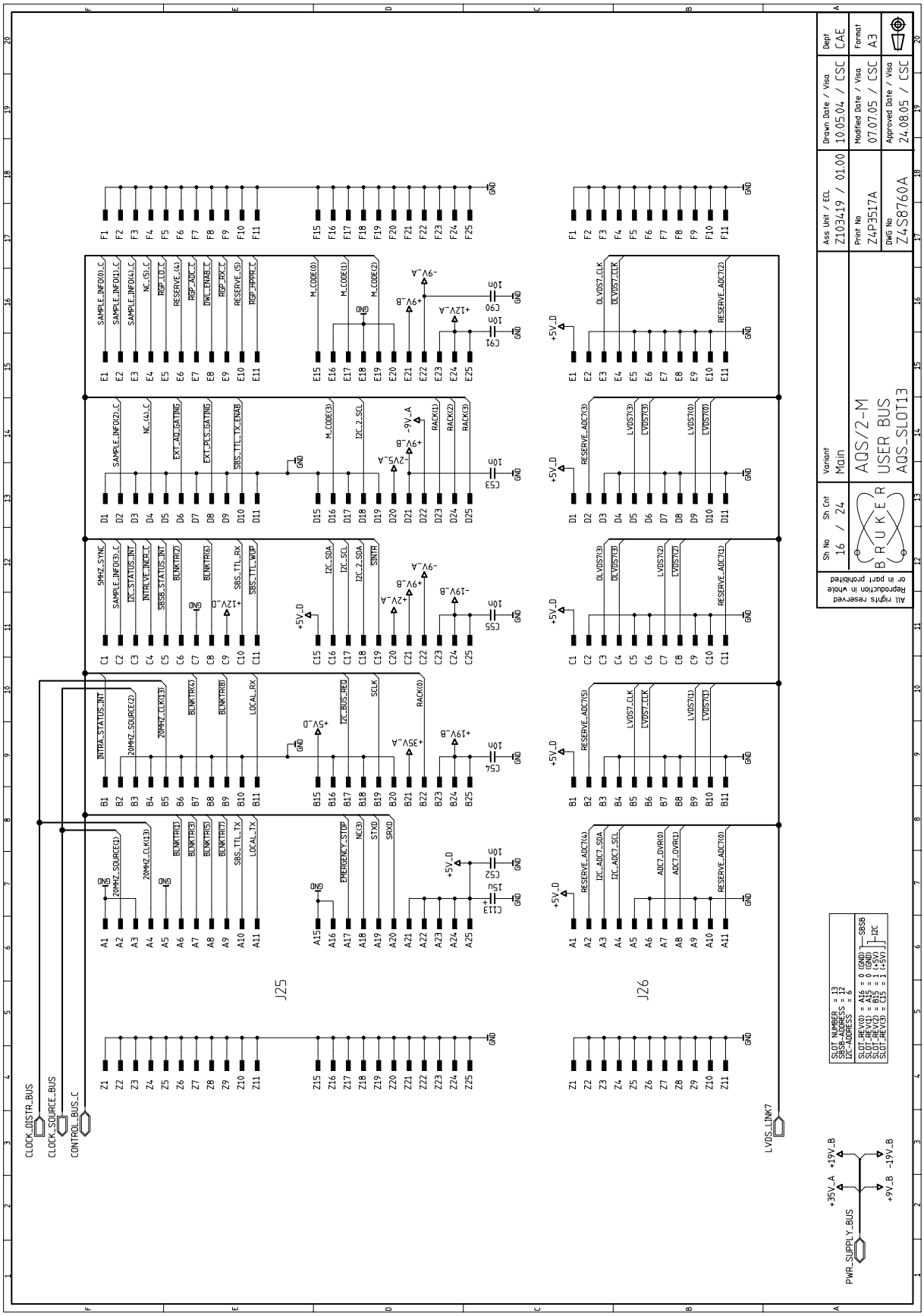


Figure 5.32. User Bus Slot 14

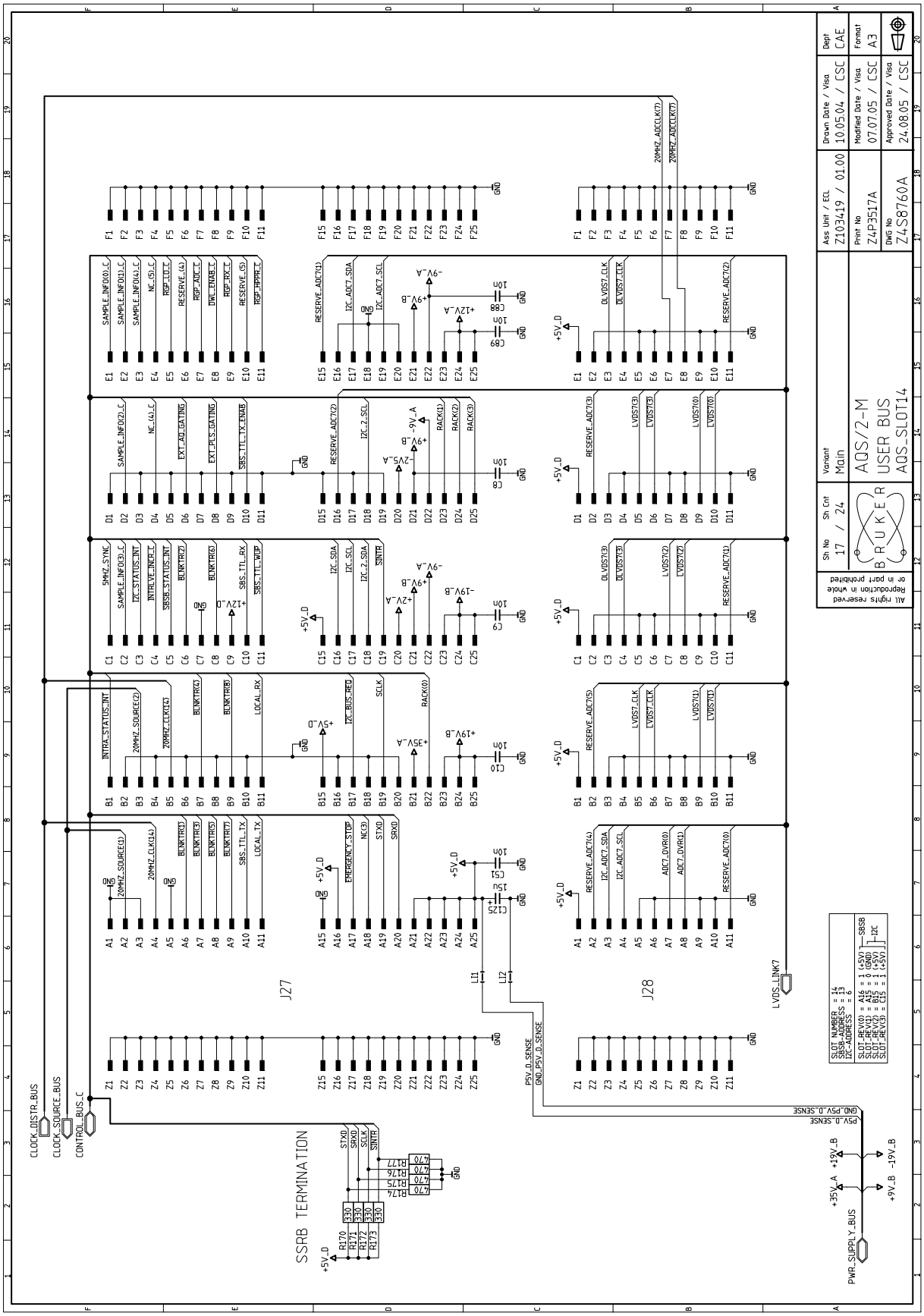


Figure 5.33. PSD Slot

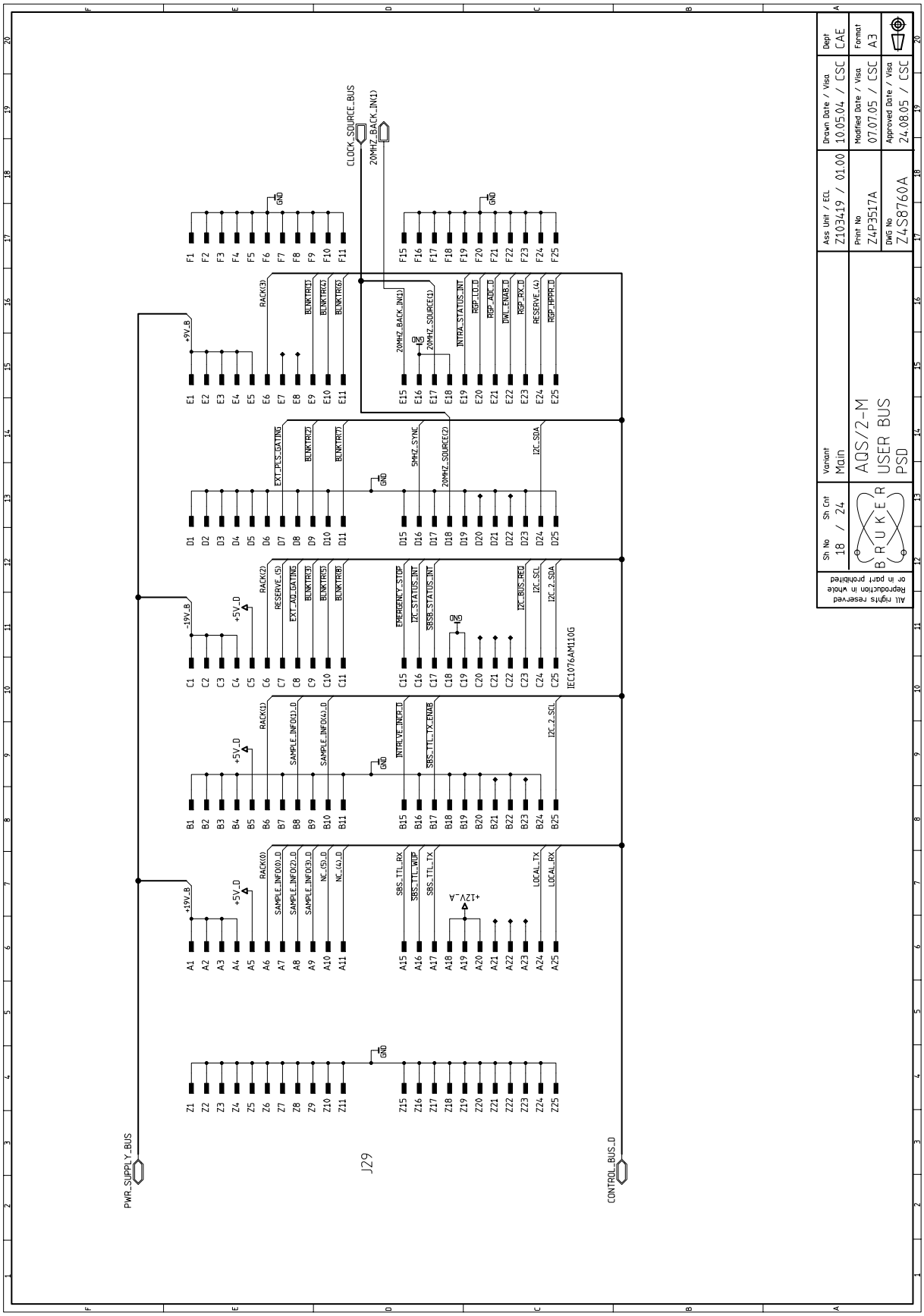


Figure 5.34. Power Supply Slot 1

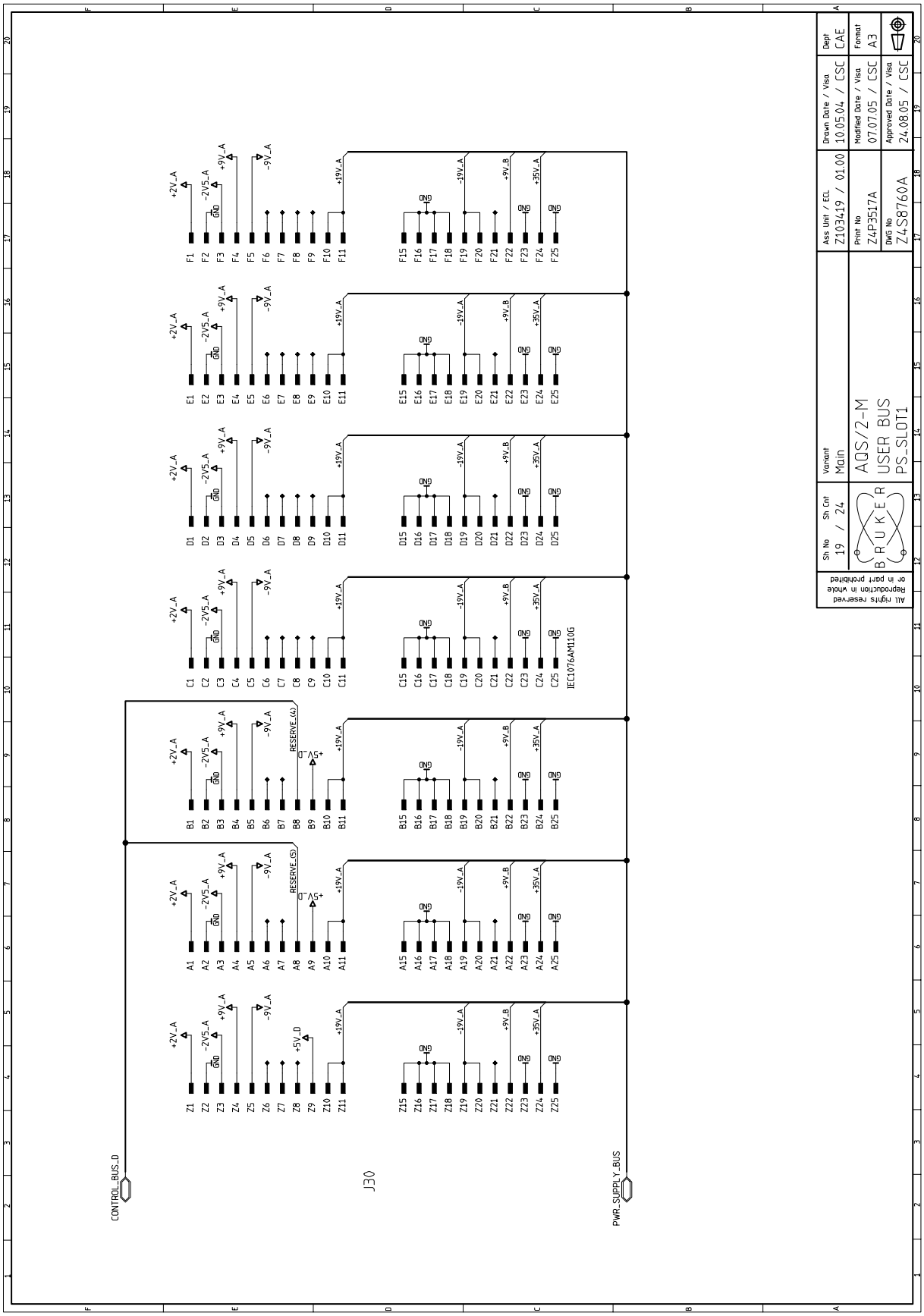


Figure 5.35. Power Supply Slot 2

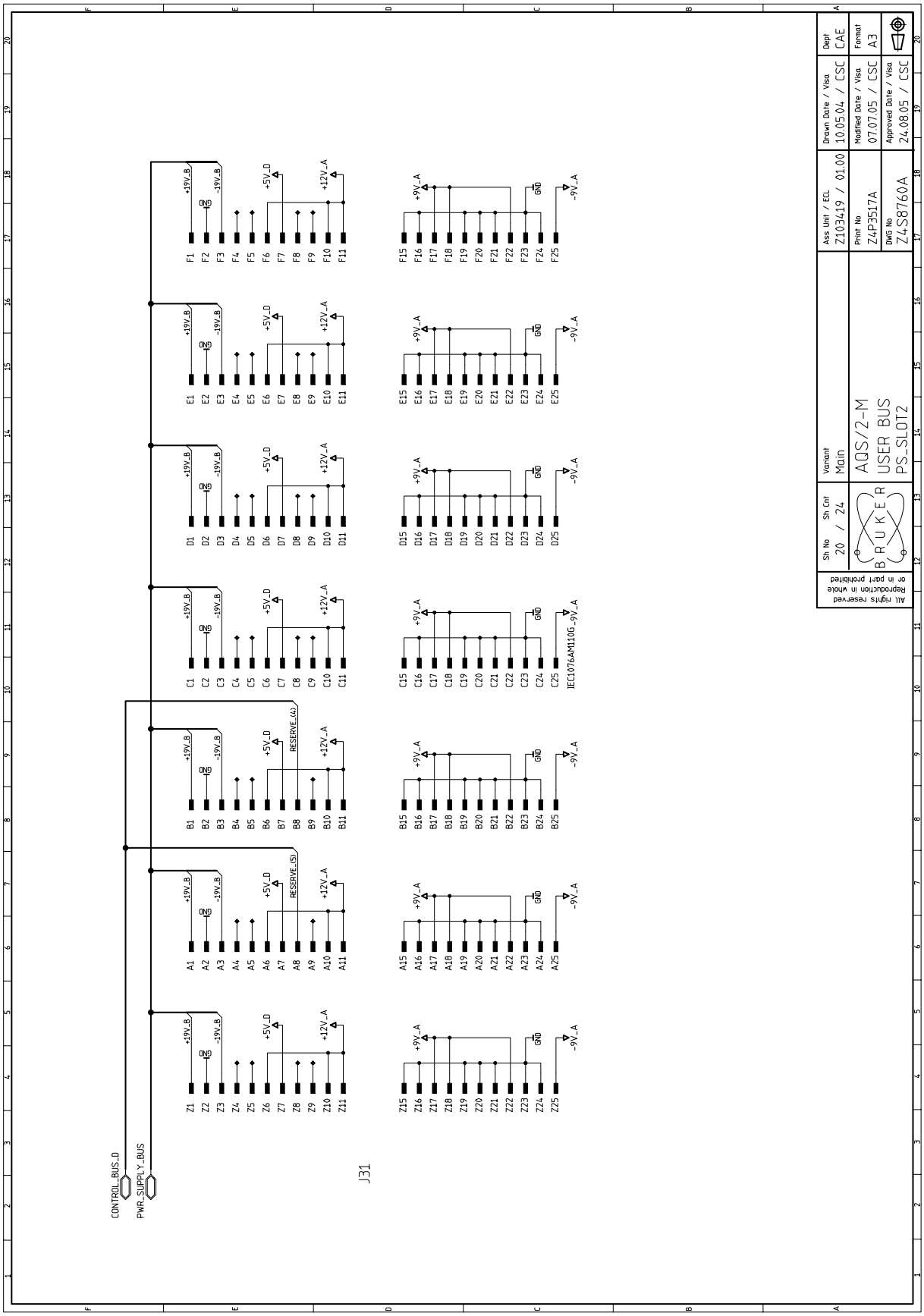


Figure 5.36. Auxilliary Slot 1

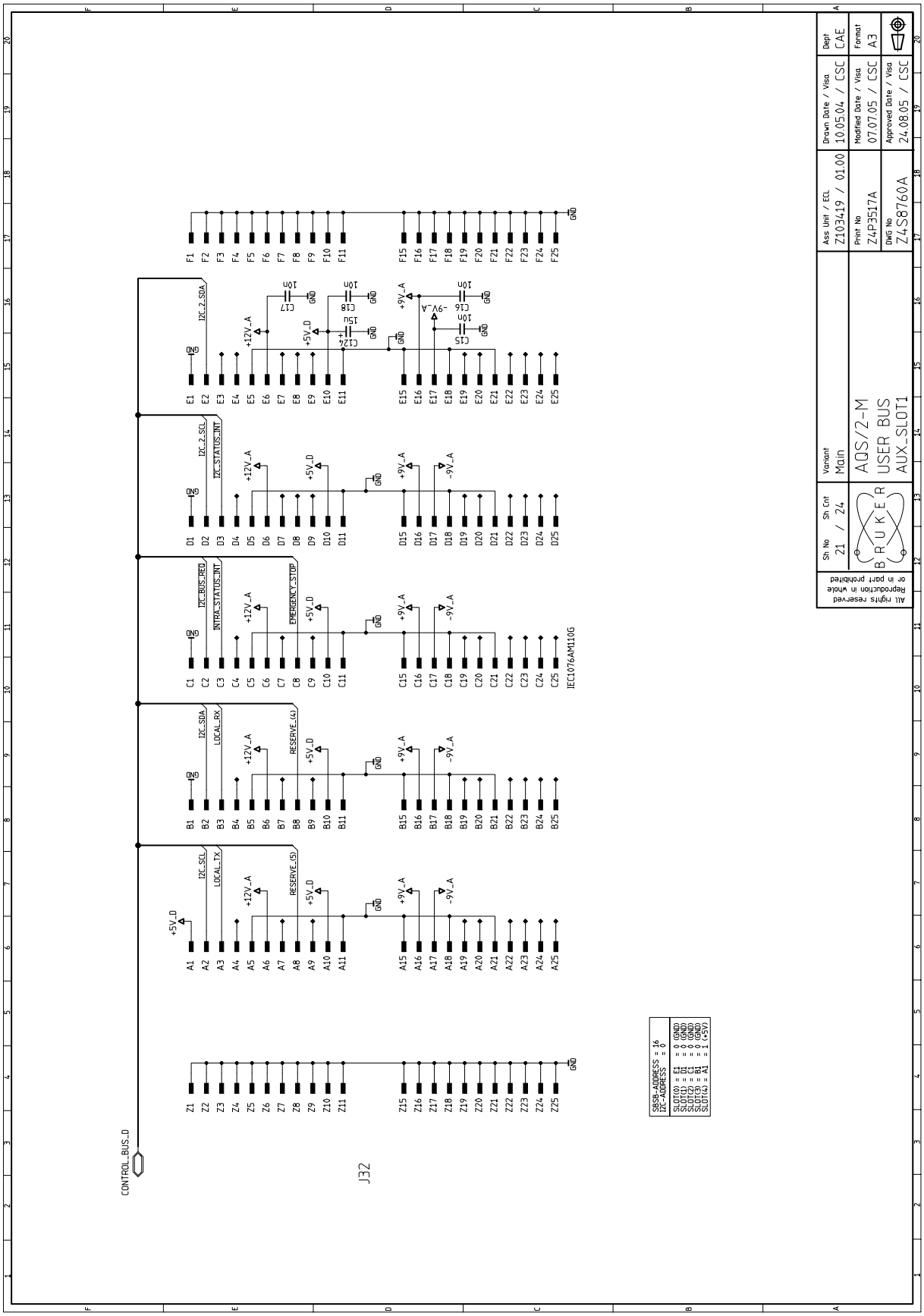


Figure 5.37. Auxilliary Slot 2 (RF-Splitter)

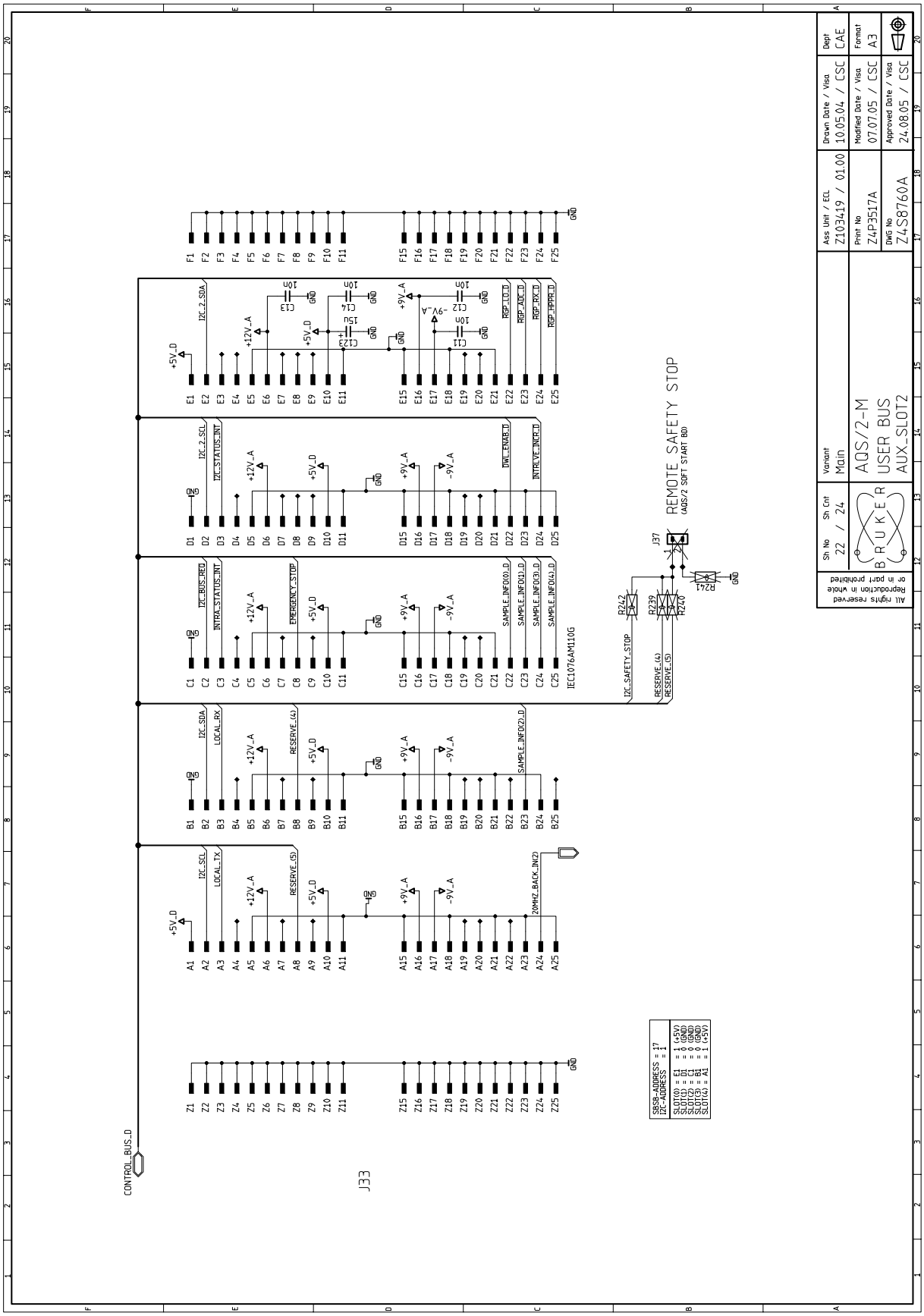
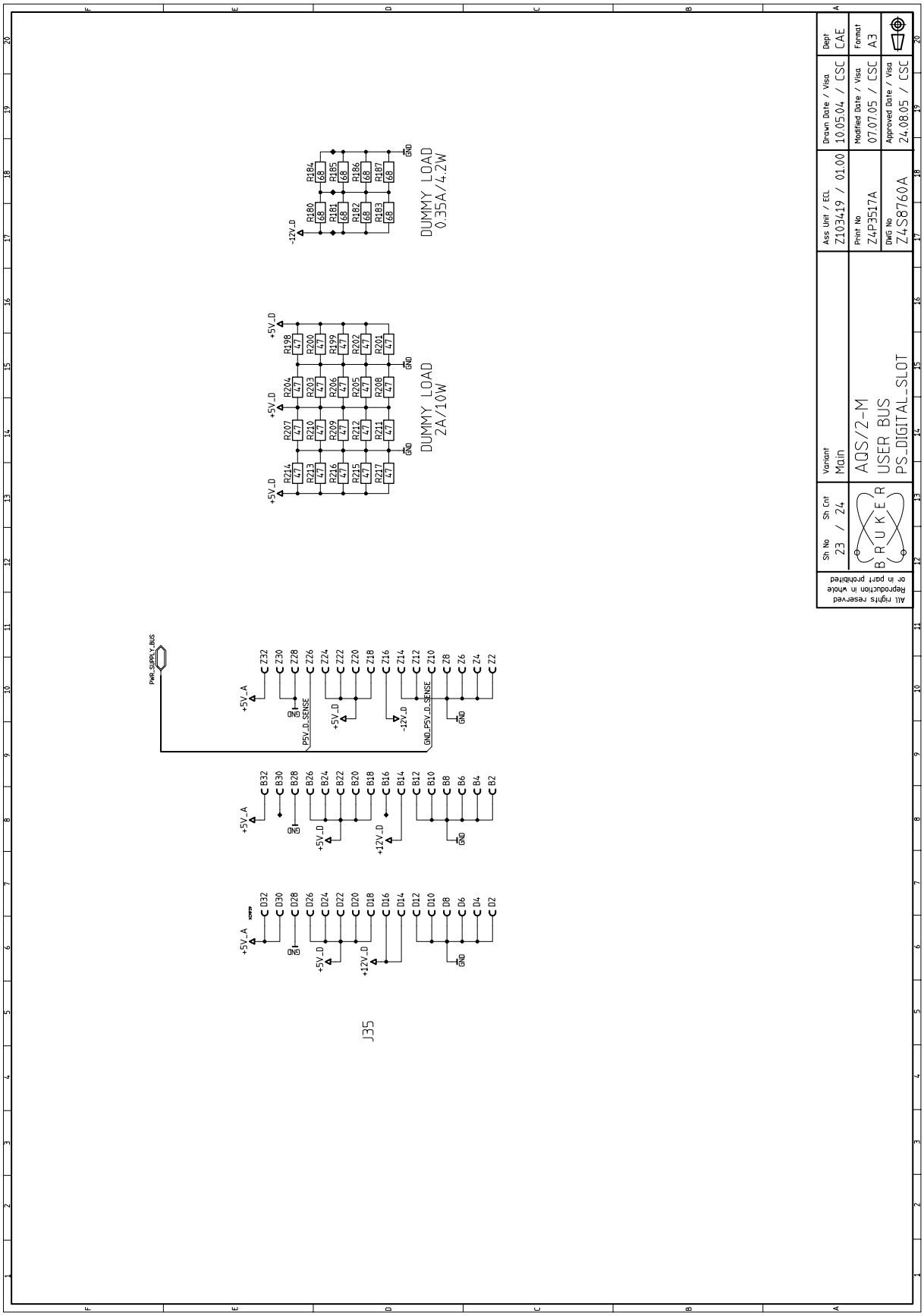


Figure 5.38. PS-Digital Slot



AQS Power Supply 6

Introduction 6.1

The AQS chassis can be equipped with different power supplies, according to the power requirements of the configuration.

Table 6.1. AQS Power Supply Part Numbers

Part Number	Description	Type
H9489	AQS POWER SUPPLY DIGITAL 350W	switched PS
H9520	AQS POWER SUPPLY DIGITAL 450W	switched PS
Z003402	AQS PSM1 POWER SUPPLY MODULE	linear PS
Z003403	AQS PSM2 POWER SUPPLY MODULE	linear PS
Z003404 [a]	*AQS PSM3 POWER SUPPLY MODULE*	*linear PS*
Z102023	AQS PSM5 POWER SUPPLY MODULE	linear and switched PS
W1345050	POWER SUPPLY COMPACT 28V 20A	switched PS
Z104783	AQS PSM HPLNA	switched PS

a This unit is obsolete. The replacement power supply is the AQS PSM5.

Table 6.2. Power Supply Comparison Table

Shortname	Supply Output						Power	Load
PS DIGITAL 350W PS DIGITAL 450W	+5V 36A 50A	+5V 10A 14A	+12V 8A 9A	-12V 2A 3A			350W 460W	VME BUS, Fan USER BUS
PSM1	+2V 0.5A	-2.5V 0.2A	+19V 6.4A	-19V 2.5A	+9V 5A	+35V 0.2A	220W	USER BUS HPPR
PSM2 PSM3 PSM5	+19V 1.5A 1.5A 1.5A	-19V 1.5A 1.5A 1.5A	+12V 5.8A 7.3A 17A	+9V 5.6A 7.3A 7.3A	-9V 2.7A 3.9A 3.9A		200W 360W 470W	USER BUS HPPR
PS BLA 28V	+28V 20A						560W	internal BLA (pulsed power)
PSM HPLNA	+500V 0.2A	+20V 0.1A	-5V 3A				117W	HPLNA (floating supply)

AQS Switched Power Supply Units *6.2*

- AQS POWER SUPPLY DIGITAL 350W (H9489)
- AQS POWER SUPPLY DIGITAL 450W (H9520)
- POWER SUPPLY COMPACT 28V 20A (W1345050)

These units consist of a compact switched power supply module with multiple outputs. The ac-input cable connects directly to the line output socket at the rear side of the chassis. The dc-outputs connect to the backplane.

The supply status is indicated with LED‘s on the front panel.

The units have no serviceable parts or fuses.

Figure 6.1. View Switched Power Supply

AQS POWER SUPPLY DIGITAL 350W

POWER SUPPLY COMPACT 28V 20A

AQS PSM HPLNA 6.2.1

The PSM HPLNA consists of a compact AC/DC power supply module with multiple outputs. The input cable connects directly to the line output socket at the rear side of the chassis. The dc-outputs connect to two D-SUB connectors with high-voltage pins on the front panel.

The supply status is indicated with LED‘s on the front panel.

The unit has no serviceable parts or fuses.

Figure 6.2. View PSM HPLNA

Attention HIGH VOLTAGE:

The D-SUB connectors A and B carry high voltage (+500Vdc).

Linear Power Supply Modules 6.3

The linear power supply modules consist of rectifiers and linear regulators mounted on an open print. The ac-inputs connects directly to the transformer in the chassis via a front panel connector. The dc-outputs connect to the backplane.

The supply status is indicated with LED‘s on the front panel.

The PSM5 has an additional switched power supply module mounted on the print. It‘s ac-input cable connects directly to the line output socket at the rear side of the chassis.

PSM1 6.3.1

Figure 6.3. Overview PSM1

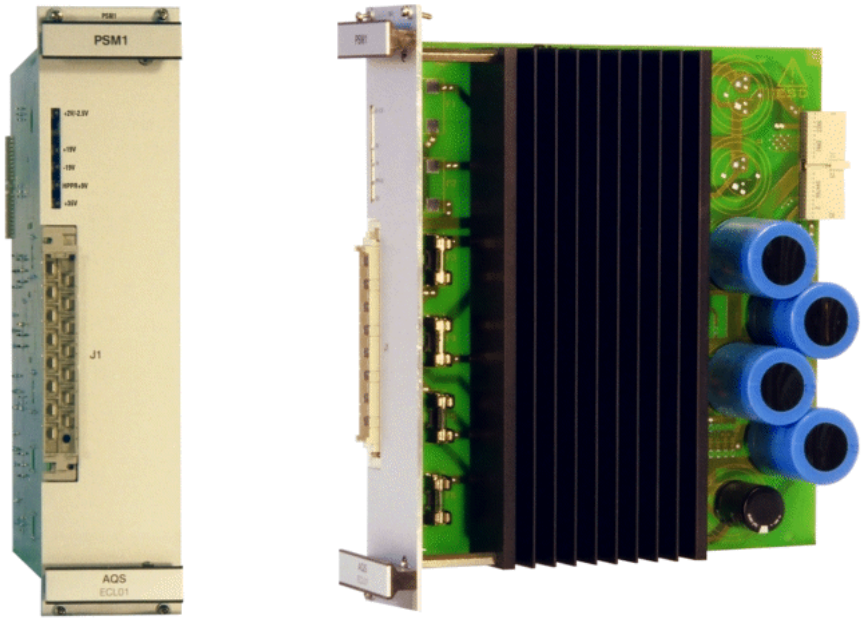


Table 6.3. Fuses PSM1

SUPPLY	FUSE	CAT_NM	VALUE
+19V	F3	2259	8AT
-19V	F4	2256	3.15AT
HPPR +9V	F5	4907	5AT
+35V	F6	2248	0.5AT [a]

a prior fuse was 0.315AT

Figure 6.4. Assembly Drawing PSM1

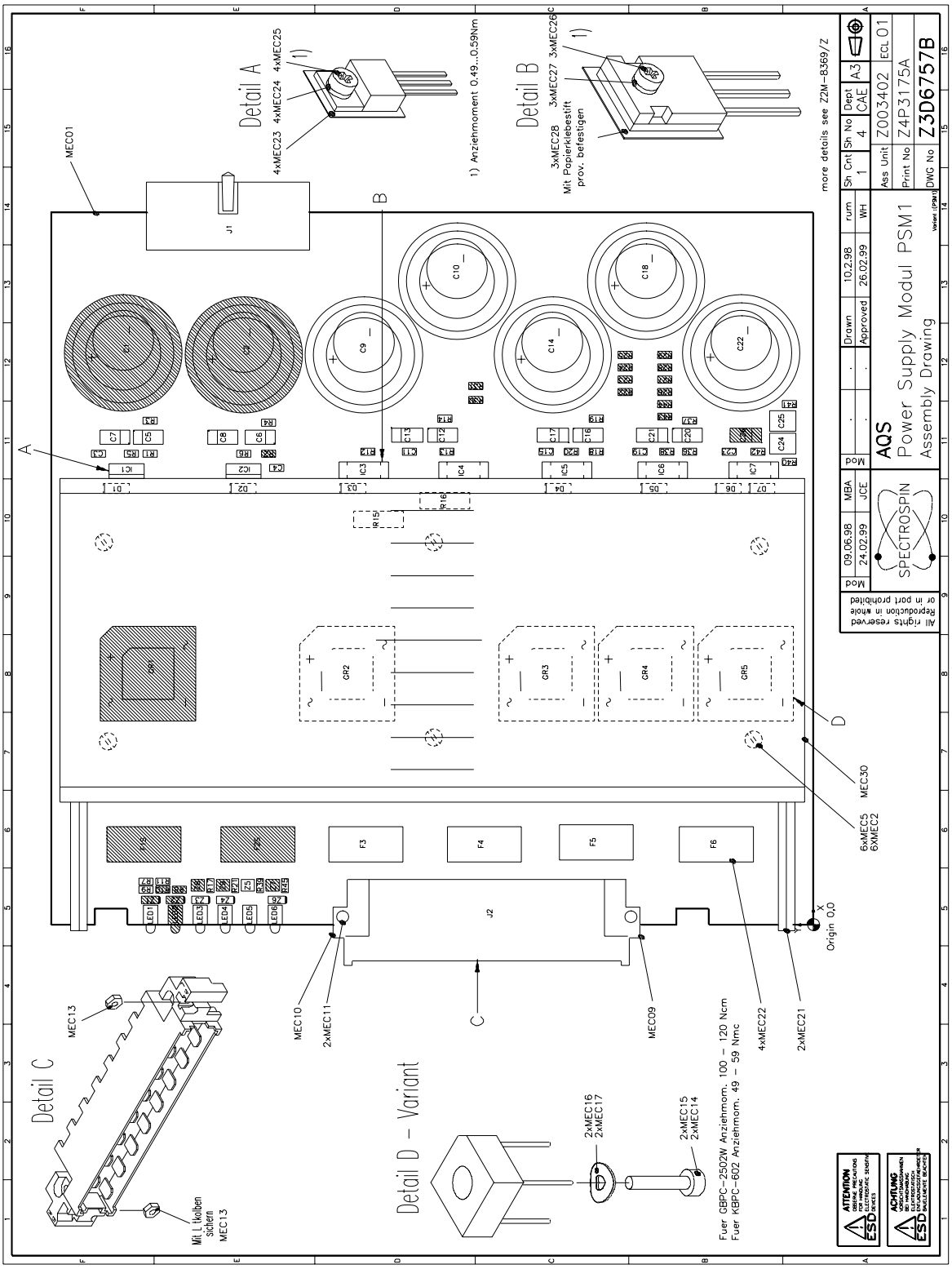


Figure 6.5. Overview PSM2

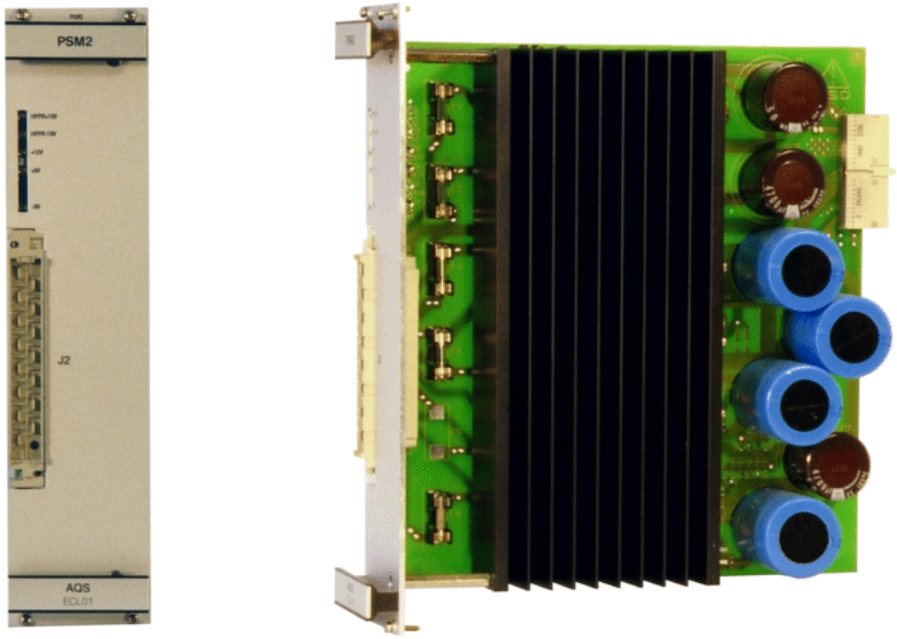
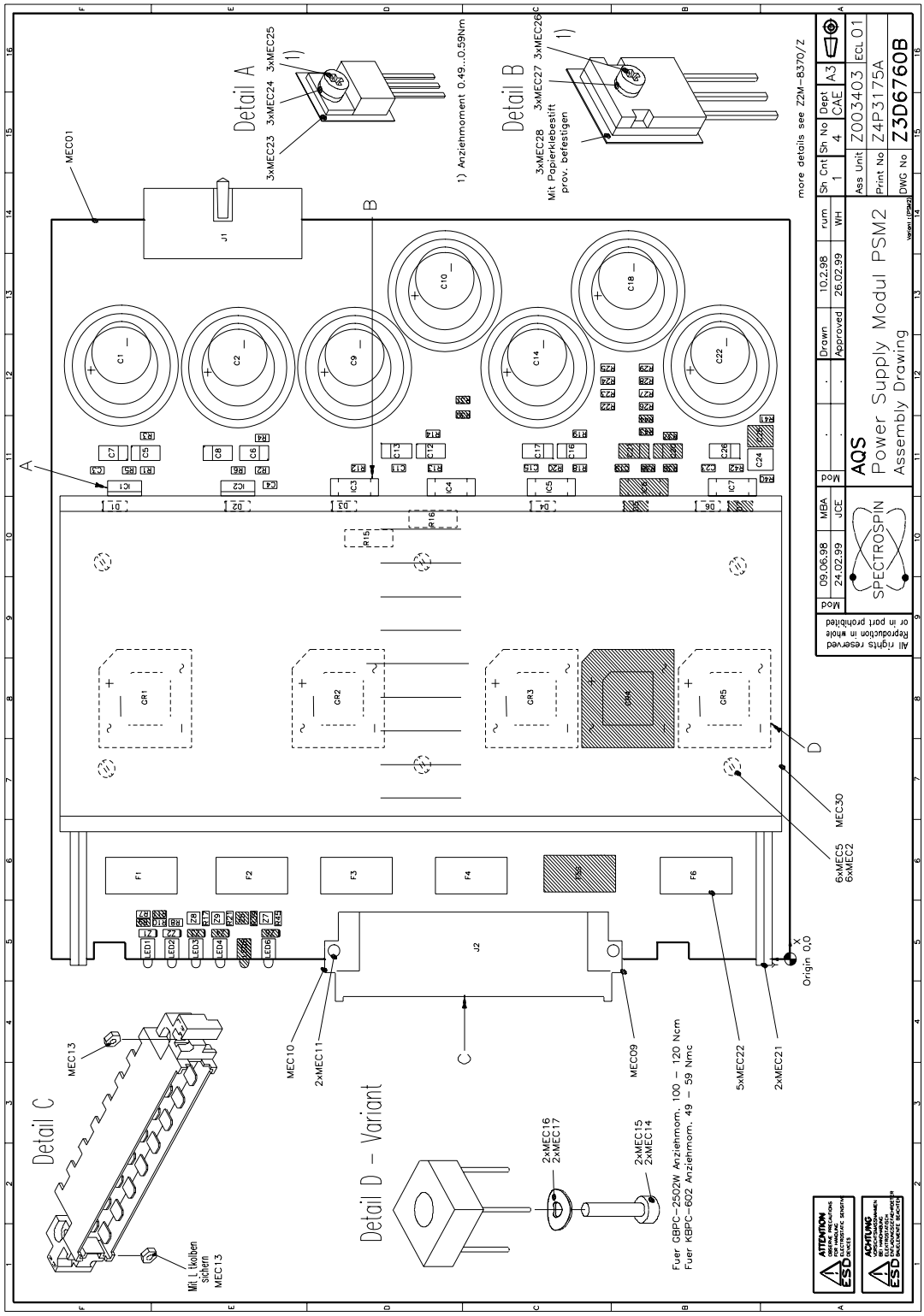


Table 6.4. Fuses PSM2

SUPPLY	FUSE	CAT_NM	VALUE
HPPR +19V	F1	2254	2AT
HPPR -19V	F2	2254	2AT
+12V	F3	2259	8AT
+9V	F4	2258	6.3AT
-9V	F6	2257	4AT

Figure 6.6. Assembly Drawing PSM2



The AQS PSM3 is compatible to the PSM2, although it is double as wide because of the increased output power.

! ***This unit is obsolete.***

The replacement power supply is the AQS PSM5.

See ***"PSM5" on page 142***

Figure 6.7. Overview PSM3

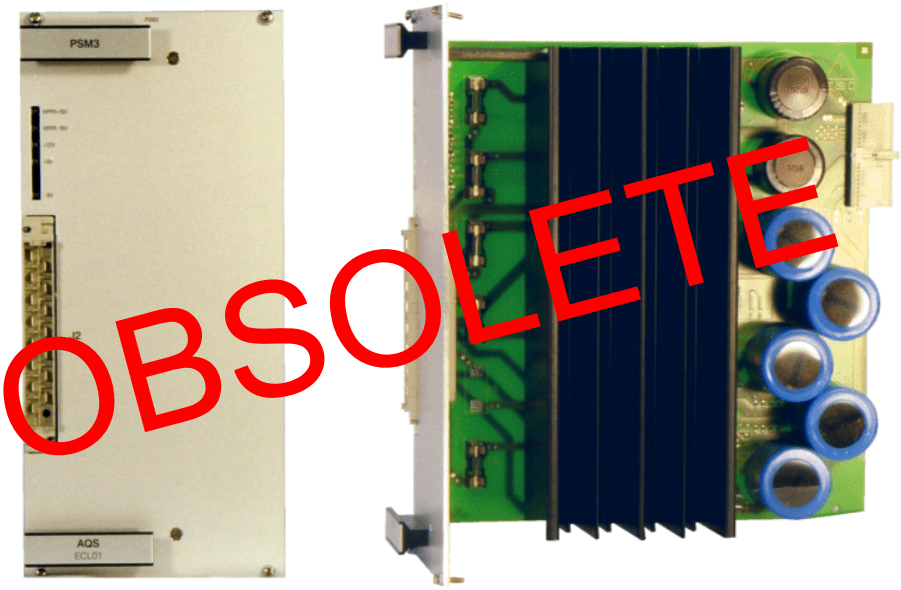
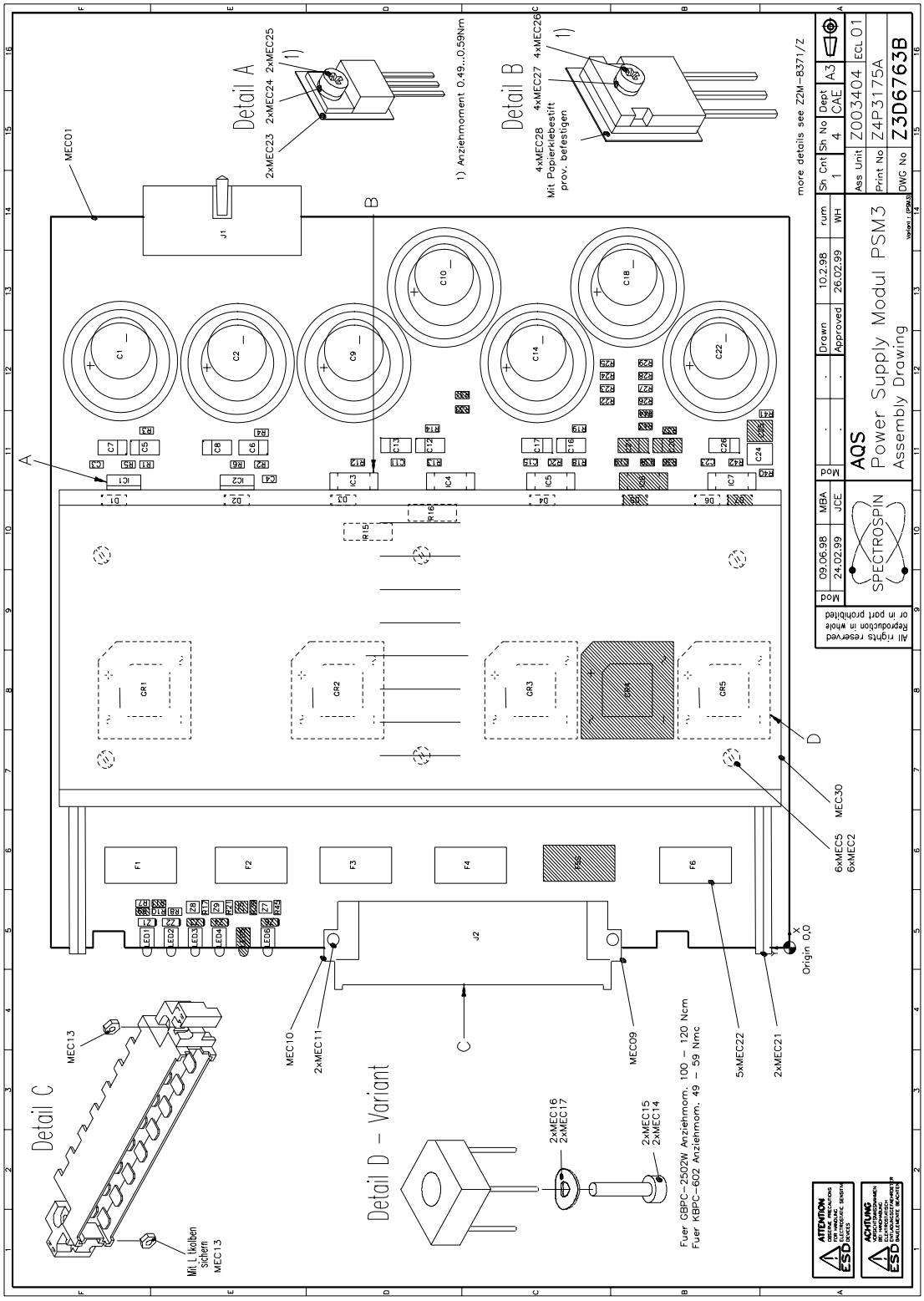


Table 6.5. Fuses PSM3

SUPPLY	FUSE	CAT_NM	VALUE
HPPR +19V	F1	2254	2AT
HPPR -19V	F2	2254	2AT
+12V	F3	2260	10AT [a]
+9V	F4	2259	8AT
-9V	F6	4907	5AT

a prior fuse was 8AT

Figure 6.8. Assembly Drawing PSM3



The AQS PSM5 is fully compatible to the PSM2 and PSM3. The main difference is the increased output power.

If a PSM5 is used as a relacement of a PSM3, an additional frontplate (Z12170) may be necessary to cover the empty space left behind by the wider unit.

Figure 6.9. Overview PSM5

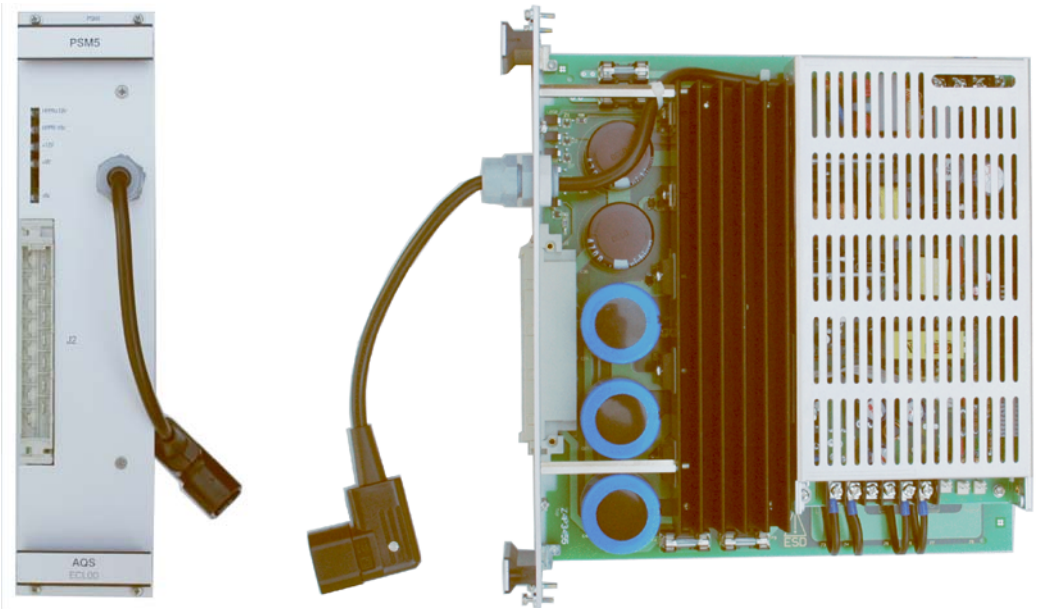


Table 6.6. Fuses PSM5

SUPPLY	FUSE	CAT_NM	VALUE
HPPR +19V	F1	2254	2AT
HPPR -19V	F2	2254	2AT
+9V	F3	2259	8AT
-9V	F4	4907	5AT

The +12V supply from the switched power supply module has no serviceable fuse.

Figure 6.10. Assembly Drawing PSM5

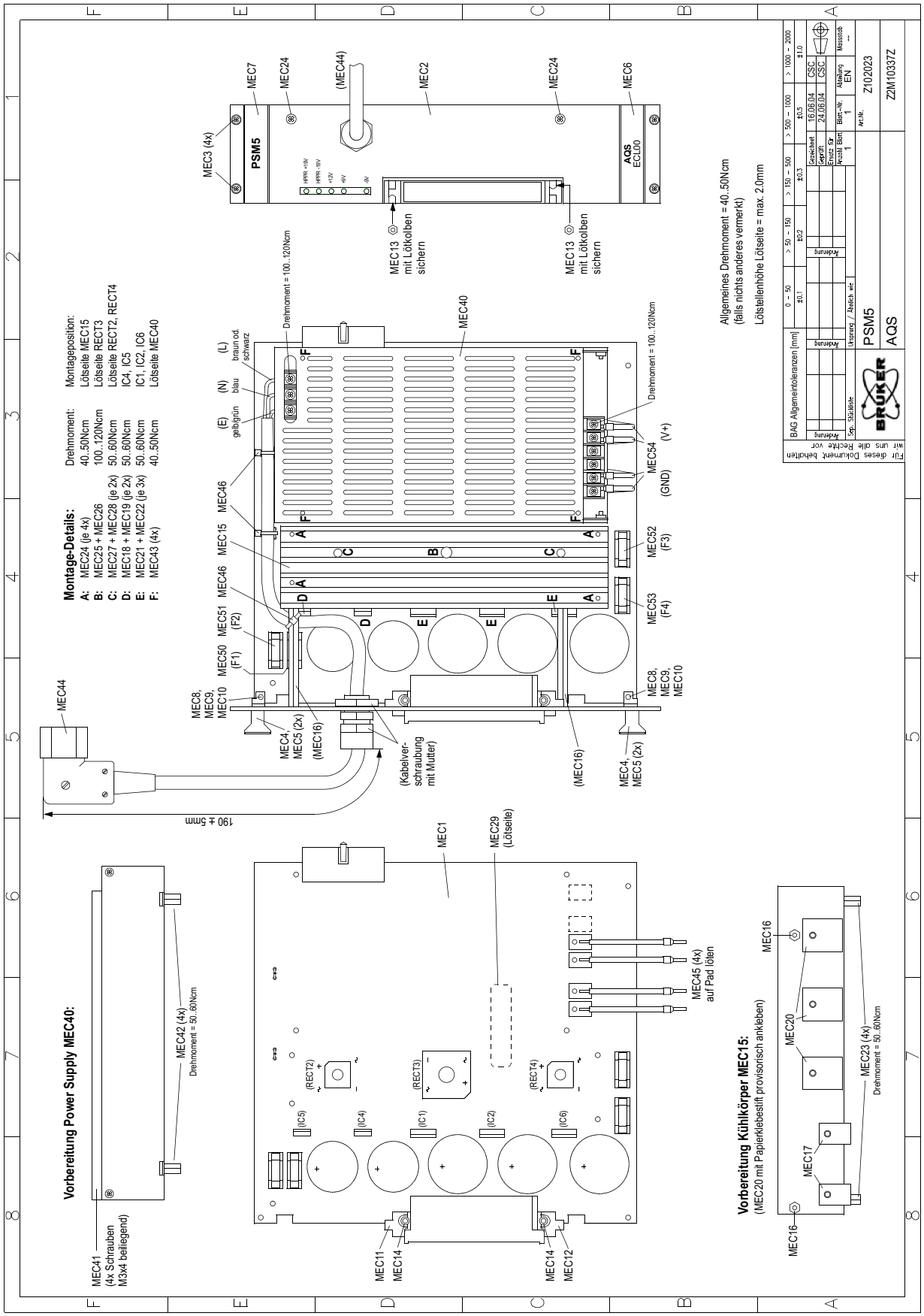


Figure 6.11. Power Supply Module 1-3 Block Diagram

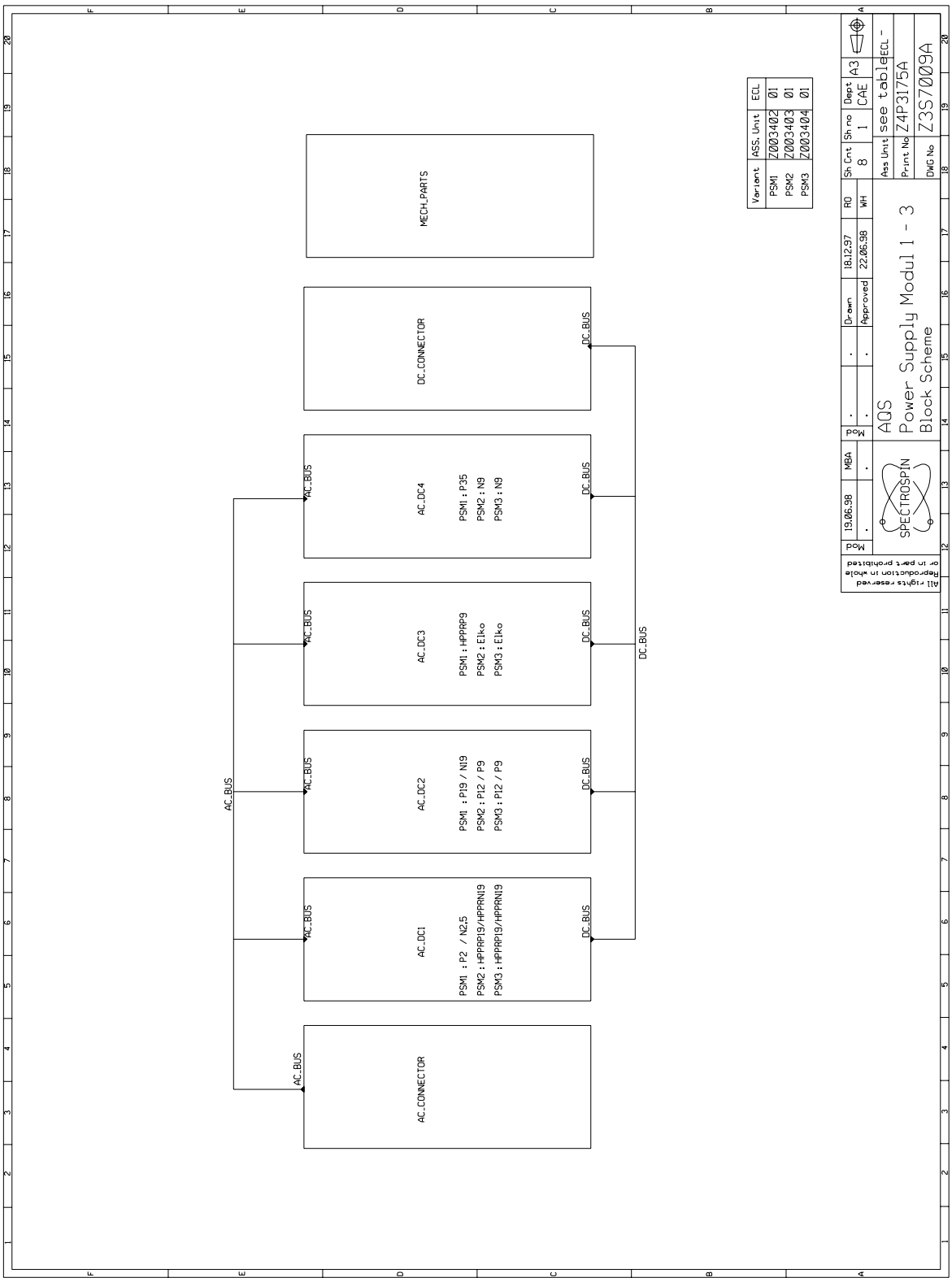


Figure 6.12. AC Connector

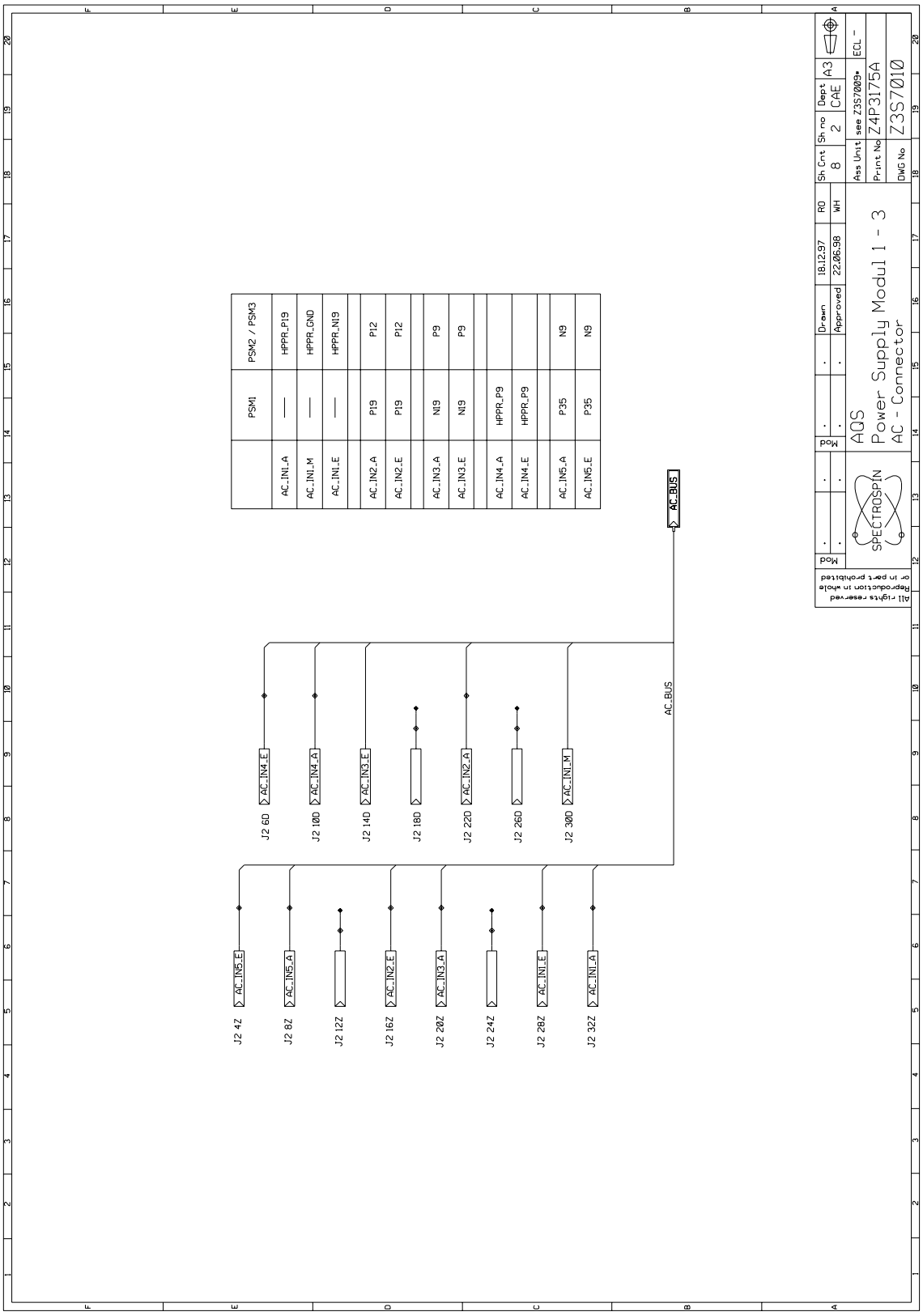


Figure 6.13. Converter AC-DC1

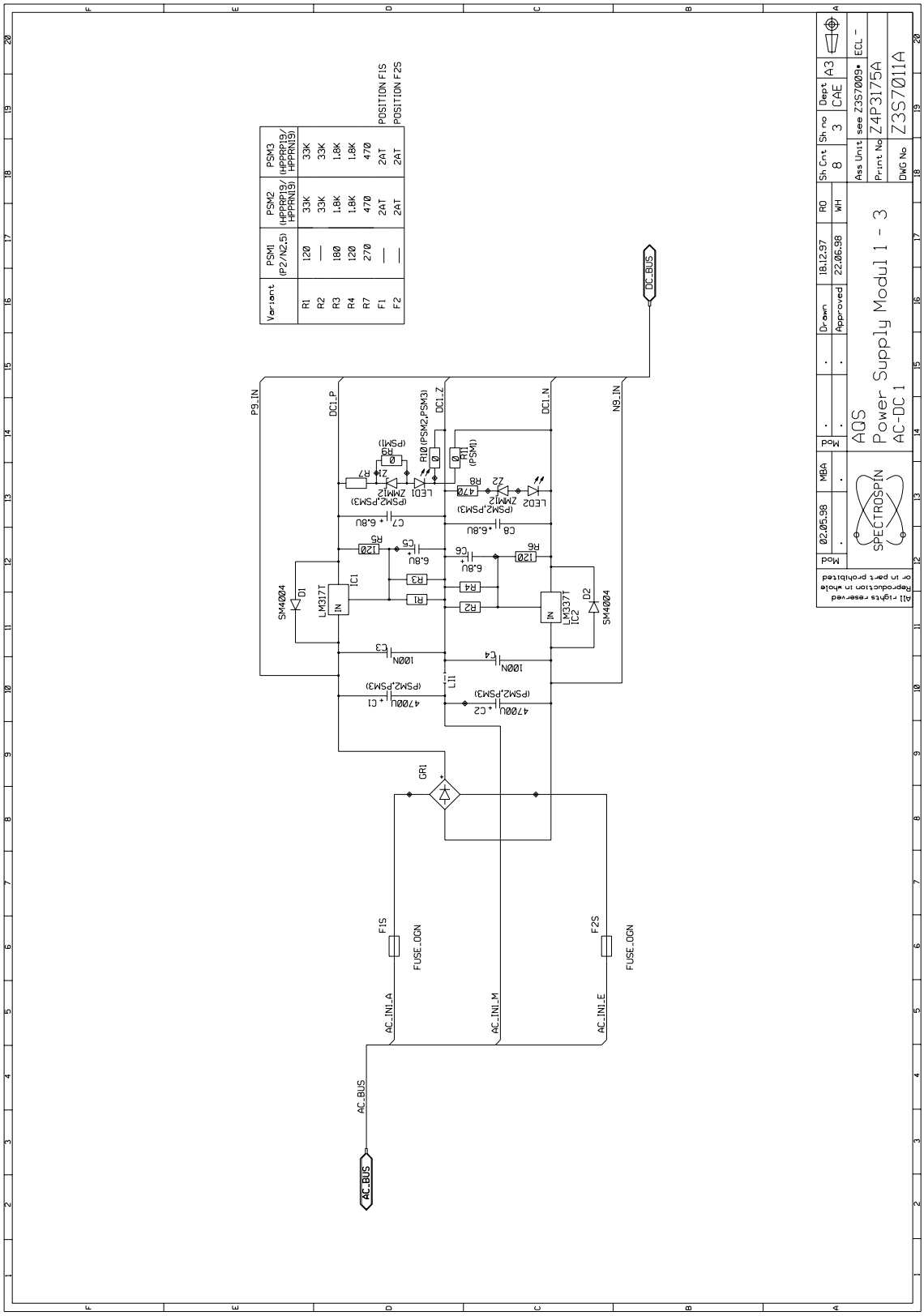


Figure 6.14. Converter AC-DC2

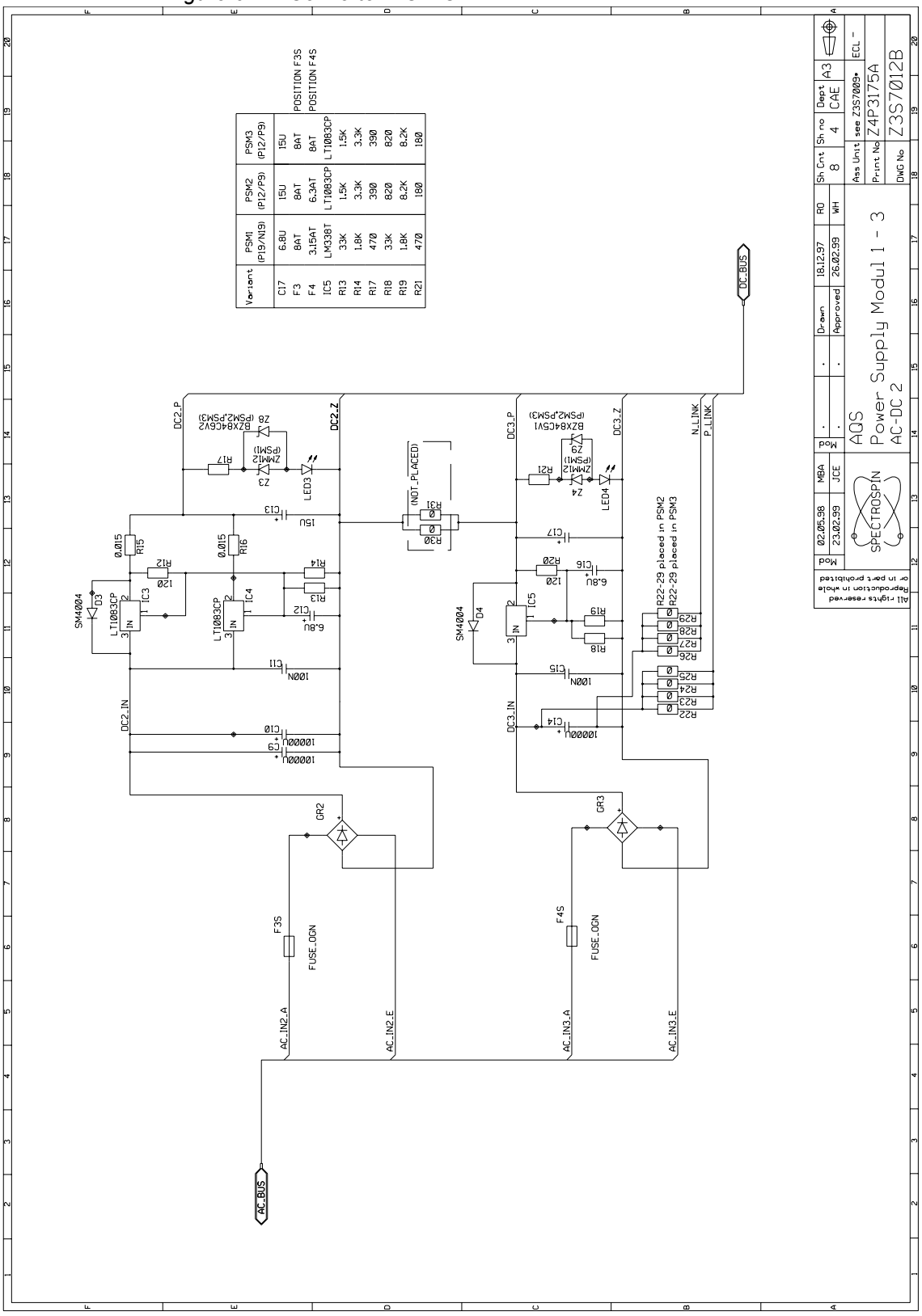


Figure 6.15. Converter AC-DC3

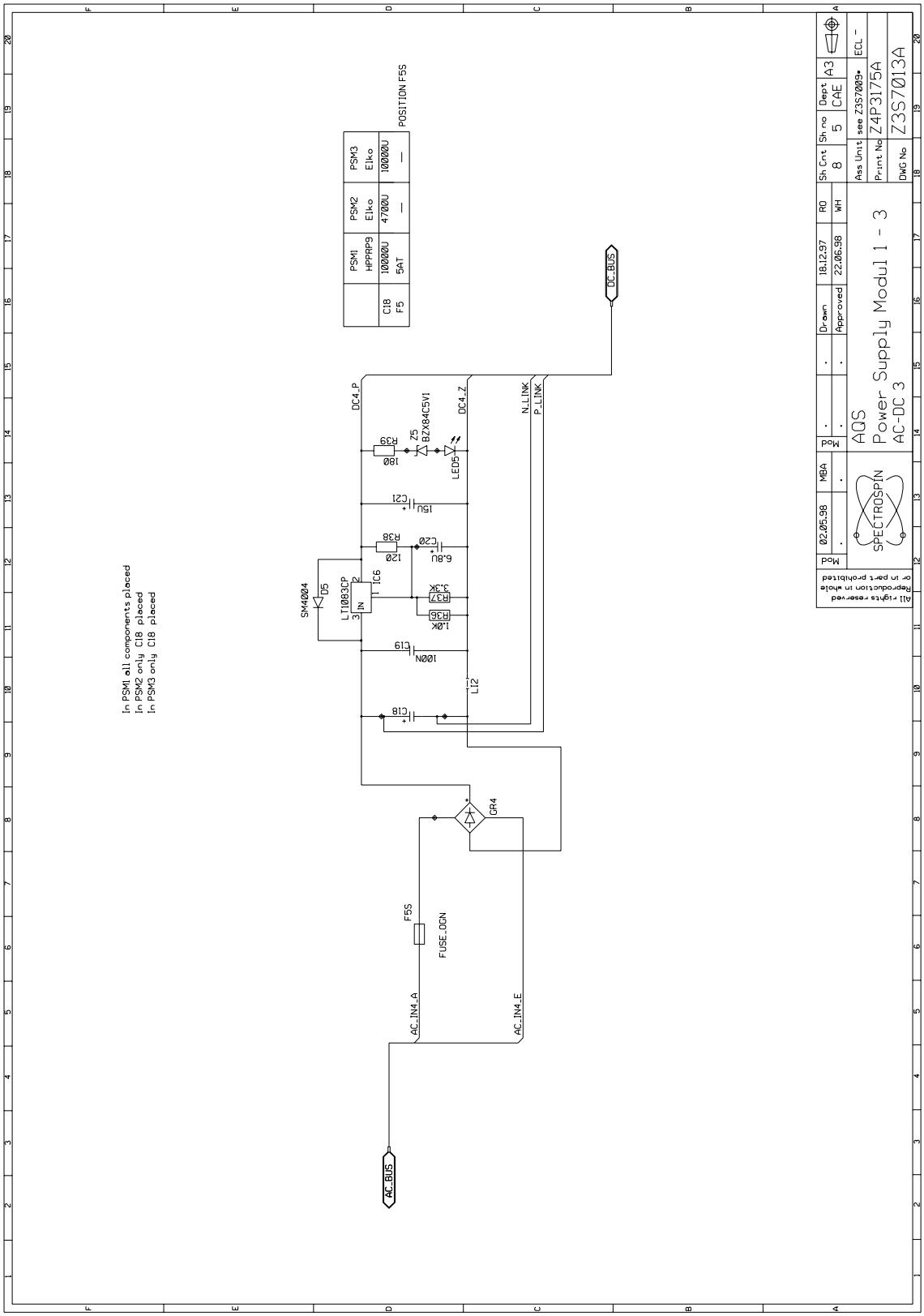


Figure 6.16. Converter AC-DC4

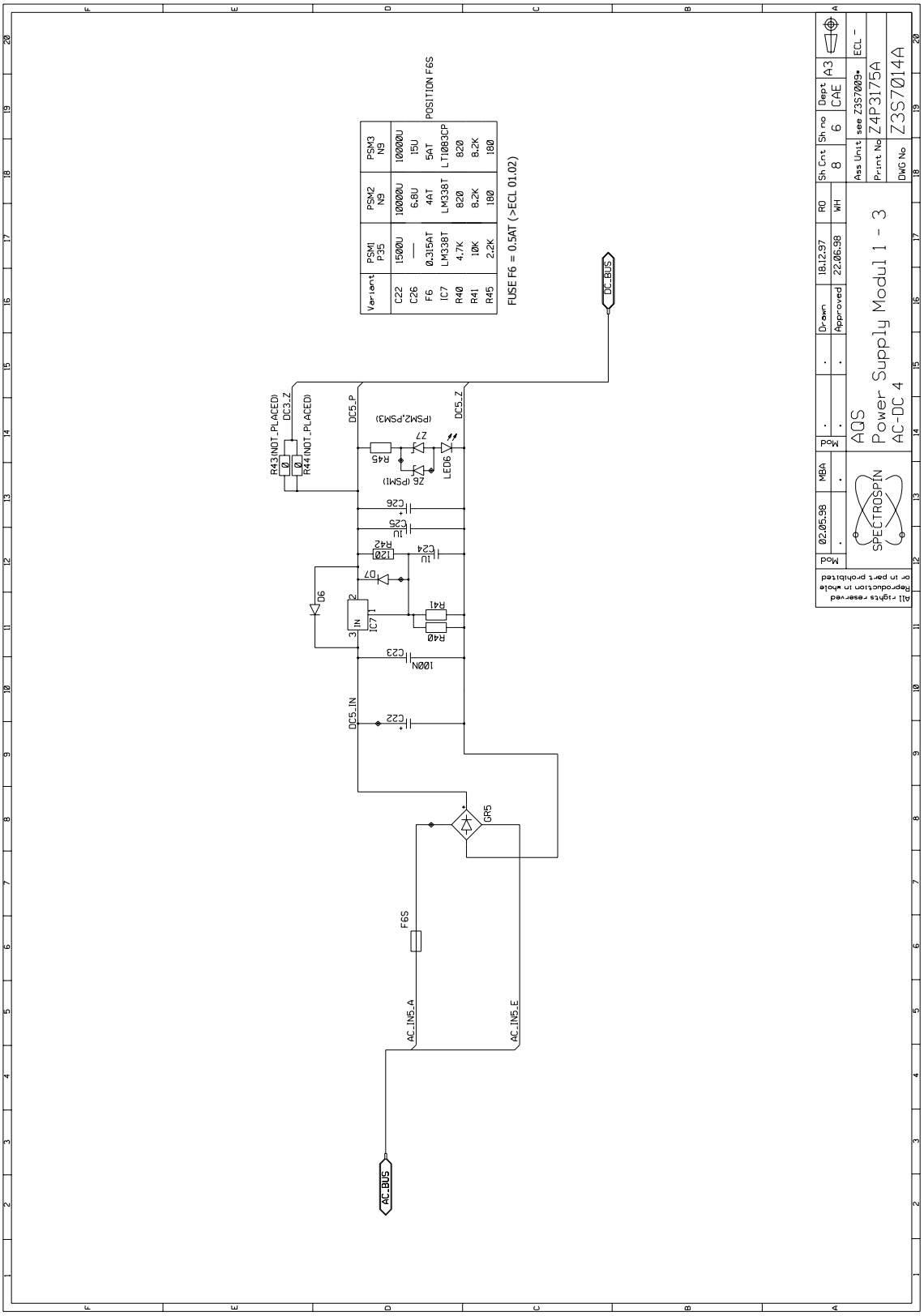


Figure 6.17. DC Connector

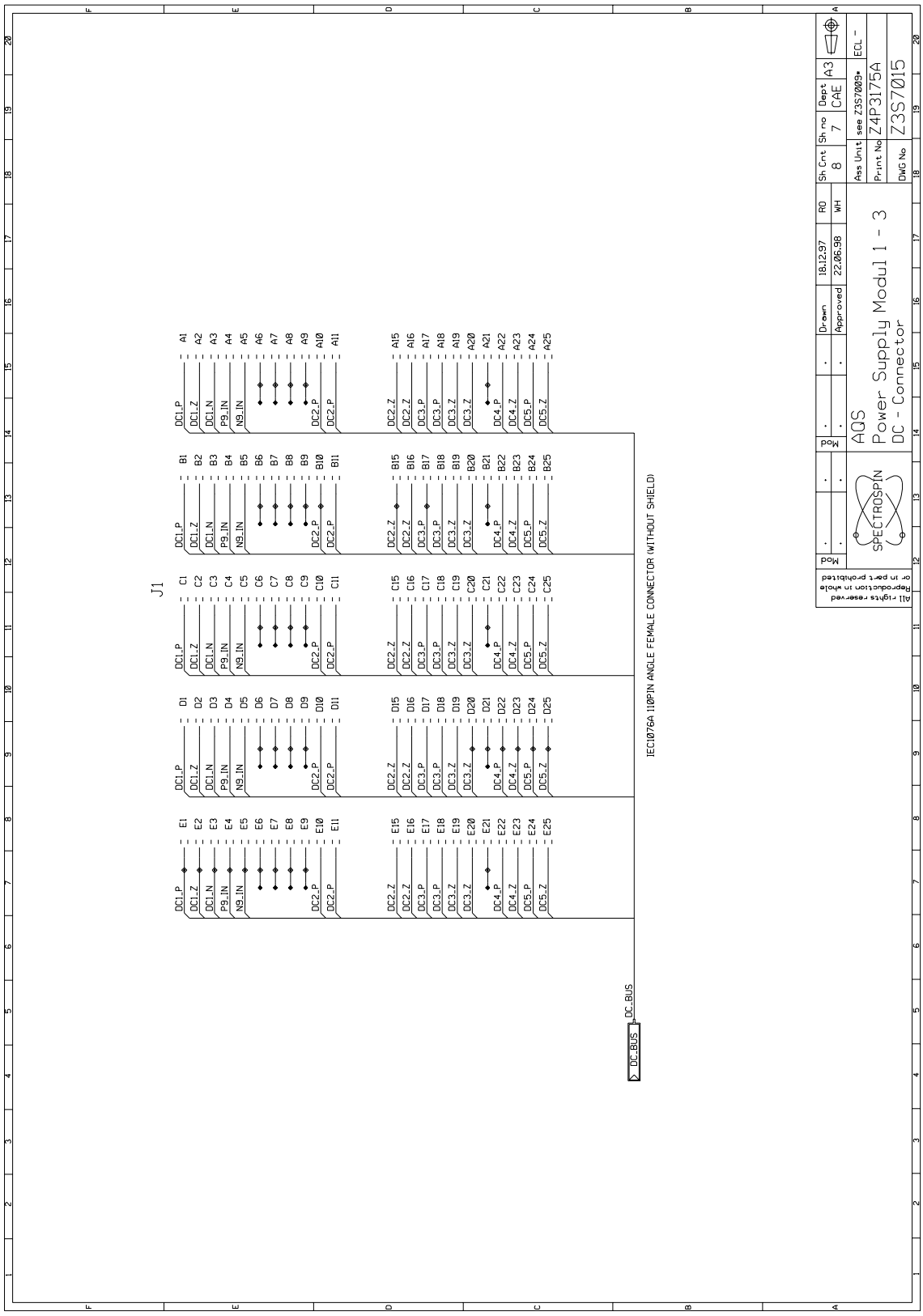


Figure 6.18. Power Supply Module 5 Block Diagram

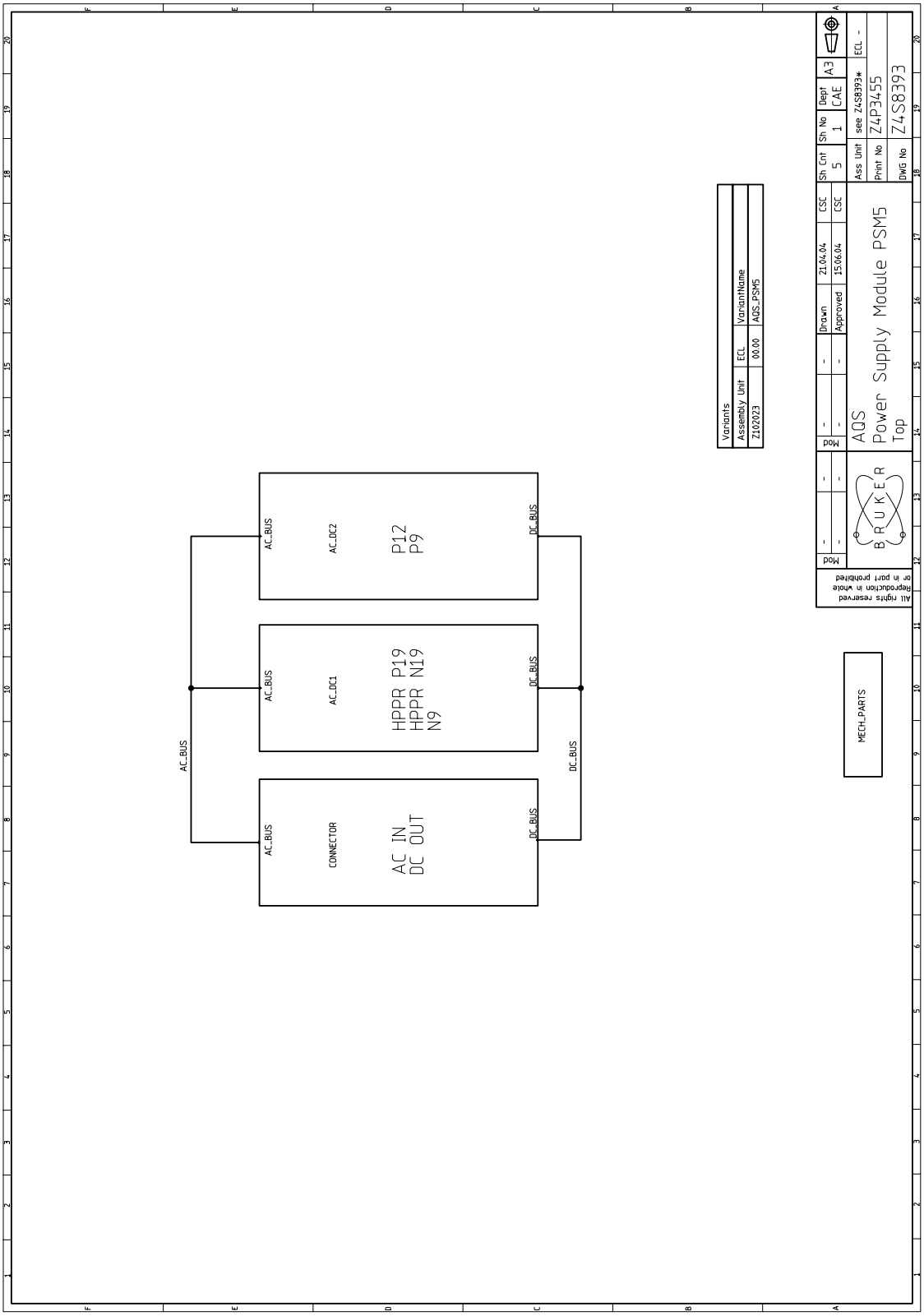


Figure 6.19. Connectors

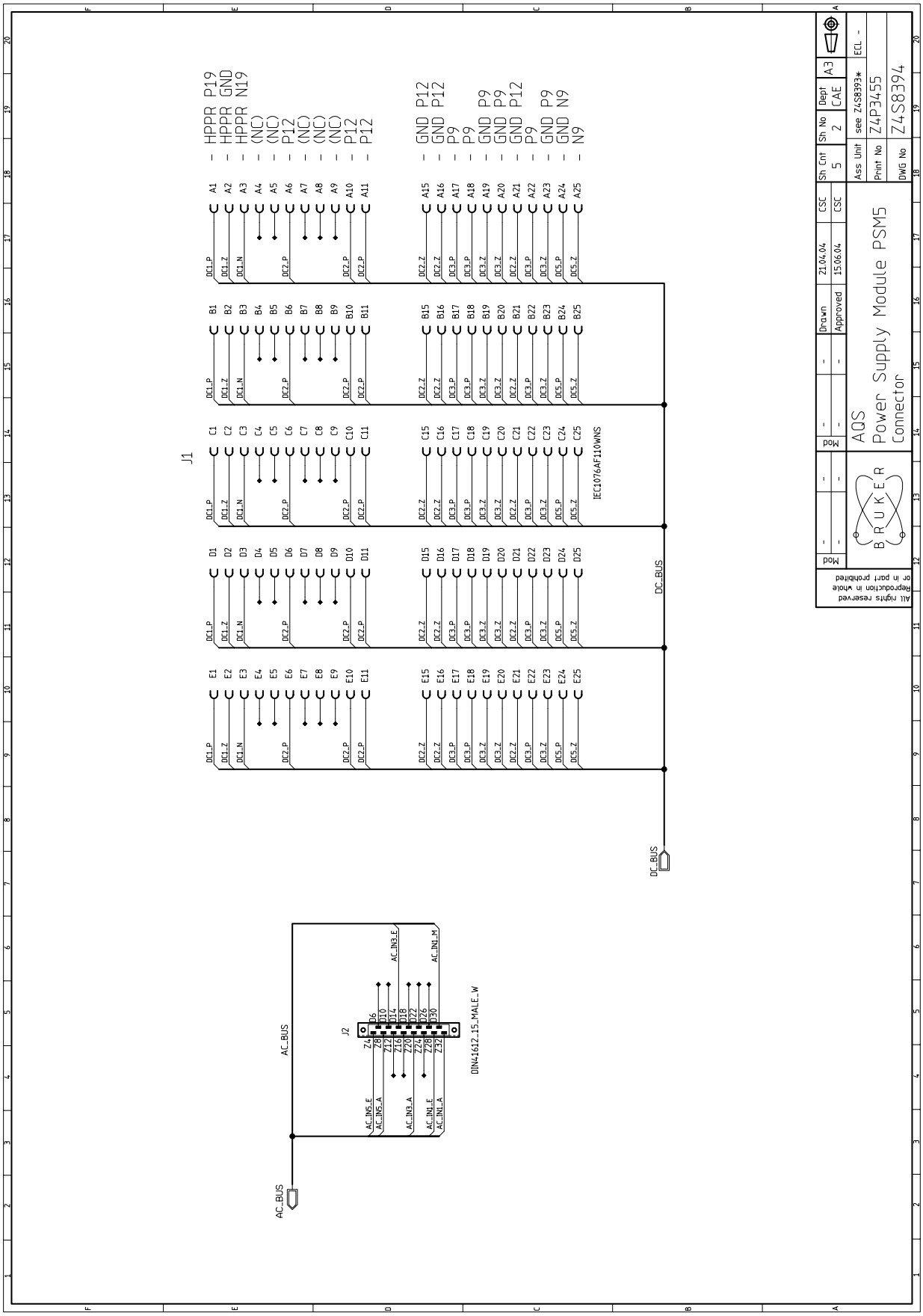


Figure 6.20. Regulators HPPR P19V, HPPR N19V, N9V

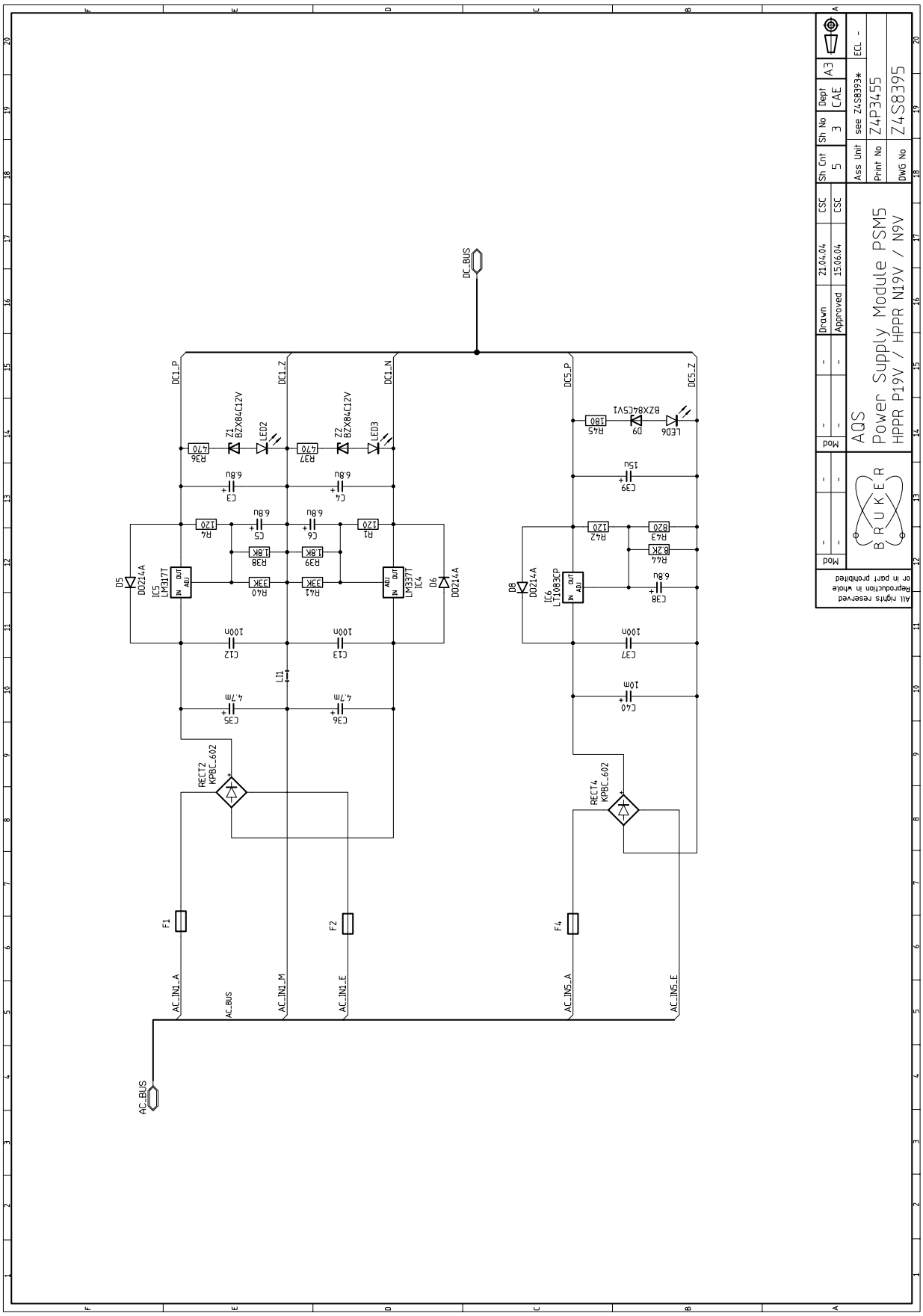
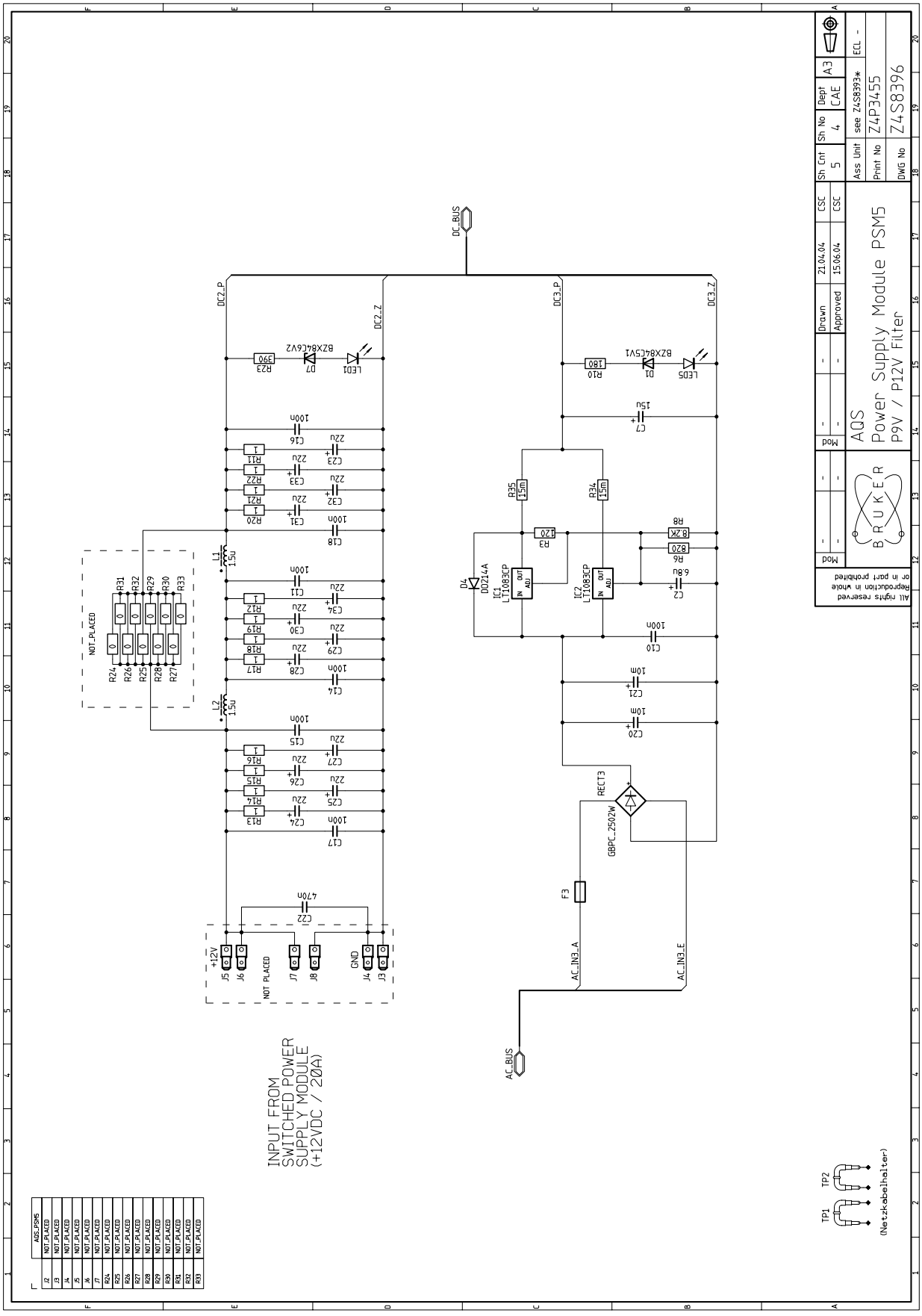


Figure 6.21. Regulator P9V, Switcher Module P12V



AQS Reference Board for RXAD

7

Introduction 7.4

The AQS Reference Board is a new development in the AV series. As spectrometers become more sophisticated the importance of coherence and in particular phase coherence between the various channels as well as between the transmission and receiving paths is more and more important. The philosophy of the AV is to ensure that all RF signals as well as all clocks originate from one source. This source is a temperature controlled crystal oscillator (OCXO) at the heart of the AQS Reference Board. Apart from clock signal each AQS Reference Board will provide the necessary RF signals for up to 4 SGUs. This is to enable the SGU generate frequencies using a so called up converter. The Reference Board REF/2 unit allows (in addition with two BB-splitter) to supply 6 SGUs. If more channels are required then a second AQS Reference Board will need to be installed. The location of the AQS Reference Board will depend on the configuration. Technically it can be placed in the slots 3 to 5. Standard configurations have placed it in slot 3 immediately to the right of the RXAD.

Functions/ Description 7.5

The Reference Board is responsible for the synchronization through the generation of various frequencies. Specifically the generated signals are:

1. Detection reference frequency (LO2 = 720 MHz) for the receiver. There are four versions of the AQS Reference Board that supports the AQS RX-BB or RXAD series (AQS REFERENCE 400, AQS REFERENCE 600, AQS REFERENCE 1000 and AQS REFERENCE/2 1000).

2. 20 MHz synchronization clock for all SGUs, FCU, TCU, user backplane

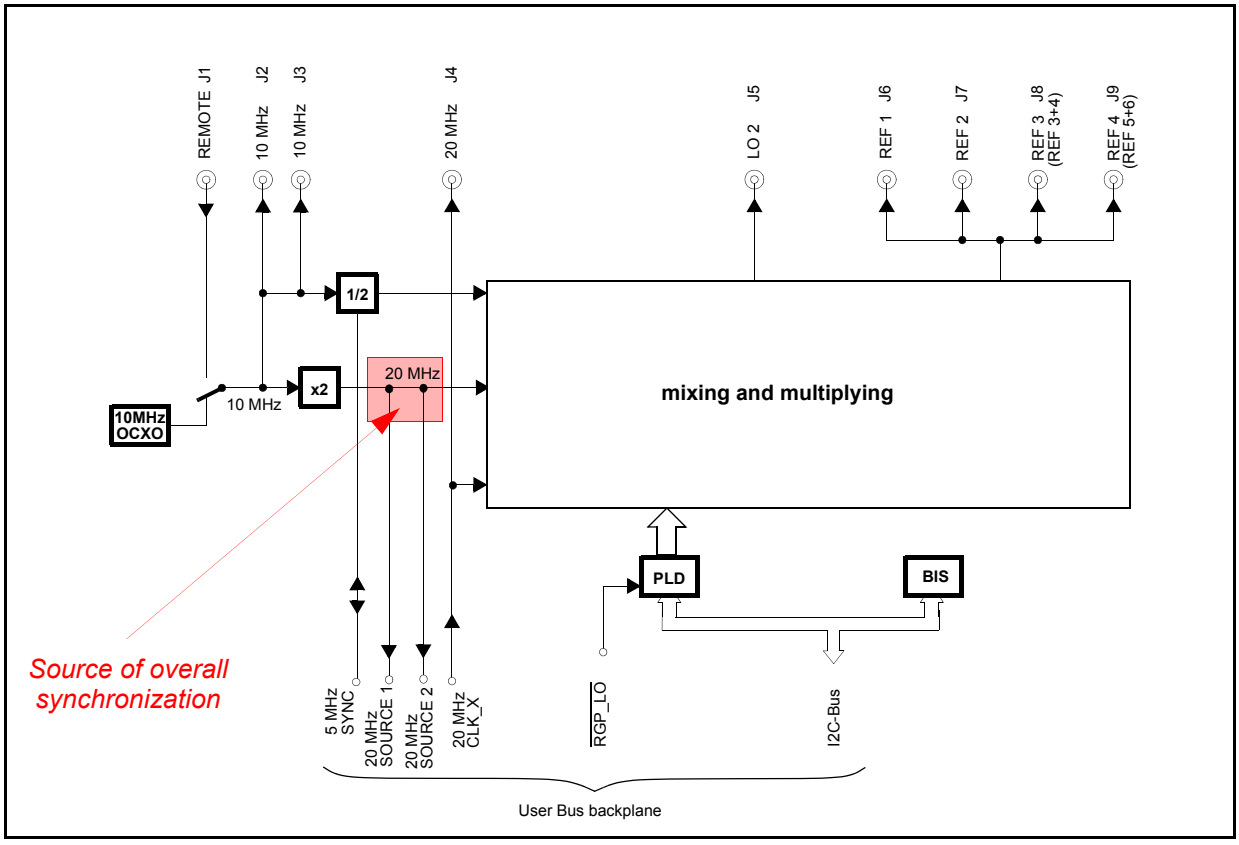
3. auxiliary signals (frequency mixture) for up to four SGUs (six for REF/2)

4. 10 MHz signal for the BSMS LTX

At the heart of the AQS Reference Board is a 10 MHz oven controlled oscillator (OCXO) see ***Figure 7.22.***. The 10 MHz signal for the BSMS LTX is ported directly through connector J2. This signal is mixed and multiplied and afterwards ported to the four REF outputs (J6-J9).

The detection reference frequency (LO2 = 720 MHz) for the AQS RX family of receivers is derived from the 10 MHz OCXO and ported to the J5.

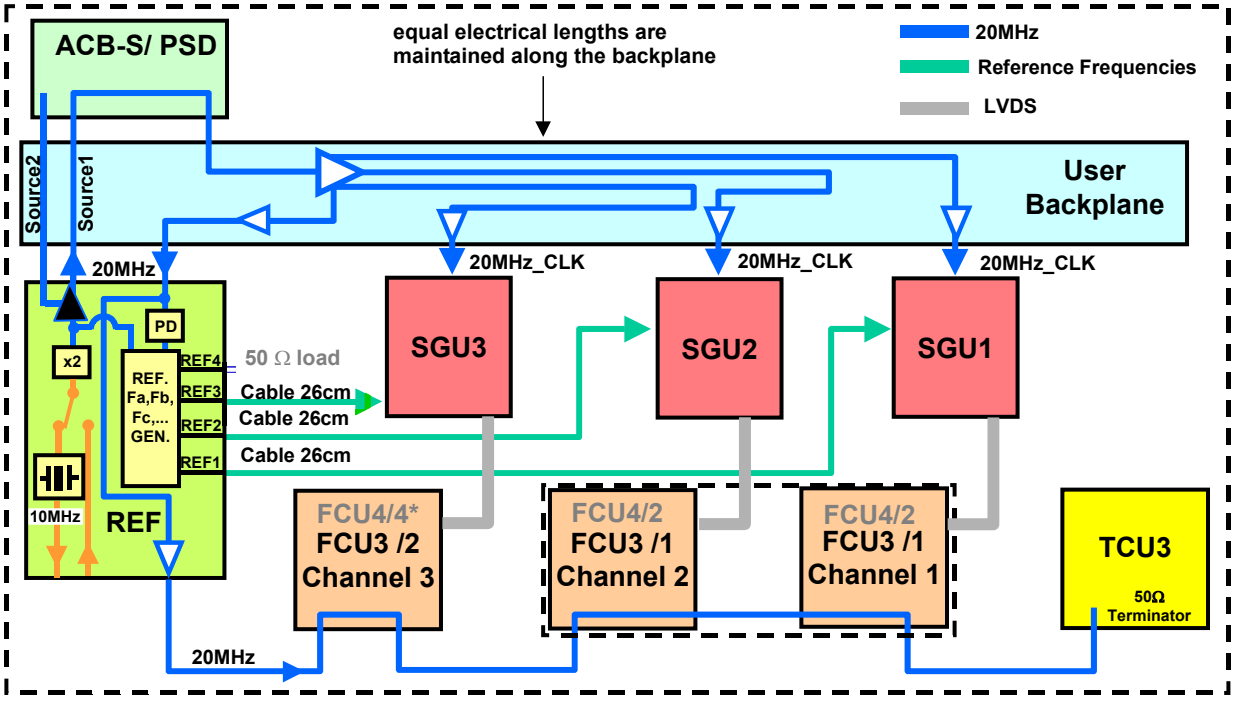
Figure 7.22. Block diagram of AQS Reference Board



Overall synchronization *7.5.1*

The overall synchronization is achieved using the 20 MHz signal generated at the first frequency doubler which is transmitted to the backplane by an ECL signal (20MHZ SOURCE1 and 2). This is then transformed into a differential clock signal (20MHZ_CLK_X / 20MHZ_CLK_X) used to clock all slots of the user bus, which will of course include the SGUs. The same 20 MHz clock is returned and is ported out via J4 and used to clock the GCU, FCUs and the TCU chain. Essentially all clocking frequencies in both the analog and digital sections of the AQS are synchronized with the 20 MHz clock of the AQS Reference Board.

Figure 7.23. Overall synchronization of spectrometer for single AQS rack



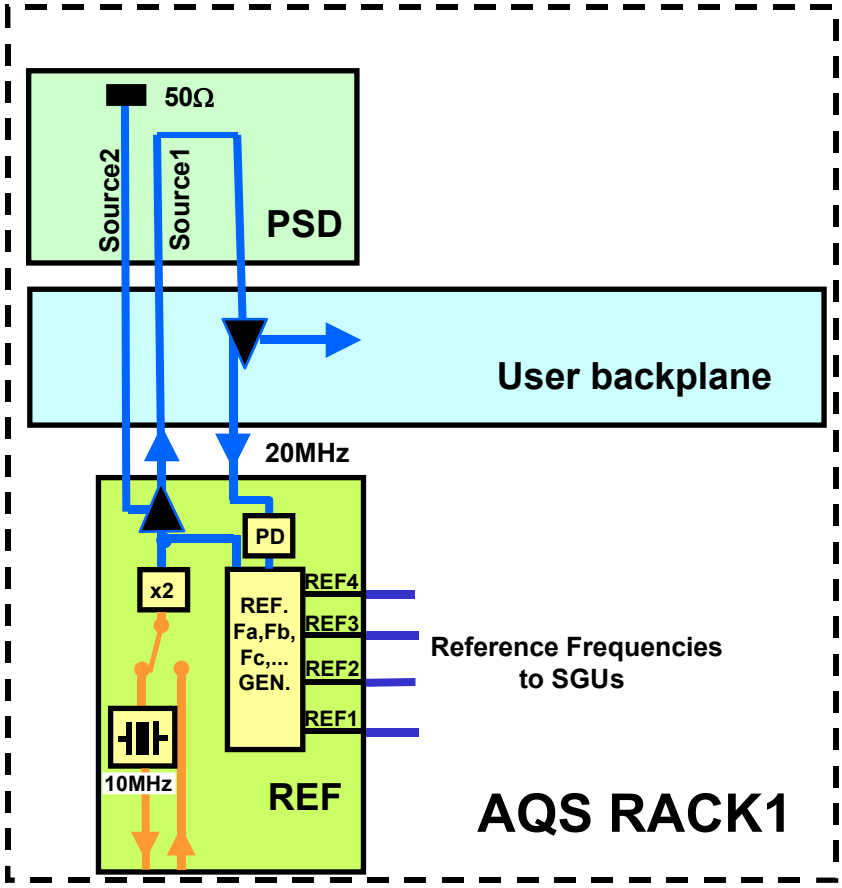
*** in case of 3 channels, a single FCU4/4 is used for all channels**

Synchronization between two AQS racks

To ensure that two AQS racks can be synchronous two (identical) 20 MHz signals (source1, source2) are used to generate the clock. The cable is extended to ensure that the total length is 895cm (earlier versions 155cm), see ***Figure 7.25. on page 159***.

In the case of a single AQS rack, the 20 MHz signal (Source2) is not required and is terminated on the PSD or ACB-S, and the 20 MHz signal (Source1) is used for the AQS user bus slots.

Figure 7.24. Single rack synchronization



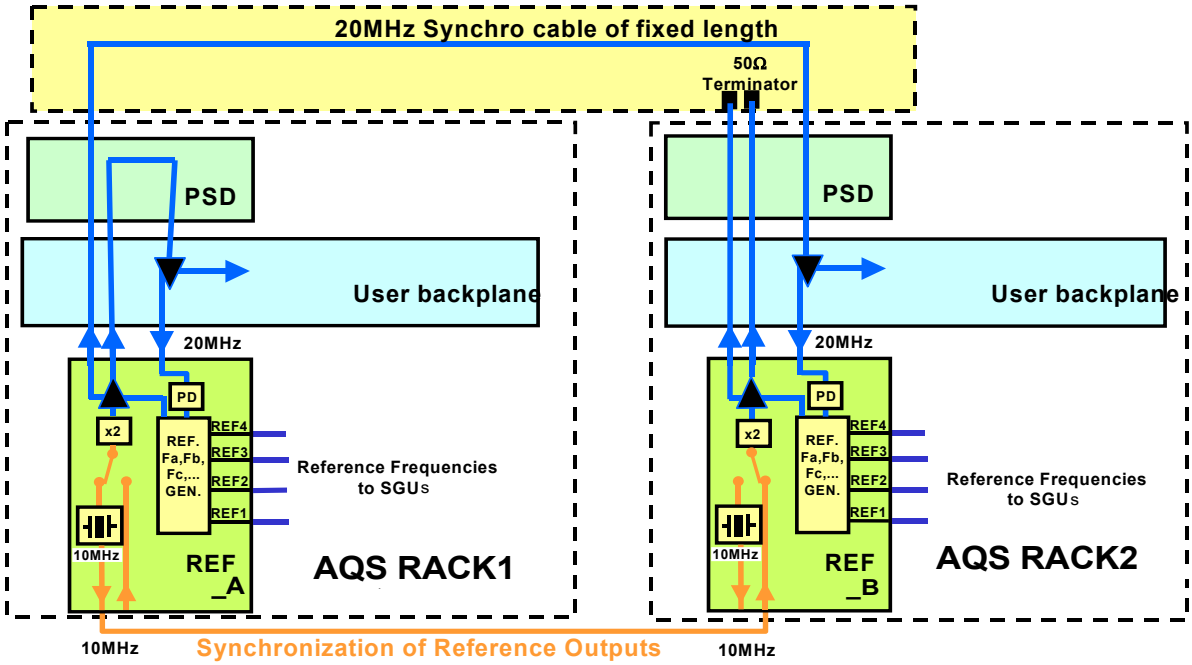
In the case of two AQS racks the two AQS Reference Boards must first be synchronized with each other. This will enable up to 8 SGUs to be synchronized. The 10 MHz out J3 of the AQS Reference Board in rack 1 (REF_A) is connected to the Remote J1 of the AQS Reference Board in rack 2 (REF_B). This signal will automatically replace the oscillator in REF_B. Both units have then essentially the same oscillator. With two AQS Reference Boards there are potential 4 sources for the 20 MHz clock. How they are used is explained in the table below.

Table 7.7. Synchronization with two AQS Reference Boards.

Signal	use
REF_A source1	used to clock AQS1
REF_A source2	used to clock AQS2
REF_B source1	not used. Terminated at PSD board
REF_B source2	not used. Terminated at PSD board

Essentially in a two rack system AQS Reference Board in rack 1 (REF_A) is used to clock both racks. The second Reference Board (REF_B) is only required to provide the RF frequency mixtures for SGU 5/6/7/8.

Figure 7.25. Double rack synchronization



Cable lengths 7.5.2

To maintain this synchronization particularly with respect to phase all signals should pass through identical electronic circuitry as well as cables of equal length. The circuitry along the user backplane is designed to ensure equal electrical lengths regardless of the physical slot occupied by an SGU.

If cables are to be replaced then the same length cable should be used. For example the cables carrying the mixture of 6 frequencies to the SGUs are a standard length of 26cm. Similarly the cables carrying the 20 MHz clock signal need to be the same length. To maintain this equal length it will be noticed that extra cable length is connected at the first PSD unit. This is to equalize the cable for PSD1 and PSD2.

Bus interfaces 7.5.3

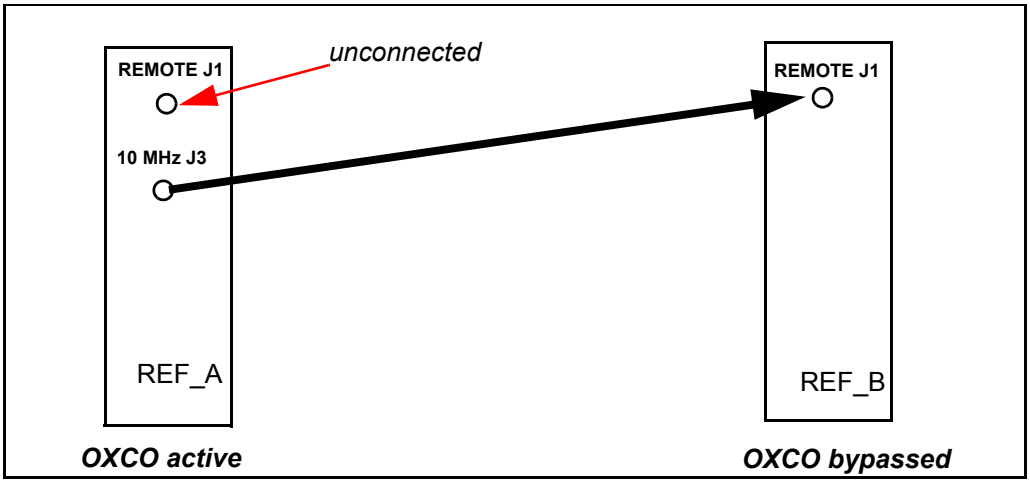
The AQS Reference Board is controlled by the I^2C bus on the backplane. This bus is used to

1. read the BIS data (Bruker information system, successor to BBIS)
2. allow the master SGU load settings which are stored in an FPGA (field programmable gate array) on-board into DACs to control the REF signal output.

Unit Configuration / Version / Jumpers 7.6

The unit is automatically configured through the ‘cf’ routine. No jumper settings are required. The distinction between AQS Reference Board in rack 1 (REF_A) and AQS Reference Board in rack 2 (REF_B) depends entirely on the presence of the J1 REMOTE input signal. This signal is connected only for REF_B.

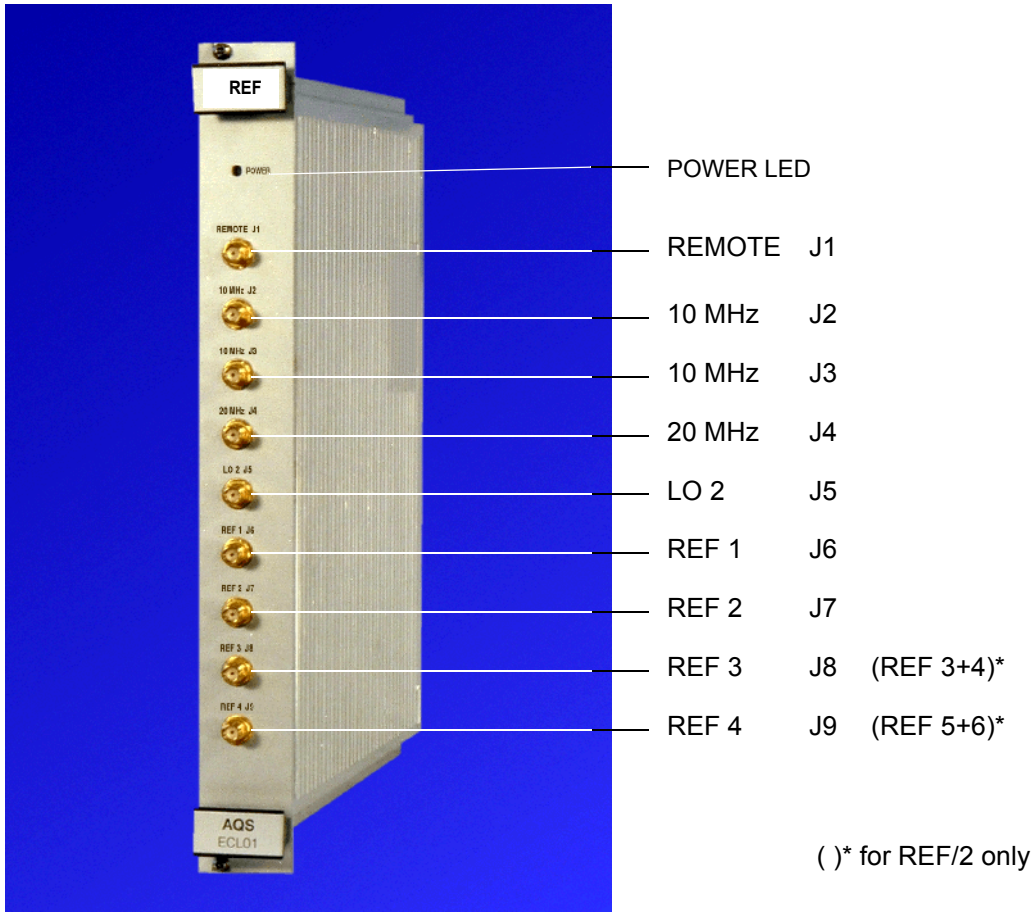
Figure 7.26. Synchronization of REF2 by REF1.



Differences from previous versions. 7.6.4

This is a totally new development for the AV series and the AQS Reference Board does not have a counterpart in the AVANCE series.

Figure 7.27. AQS Reference Board front panel



J1 REMOTE IN

Sinusoidal input for external 10 MHz clock and must have a power level in the range 6...13 dBm @ 50 Ω. The presence of this signal will automatically switch off the internal 10 MHz clock generated by the crystal oscillator. This is normally not connected except when a second AQS Reference Board is synchronized with the first.

J2 10 MHz OUT

Output to BSMS L-TX J2, used to clock BSMS Lock Transmitter board. Sinusoidal wave approx. 7 dBm (1.4 Vpp) @ 50 Ω

J3 10 MHz OUT

Output for synchronization with second AQS Reference Board. Sinusoidal wave approx. 7 dBm (1.4 Vpp) @ 50 Ω

J4 20 MHz OUT

Clock signal to TCU/FCUs, ECL (emitter coupled logic) square wave approx. ±1 Vpp @ 50 Ω. This is the principal synchronization signal for the spectrometer.

J5 LO 2 OUT

Receiver detection reference to AQS RX J3, 720 MHz approx. 4 dBm (1.0 Vpp) @ 50 Ω

J6 - J9 REF 1-4 OUT

Frequency mixture to SGUs. 2.2 Vpp @ 50 Ω, all variants except REF/2 at J8 and J9
Frequency mixture to BB-SPLITTER. 4.4 Vpp @ 50 Ω, for variant REF/2 at J8 and J9

POWER LED

See ***"Power Supply / Fuses" on page 163***

Part Numbers and Cables *7.8*

Four versions of AQS Reference Boards are available. They differ for the maximum NMR frequency up to 400, 600 or 1000 MHz and for the number of SGUs.

For 4 SGUs:

- AQS REFERENCE BOARD 400, P/N Z003265
- AQS REFERENCE BOARD 600, P/N Z003936
- AQS REFERENCE BOARD 1000, P/N Z003937

For 6 SGUs with BB SPLITTERs on J8 and J9:

- AQS REFERENCE BOARD/2 1000, P/N Z104236

Troubleshooting / Unit replacement / Tips 'n' Tricks *7.9*

1. Terminate any unused outputs with 50Ω.
2. If you suspect the OCXO is faulty switch to an external 10 MHz signal (> 4 dBm resp. 1 Vpp @ 50 Ω) by applying it to REMOTE J1.
3. Ensure that any unused REF outputs (J6-J9) are properly terminated with a 50 Ω connector.

Diagnostic Tests *7.10*

Not applicable.

Specifications *7.11*

The principal specification is that of the stability of the crystal oscillator which is specified to:

1 x 10^{-9}/day on REF 1000 and REF/2 1000
3 x 10^{-8} total deviation for REF 600
2 x 10^{-9}/day on Ref 400

Power Supply / Fuses *7.12*

The Reference Board uses +5 V, +12 V, ±9 V, +19 V from the backplane see ***"Backplane Connector Ref. unit" on page 164***. The power LED on the front panel indicates that all necessary voltages are present and at the correct level. If the voltage level drops then the LED will go out. Thus once the power LED lights then further investigation of the backplane to check the precise voltage is unnecessary.

Backplane Connector *7.12.5*

The table below shows the pin assignment for the middle rear 110 pin connector. Note the presence of the source and clock signals.

Table 7.8. Backplane Connector Ref. unit

	z	a	b	c	d	e	f
1	GND	GND		5MHZ_SYNC	GND		GND
2	GND	20MHZ_SOURCE1	GND				GND
3	GND	GND	20MHZ_SOURCE2		GND		GND
4	GND	20MHZ_CLK_X	GND				GND
5	GND	GND	20MHz_CLK_X		GND	RGP_LO	GND
6	GND		GND				GND
7	GND				GND		GND
8	GND		GND				GND
9	GND				GND		GND
10	GND		GND				GND
11	GND				GND		GND
						23x GND (21%)	
15	GND	SLOT2	SLOT1	SLOT0	GND		GND
16	GND		GND	I2C_SDA		GND	GND
17	GND			I2C_SCL	GND		GND
18	GND		GND			GND	GND
19	GND				GND		GND
20	GND		GND			GND	GND
21	GND	P5V		P9V	P9V	P9V	GND
22	GND	P5V		N9V	N9V	N9V	GND
23	GND	P5V	P19V	N19V	RACK1	P12V	GND
24	GND	P5V	P19V	N19V	RACK2	P12V	GND
25	GND	P5V	P19V	N19V	RACK3	P12V	GND

AQS RXAD 8

Introduction 8.1

The AQS RXAD is a high dynamic range receiver for NMR with integrated analog-to-digital converter (ADC). The AQS RXAD is available for different nuclei ranges (RXAD400, RXAD600, RXAD1000) and also in a broadband version (RXAD-BB). The AQS RXAD is fully integrated in the AQS concept and runs in conjunction with the AQS SGU, AQS REF and AQS DRU. The AQS RXAD is located in the analog section of the AQS rack. The board is physically as long as the other AQS units (REF/SGU/DRU) and attaches to the user bus (backplane) directly.

As the name suggests the AQS RXAD receiver is concerned with the amplification of the signal 'received' from the sample and therefore uses a intermediate frequency that is generated by the input signal and the local oscillator synthesizer signal. In contrast to former receiver types with analog audio frequency output (RX-22, AQS RX-BB) the output signal from the AQS RX*AD* is in a raw digital format already. The integrated high performance ADC combines wide bandwidth with optimal shielding, shorter signals paths (lower EMI sensitivity) and less wiring.

The AQS RXAD has a sufficient gain range to be set in 1 dB steps. The correct setting of the RF gain will ensure that the receiver output is matched to the ADC range.

The entire receiver function is controlled by a microprocessor. This allows accurate gain setting, phase/amplitude and dc offset adjustment in the quadrature-module via a RS485-Interface which runs over the backplane. Calibration and production data (BIS, Bruker Board Information System) are stored in a EEPROM flash on the board.

A vital element of any RF receiver is the quality of the shielding to maximize the suppression of noise. In the design of this unit special attention has been paid to good clean signal transmission etc. The AQS RXAD is mounted in a 19" RF cassette type case, the quadrature module is temperature stabilized separately.

All communication with the AQS RXAD take place using the SBSB1 link along the backplane. This enables the application of the UniTool which is a software diagnostic tool and is also used for accessing other devices like SGU or HPPR/2.

In contrast to the RX22, the AQS RXAD is also initialized and supervised by the AQS controller (DRU or SGU) using the separate internal RS485 bus on the AQS User Bus.

In multi receiver systems each channel is equipped with a separate AQS RXAD and DRU and its SGU for LO (local oscillator) signal generation.

Functions/Description *8.2*

The AQS RXAD has four main functions, which are to amplify the signal from the sample/HPPR, to down convert it, to match the input range of the ADC and digitize the quadrature signal. The vital elements of this are the linear amplification of all frequencies as well as to guarantee the precise phase relationship of all RF signals.

The RF input is amplified in several stages to increase the dynamic range. The current LO frequency for the first mixer stage is generated in the LO frequency synthesizer.

At the final section the IF signal is split into two channels with phase difference of 90 degrees, a standard method well known as quadrature detection. In order to ensure that the two channels provide identical amplification, slight adjustment to the phase and gain of these channels may be necessary. This can be done via UniTool. Channel A and B are connected directly to the integrated ADC.

The integrated ADC converts the quadrature signal at a very high sampling rate and transmits the data to the AQS DRU over a high speed data link on the backplane.

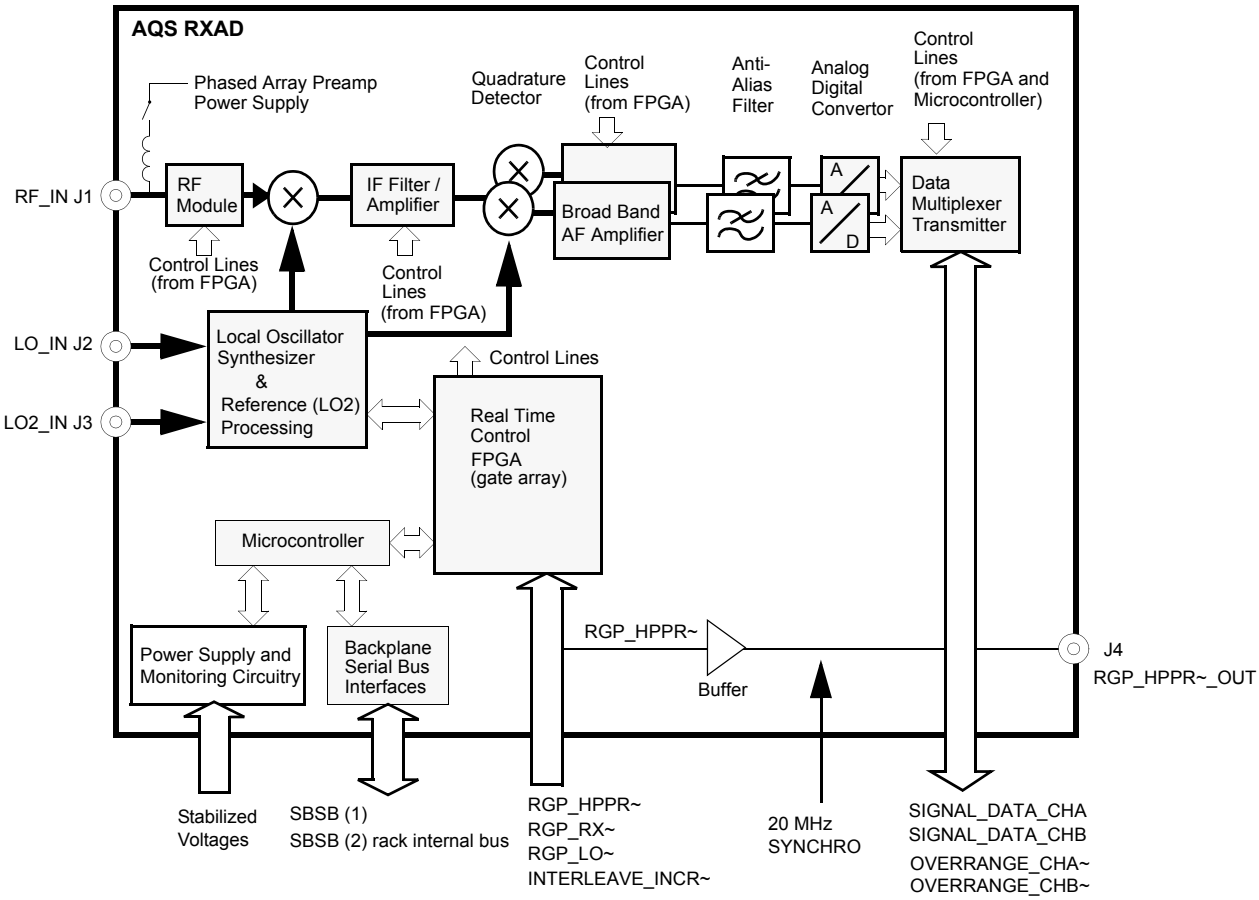
DC offset is pre-adjusted for proper control of the ADC input range and can be fine-adjusted using UniTool. The adjusted values can be saved in the on-board non-volatile memory.

During acquisition full control of the RXAD sections (gain, frequency, sampling etc.) is maintained by two complex FPGA (field programmable gate array) that handles the real-time behavior. The FPGA real-time circuitry is controlled by external gating and pulse signals from the backplane (AQS/2 User Bus). Control information is passed on from TCU, FCU and the actual Observe-SGU in order to the channel concept.

The on-board microcontroller is used for initialization and RS485 communication.

For multi receiver systems with several preamplifiers, the gating pulse for the HPPR (RGP_HPPR~) from the backplane is buffered and is fed separately to the front panel of the AQS RXAD (RGP_HPPR~_OUT J4).

Figure 8.1. RXAD-Blockdiagram



Power Supply and Monitoring *8.2.1*

All voltages supplied from the backplane are filtered and stabilized on the RXAD. Operation of the *on-board* power stabilization is monitored and indicated by the green LED on the front labeled POWER. If one of the AQS power supply voltages used by the AQS RXAD fails the monitoring circuit will turn the LED off.

Reset *8.2.2*

The AQS RXAD controller is normally in sleep mode (reset state) to prevent disturbance and spikes in the spectra. The 20 MHz microprocessor clocking frequency is also switched off. The controller will be restarted each time a communication via the RS485 is opened (TOPSPIN or UniTool).

The controller will be active during acquisition only in the following cases:

- ‚gs'-mode operation (which is typically used to adjust parameters dynamically) and
- at the beginning of wobble and receiver gain adjustment (rga)

This state is indicated by a ***blinking*** red LED labeled ERROR while the green LED labeled READY ***remains on***.

The AQS RXAD is mainly controlled from the backplane by the following pulses

- RGP_LO~
- RGP_RX~
- INTERLEAVE_INCR~

RGP_LO~

The RGP_LO~ pulse indicates that the LO signal from the SGU is available and so the LO synthesizer of the AQS RXAD can synchronize. If there is a RPG_LO~ pulse and no appropriate LO signal (defective cable, not connected, wrong setting of SGU) an error message will appear.

RGP_RX~

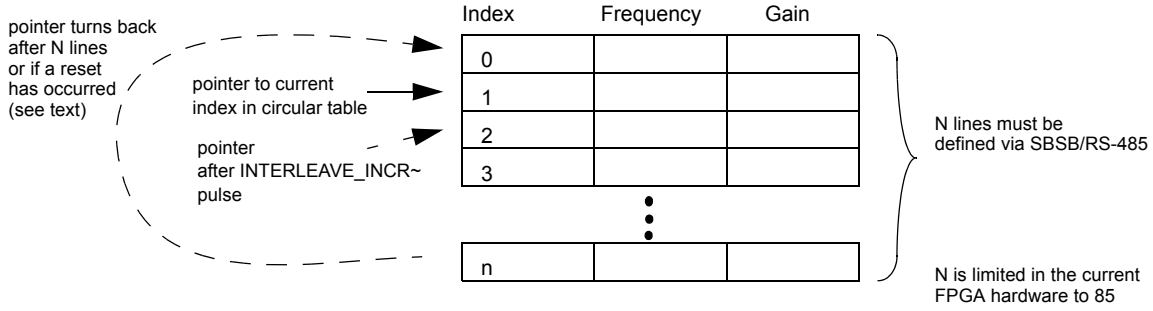
The RGP_RX~ pulse opens the receiver after excitation and prevents saturation of the input stage while transmitters are switched on. An RGP_RX~ pulse occurrence while the on-board microcontroller is running will also lead to an error message (except in ‚gs'-mode operation) because microcontroller circuitry noise might affect the spectral purity of the RF signals.

INTERLEAVE_INCR~

The receiver is prepared for pre-loading a table of different frequency/gain pairs. An INTERLEAVE_INCR~ pulse selects the next line of the table.

This concept is used for wobble, interleaved acquisition experiments and fast receiver gain ('rg') switching.

Figure 8.2. Circular Table: Mode of operation



*For **RXAD1000** ECL02.00 or newer and **RXAD-BB** ECL03.00 or newer:*

The pointer in the circular table resets to index 0 if a long (≥ 4 μs) INTERLEAVE_INCR~ pulse has occurred. A short pulse (≤ 1 μs) selects the next line of the table.

Effective Gain of the AQS RXAD *8.2.4*

Table 8.1. Possible gain steps of the AQS RXAD

Receiver Gain 'rg'	Equivalent RX-BB/RX-22 Voltage Gain [dB] $20*\log([V_{HR_OUT}/V_{RF_IN}])$
2050	78
1820	77
1620	76
1440	75
1150	73
1030	72
912	71
812	70
724	69
645	68
575	67
512	66
456	65
406	64
362	63
322	62
287	61
256	60
228	59
203	58
181	57
161	56
144	55
128	54
114	53
101	52

Receiver Gain 'rg'	Equivalent RX-BB/RX-22 Voltage Gain [dB] $20*\log([V_{HR_OUT}/V_{RF_IN}])$
90.5	51
80.6	50
71.8	49
64.0	48
57.0	47
50.8	46
45.2	45
40.3	44
36.0	43
32.0	42
28.5	41
25.4	40
22.6	39
20.2	38
18.0	37
16.0	36
14.2	35
12.7	34
11.3	33
10.0	32
9.00	31
8.00	30
7.12	29
6.35	28
5.60	27
5.00	26

Receiver Gain 'rg'	Equivalent RX-BB/RX-22 Voltage Gain [dB] $20*\log([V_{HR_OUT}/V_{RF_IN}])$
4.50	25
4.00	24
3.56	23
3.20	22
2.80	21
2.56	20
2.25	19
2.00	18
1.78	17
1.60	16
1.40	15
1.28	14
1.12	13
1.00	12
0.89	11
0.80	10
0.70	9
0.64	8
0.56	7
0.50	6
0.44	5
0.40	4
0.35	3
0.32	2
0.28	1
0.25	0

Unit Configuration / Version / Jumpers *8.3*

There are four versions of RXAD available (see ***"Part Numbers" on page 173***).

Key specifications and digital control behavior remain the same for all versions.

There are no jumpers or manual switches to set.

Through the ‘cf’ routine the number and location of all installed RXADs is determined. In multi receiver systems each RXAD in the AQS chassis has a unique address derived from its physical position.

Differences to previous receiver versions *8.3.1*

The AQS RXAD is different from the RX22 in many ways:

- very low dead-time to switch on receiving (RXAD-BB)
- matching AQS reference unit necessary
- broadband suitability (RXAD-BB)
- service access with UniTool instead of RX22 Tool

For solids experiments, the AQS RXAD-BB replaced the SE-451 system:

- now more than 3 channels available
- phase modulation with SGU
- integrated in AQS concept

The difference to AQS RX in AV systems with RCU:

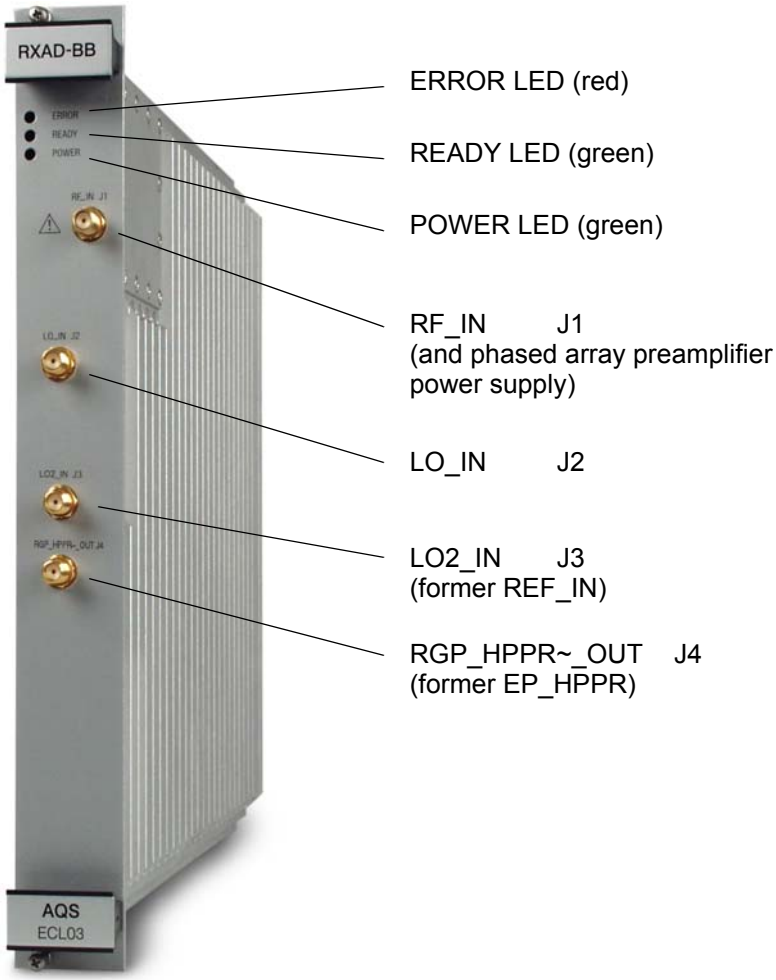
- Integrated ADC and level matching circuits
- additional connector for digital output data (on backplane)

Differences to previous ECLs

- RXAD1000 ECL02.00 and RXAD-BB ECL03.00:
  - Phased array preamplifier power supply on RF_IN (J1) → see ***"J1 RF_IN" on page 173***
  - The pulse width of INTERLEAVE_INCR~ affects the changes in the frequency/gain-table. → see ***"INTERLEAVE_INCR~" on page 168***

Front Panel Wiring / Display *8.4*

Figure 8.3. AQS RXAD front panel



LED Display *8.4.1*

The table below summarizes the states of the three front panel LEDs.

Table 8.2. LED States

ERROR (red)	READY (green)	POWER [a] (green)	Description
-	-	off	- Power supply switched off or operating incorrectly
off	on	on	- **Normal sleep mode** - Microcontroller asleep (no spectral spikes due to microcontroller circuitry) - No communication is possible with the RXAD.
off	on resp. short-time flickering [b]	on	- Ready for operation (microcontroller awake) - Communication with the RXAD is possible.
off	blinking (data stream)	on	- Communication LED The unit has received a command from the RS485 bus master. The READY LED switches off and as soon as the RXAD acknowledges the command the READY LED is switched on again.
blinking slowly (approx. 3 Hz)	on [b]	on	- Indicates warning and not error (‘gs’ mode). Caution: Sensitive NMR experiments are not possible in this mode due to disturbances of the controller system.
blinking slowly (approx. 3 Hz)	off	on	- An error has occurred on the RXAD
blinking fast	-	on	- Boot-mode Board not initialized yet or no application firmware found (e.g. because of power failure during firmware update).

a The power LED indicates that **all** necessary voltages are present and at the correct level. If any voltage level drops then the LED will go out. Thus once the power LED lights, further investigations on the backplane to check the precise voltage are unnecessary.

b The flickering LED indicates the active microcontroller (from firmware „rxs_ap.hex“ and later; previous firmware does turn on the LED permanently).

Front Panel Connectors *8.4.2*

J1 RF_IN

Input (receive signal) from HPPR. This is a RF signal which will only be present when the HPPR is in receive mode. The timing is controlled by the RGP_HPPR signal which is closely linked to the AQS RXAD gating signal (RGP_RX~).

*For **RXAD400/600/1000** ECL02.00 or higher and **RXAD-BB** ECL03.00 or higher:*

In addition to the receiving signal, this port supplies also a switchable phased array preamplifier power source. If switched on, a 14 V_{DC} voltage will appear on this connector. If anything but a suitable phased array preamplifier is connected to it, permanent damage may occur to the connected device.

After system power up the phased array preamp power supply is always turned off. It must be switched on prior to every use by a software command.

The phased array preamp power supply is protected against short circuit and will recover automatically after removing the overload condition. The maximal DC-current of the phased array preamplifier must not exceed 70 mA for proper supply voltage.

J2 LO_IN

RF CW signal with frequency of SFO1 + f_{DQD} from SGU. This signal ($1V_{pp}$ at 50 Ω) originates from the observing SGU (LO generating SGU) and is only present when the RXAD is receiving.

The LO signal is routed in a chain through all SGUs and is fed from the most right SGU (connector LO OUT J4) to the RXAD – see also wiring principle.

J3 LO2_IN (former REF_IN)

Detector reference frequency (local oscillator signal 2) from AQS Reference Board (REF) LO2 J5.

J4 RGP_HPPR~_OUT (former EP_HPPR)

Buffered gating pulse (RGP_HPPR~) from backplane, used for preamplifiers in multi receiver systems.

Part Numbers *8.5*

- Z102116 RXAD400 (5...432.5 MHz)
- Z102117 RXAD600 (5...647.5 MHz)
- Z102118 RXAD1000 (5...1072.5 MHz)
- Z102119 RXAD-BB (BB option, 5...1072.5 MHz)

Troubleshooting / Unit replacement / Tips 'n' Tricks *8.6*

General *8.6.1*

1. Do not open the AQS RXAD in the field (calibration void).
2. Ensure the AQS Reference Board unit is **not** labeled with REF22-400, REF22-600 or REF22-1000. The AQS REF must be a REF400, REF600 or REF1000 type.
3. To replace the unit simply switch off the AQS chassis, replace the board and switch the chassis on. Having inserted a new AQS RXAD the spectrometer should be reconfigured ('cf') and the entry in the file `uxmnr.info` checked.
4. RF signals are all AC coupled[1] and the overall input resp. output impedance is 50 Ω. (Please note: The SMA-connector nuts must not be tightened more than to a torque of 45Ncm.)

Download new AQS Receiver (RX) Firmware *8.6.2*

1. Check if the directory (/Bruker/<`xwinnmr/topspin release`>/conf/instr/servtool/UniTool/files/birds) exists. Otherwise create it.
2. Copy the new firmware e.g. **rxs**_ap.hex into the directory Bruker/<`xwinnmr/topspin release`>/conf/instr/servtool/UniTool/files/birds
3. Open a shell or the command prompt in the BRUKER Utilities folder when using Windows.
4. Start the UniTool: `xwinnmr -e UniTool or topspin -e UniTool`
5. -> `aqs`, confirm
6. -> decimal address for RX-1 is **`16`**, confirm
7. When the UniTool Menu is loaded, enter `<4> Auto Download` -> download is started. The download takes about 22 minutes
8. If you have more than one RX, do the same as above with address **`17, 18,`** and so on.

1 Except RF_IN (J1) → see ***"J1 RF_IN" on page 173***

Error Messages *8.6.1*

Description of possible error messages:

Table 8.3. AQS RXAD error messages

Error No.	Error Message	Description	Possible cause
Error No. 1	Serial RS485 time-out	slave device did not answer in expected time	slave device probably not initialized, check connections
Error No. 4	Serial RS485 command, checksum error	RS485 protocol violation	spectrometer control software failure
Error No. 10	RAM Selftest Error	RAM test failed	hardware failure
Error No. 11	No application firmware found	no application firmware found	hardware failure or firmware download failed
Error No. 13	**Power failed**	**indicate that a power up has occurred and the system is not initialized**	**ordinary power up or a power breakdown during an experiment**
Error No. 15	Parameter exceeds valid range	value out of range	spectrometer control software failure or faulty input using Unitool
Error No. 16	Unknown board hardware version	this hardware version has never been delivered	firmware or hardware error on RXAD
Error No. 18	Unknown version index in configuration page	internal validation of calibration data failed	hardware error
Error No. 20	Syntax error	selected feature not supported by actual firmware, board does not understand command	spectrometer control software failure, wrong board selected, hardware feature not supported by actual version
Error No. 22	RTX create error	operating system error	firmware or hardware error on RXAD
Error No. 23	RTX memory allocation error		
Error No. 24	RTX memory free error		
Error No. 25	RTX communication pool exhausted		
Error No. 26	RTX send signal error		
Error No. 27	RTX interrupt handling error		
Error No. 28	RTX semaphore waiting list full		
Error No. 29	RTX pool create error		

Table 8.3. AQS RXAD error messages

Error No.	Error Message	Description	Possible cause
Error No. 36	Flash Byte Program Error	failure during FLASH memory programming	hardware error
Error No. 37	Flash Erase Error		
Error No. 40	Flash Erase Timer expired		
Error No. 41	Error in Flash Command Sequence		
Error No. 42	Flash Page mismatch, storing terminated		
Error No. 43	calibration data not valid		
Error No. 50	RAM selftest error	RAM test failed	hardware failure
Error No. 51	no app firmware found (wrong FW checksum)	RAM test failed	hardware failure
Error No. 52	no app firmware found (wrong FW name)	RAM test failed	hardware failure
Error No. 53	no app firmware found (wrong FW id)	RAM test failed	hardware failure
Error No. 58	Corrupt BIS on board	BIS (Board Information System) test failed	hardware failure
Error No. 59	BIS checksum error	BIS (Board Information System) test failed	hardware failure
Error No. 62	BIS Group does not exist	BIS (Board Information System) missing Group entry	should never occur
Error No. 102	Missing valid configuration page	configuration data (calibration data) not available	hardware failure
Error No. 105	Flash table does not exist, using default table	configuration data (calibration data) not available	hardware failure
Error No. 128	input value out of range	entered input value out of range	spectrometer control software failure or faulty input using Unitool
Error No. 129	Error in LO generation (coarse tuning)	LO synthesizer was not able to set its frequency correctly	hardware failure
Error No. 130	Error in LO generation (VCO gradient fail)		
Error No. 131	**Error in LO generation (PLL lock lost)**	**LO synthesizer was not able to set its frequency correctly**	**LO IN cable from SGU not connected REF IN cable from REF not connected spectrometer control software failure**
Error No. 133	Wrong RF-switch value	faulty input using Unitool	faulty input using Unitool
Error No. 134	Wrong IF-switch value		
Error No. 135	Wrong AF-switch value		
Error No. 136	Wrong PLL-gain-adjust value		
Error No. 137	Wrong PLL-level value		

Table 8.3. AQS RXAD error messages

Error No.	Error Message	Description	Possible cause
Error No. 138	Enable/Disable expected		spectrometer control software failure or faulty input using Unitool
Error No. 139	No oscillator selected	faulty input using Unitool	faulty input using Unitool
Error No. 140	**Power Diagnostic failed**	**on-board diagnostic detected faulty power supply voltages**	**check power LED on AQS RXAD and other AQS boards to determine if AQS RXAD hardware failed or fuses on the power supplies need to be exchanged**
Error No. 141	**RGP_RX-Error occurred**	**receiver has been gated while the on-board microcontroller was running – spectra may show spikes**	**spectrometer control software failure**
Error No. 142	Frequency invalid		spectrometer control software failure or faulty input using Unitool
Error No. 143	Gain invalid		
Error No. 144	Gain distribution table not found		hardware failure
Error No. 145	Gain table not found		
Error No. 146	PLL table not found		
Error No. 147	VCO gradient too low		
Error No. 148	VCO gradient too high		
Error No. 149	I2C bus fail		
Error No. 150	wrong IF-gain-adjust value		faulty input using Unitool
Error No. 151	wrong gain distribution table-index		faulty input using Unitool
Error No. 152	invalid row number in loop-table		spectrometer control software failure or faulty input using Unitool
Error No. 153	invalid amount of rows in loop table		
Error No. 154	Wrong PLL-tune value		faulty input using Unitool
Error No. 155	On/Off expected		spectrometer control software failure or faulty input using Unitool
Error No. 156	Frequency too high for this type of RX		
Error No. 157	DC offset correction table full, offset setting is stored temporally only		too many entries in the dc offset correction table
Error No. 158	DC offset correction table can't be deleted - delete DC offset correction table in RAM then save config		faulty input using Unitool

Diagnostic Tests 8.7

The AQS RXAD has no special written diagnostic program. The AQS RXAD can be accessed with the UniTool that is accessible from BRUKER Utilities:

With UniTool you can

1. read and write the AQS RXAD receiver gain
2. adjust the gain, phase and baseline for the quad module
3. adjust DC offset
4. measure the quad module temperature
5. read actual firmware version, ECL and hardware version
6. download new firmware

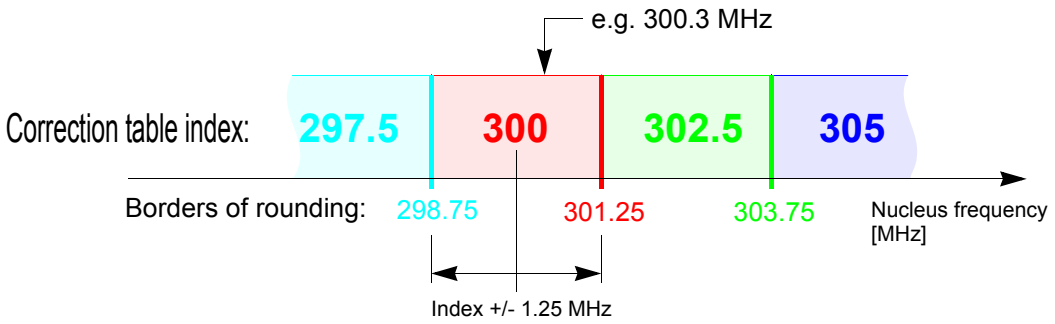
Be aware that UniTool is a hardware level tool and improper operation may void the calibration data. UniTool should be used by service personnel only.

DC Offset and Quadrature Correction Table 8.8

The DC offset of the AQS RXAD variants running with TOPSPIN can be adjusted by software and stored in the on-board FLASH non-volatile memory. The offset values are handled for each frequency/gain pair and will automatically be adjusted each time the receiver gain (rg) or the observe frequency (the nucleus) is changed.

! ***NOTE: The frequency value in the correction table is rounded to the next 2.5 MHz index-step (see Figure 8.4.). As a consequence of this rounding, a drifting magnet can cause a nucleus frequency to fall into another 2.5 MHz index-step where the RXAD is not adjusted. In this case a readjustment is necessary.***
(This difficulty can occur in unlocked magnet systems only. In locked magnet systems the nucleus frequency does not drift away.)

Figure 8.4. Rounding of the frequency in the Correction Table



If quad image gain/phase adjustment is necessary (initial quad image in qsim mode is factory preadjusted), do that ***before adjusting DC offset***. See chapter ***8.9 "Quadrature Phase/Gain Adjust / Useful Pulse Programs"***

To fill a DC offset correction table you have to do a 'gs'-experiment with TOPSPIN. Be sure TOPSPIN has selected the nucleus/frequency you want to adjust the DC offset correction for.

! ***Set the following environment variable (in TOPSPIN command line):***

```
env set TOPSPIN_DC_CORRECTION=no
```

(or run the following au-program: `dccorr off`)

Choose the acquisition window (fid) in TOPSPIN to see the time domain signal and select `Unsh` (`Unshuffle` Symbol) to see both channels.

Set the AQ_mod in the acquisition parameters (eda, AcquPars) to **qsim**.

Important: 'gs' must be started before UniTool because the UniTool occupies the serial port communication. At the end, before you try to change parameters in TOPSPIN, UniTool must be left.

You can program the DC Offset correction with UniTool (Note: 'gs' must be started before UniTool!). When working with Windows start UniTool from BRUKER Utilities, then Service Tools, then click on UniTool.cmd or when working with UNIX or Linux open an shell and enter `UniTool.cmd` or start the UniTool from the directory (/Bruker/<Topspin release>/conf/instr/servtool/UniTool).

```
Enter device name ['?' for details] (aqs) >
```

--> hit <return>

```
Enter decimal SBSB address for board in AQS rack (36) >
```

--> enter address 16 for RX_1, address 17 for RX_2, ... and hit <return>

```
B r u k e r  U n i T o o l
   Version: 1.0
   Compilation date: 040226

W A R N I N G:
   This is a hardware level debug tool.
   Improper operation may damage your hardware.

Connecting SBSB address 16 (0x10).

>>>   RX Main Menu   <<<
========================
[0] RX Init
[1] RX Board Info
[2] RX Delete Error
[3] RX Query Request
[4] RX Auto Download
[5] RX Manual Download
-------------------------
[G] RX Gain
[Y] RX DC Offset and Quadrature Adjust (built-in-ADC)
[V] RX save Configuration (OfsTable: uP RAM -> uP Flash)
[T] RX erase all OfsTableEntries of actual Frq (OfsTable: uP RAM -> Trash)
-------------------------
[P] RX select Gain Distribution Scheme
[D] RX Diagnostic Functions
```

```
[X] eXit UniTool

your choice:
```

The AQS rack must be powered on at least for 30 minutes to guarantee a stable temperature of the RXAD before adjusting any quad image or DC offset.

If necessary you can check the RX-temperature with `[D] Diagnostic Functions` and `[T] RX Temperature`:

```
    measurement range: 38...63 degree celsius
       AF Temperature:      xx degree celsius
      PLL Temperature:      xx degree celsius
```

The temperature should be about 54 °C or 59 °C constantly (depends on the internal hardware-version).

To be sure the actual DC offset correction table in the random-access-memory (RAM) is empty for this nucleus/frequency choose `[T] RX erase all OfsTableEntries of actual Frequency` in the main menu and `<y> yes`.

Select <Y> `RX DC Offset and Quadrature Adjust (built-in ADC)`. You will get this menu:

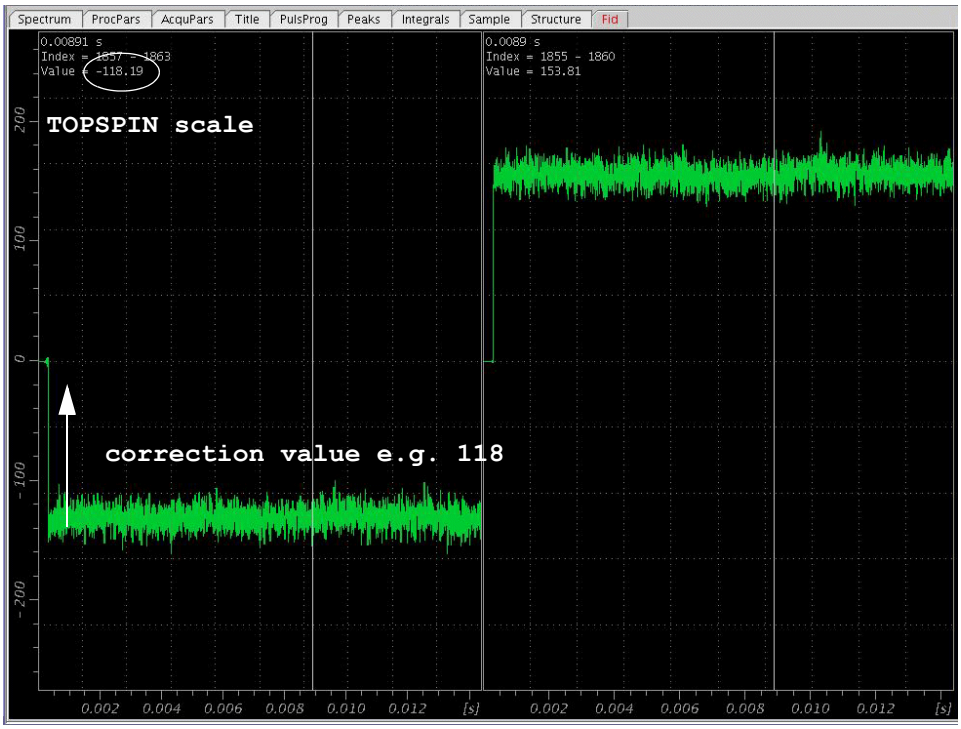
```
>>>  RX DC Offset and Quadrature Adjust Menu  <<<
================================================
[G] RX Gain
[N] next Gain
----------------------------
[A] RX set DC Offset Channel A       [1] Inc  [2] Dec  [I] Delta
[B] RX set DC Offset Channel B       [3] Inc  [4] Dec  [J] Delta
[C] RX set Quadrature Amplitude DAC  [5] Inc  [6] Dec  [K] Delta
[D] RX set Quadrature Phase DAC      [7] Inc  [8] Dec  [L] Delta
----------------------------
[V] RX save Configuration
[Q] Quit Menu

your choice:
```

The ‘offset and quad image‘ table handles entries (max. 900 entries) which are stored according to the selected nucleus/frequency (in steps of 2.5 MHz) and the selected gain (in steps of 1 dB).

To adjust the table for the actual nuclid/frequency you must start with the lowest gain. Choose `[G] Gain` and enter `1`.

Choose `[A] RX set DC Offset Channel A` to adjust channel A.

Figure 8.5. Example figure 1



The graph's left half of the TOPSPIN's y-axis shows the offset correction of channel A. If the graph's y-value is negative you have to enter that value positively to converge to zero offset. If the graph's y-value is positive enter the value negatively.

The controller on RXAD will calculate the internal correction values needed. Repeat this once or twice and you will be within one percent of the uncorrected offset.

There may be an inaccuracy between entered value and actually set correction due to scaling variation by chosen digital filter and SWH.

`a <correction value>`, for channel A respectively `b <correction value>` for channel B

e.g. for the above example:

```
a 118
```

When you have achieved small offset values you can adjust the offset by increasing or decreasing the lowest significant bit of the adjustment D/A-converter by typing

`[1] Inc` or `[2] Dec` for Channel A respectively
`[3] Inc` or `[4] Dec` for Channel B

The graph's right half of the TOPSPIN's y-axis shows you the offset correction of channel B. --> the same as above for Channel B...

Choose `[B] RX set DC Offset Channel B` to adjust channel B --> the same as above...

Instead of type [B] and afterwards enter the correction value you can also type:

`b <correction value>` for channel B

e.g. for the above example:

```
b -153
```

When you have achieved small offset values you can adjust the offset by increasing or decreasing the lowest significant bit of the adjustment D/A-converter by typing

`[3] Inc` or `[4] Dec` for Channel B

Repeat the whole procedure for the next gain by choosing `[N] next Gain`. Repeat 'Next Gain' until all gains are adjusted including the highest gain (= 203 respectively 2050).

If you don't want your table entries to be lost after a power down of the AQS-rack you need to save the RXAD configuration with `[V] RX save configuration`. This will take a few seconds.

```
Configuration has been saved
```

After having saved the table initialize the receiver selecting `[0] RX Init` from the Main Menu.

Important: You must choose `[Q] Quit Menu` and `[X] eXit UniTool` to free/release the serial port of your work station before altering parameters in TOPSPIN.

Stop the TOPSPIN experiment, select the next nucleus/frequency you want to adjust and start another 'gs'-experiment. Adjust in the same way as above...

! ***If you have finished DC offset correction reset the following environment variable (in TOPSPIN command line):***

```
env set TOPSPIN_DC_CORRECTION=yes
```

(or run the following au-program: `dccorr on`)

This will set the AQ_mod as it was before the adjustment.

Quadrature Phase/Gain Adjust / Useful Pulse Programs *8.9*

For quadrature phase/gain adjustment the following pulse program is useful:

```
;zgcw.mod
;avance-version (04/02/08)
;1D sequence with CW decoupling
#include <Avance.incl>
"d11=30m"
1 ze
2 d11 reset:f1 reset:f2
  d11 pl26:f2
  d11 cw:f2 ph30
  d1
  p1 ph1
```

```
go=2 ph31
wr #0
d11 do:f2
exit
ph1=0 2 2 0 1 3 3 1
ph31=0 2 2 0 1 3 3 1
ph30=0
;pl1 : f1 channel - power level for pulse (default)
;pl26: f2 channel - power level for cw decoupling
;p1 : f1 channel -  high power pulse
;d1 : relaxation delay; 1-5 * T1
;d11: delay for disk I/O [30 msec]
```

In `edasp` select two identical nucleus for F1 and F2 and set the offset frequency OFS2 of the second one to e.g. 1000.0 Hz

Figure 8.6. Example of eda for RXAD Quadrature Adjustment

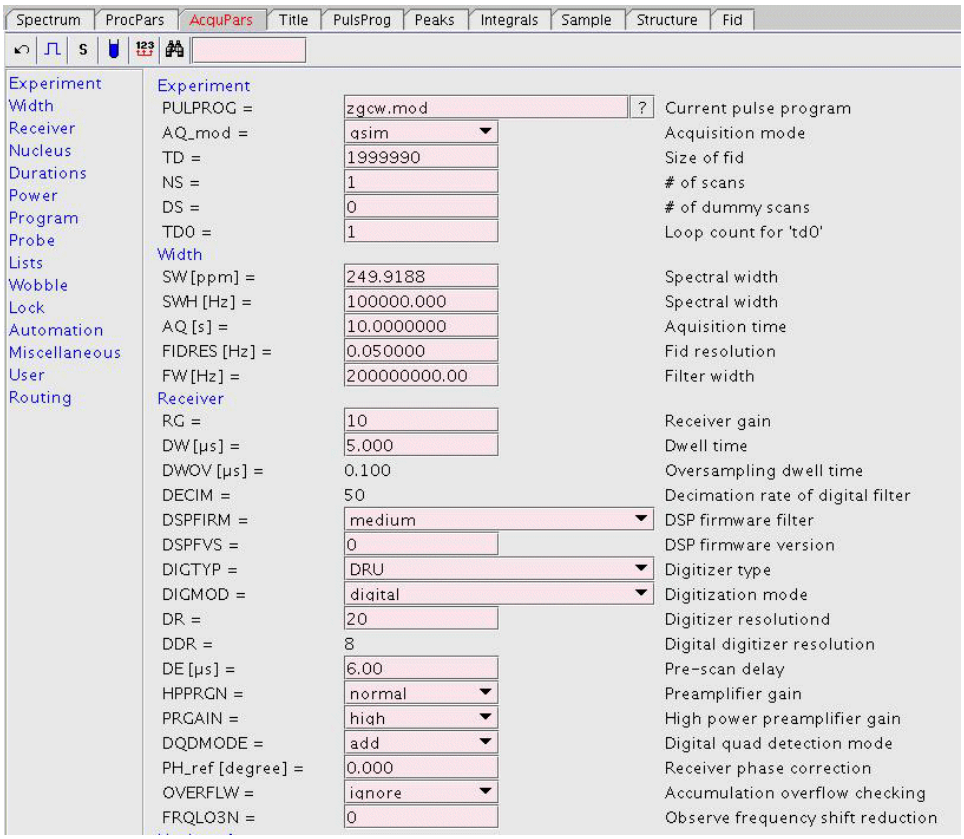
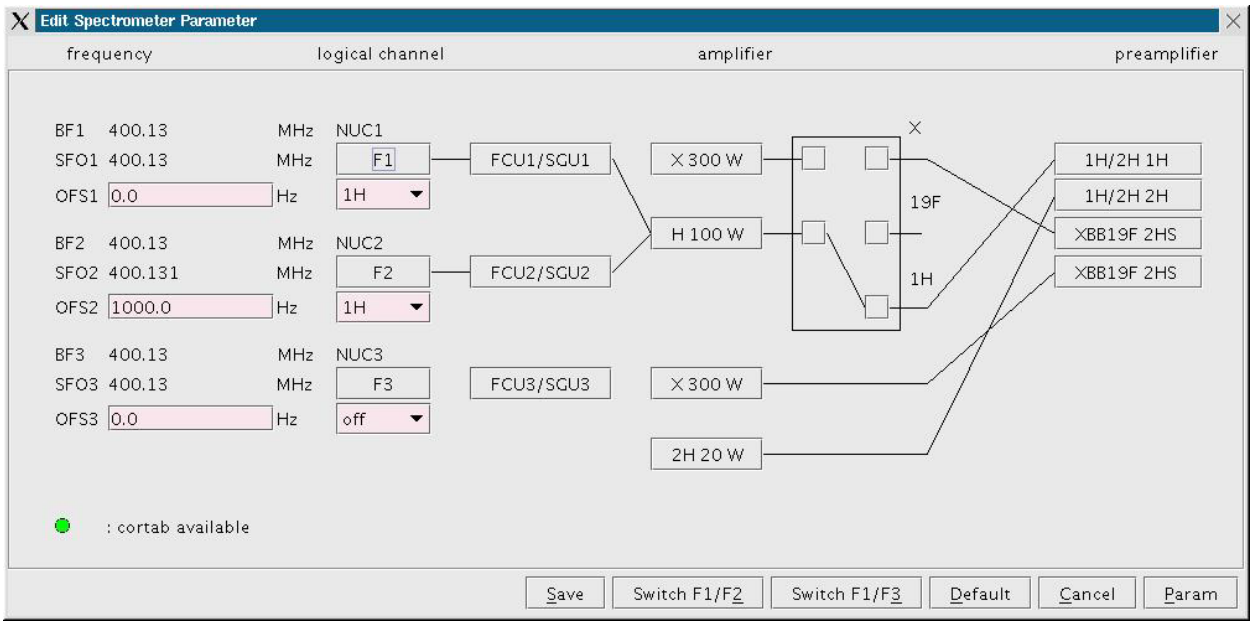


Figure 8.7. Proposed setup for quad image adjustment



Set `phmod` to `mc`.

Connect now the RF OUT of SGU2 with the RF IN of the RXAD directly and start acquisition in ‘gs’ mode (pl26 ≈ 40 dB).

Check the input signal level in the acquisition window. Check for appropriate amplitude of the ADC and do not overdrive it.

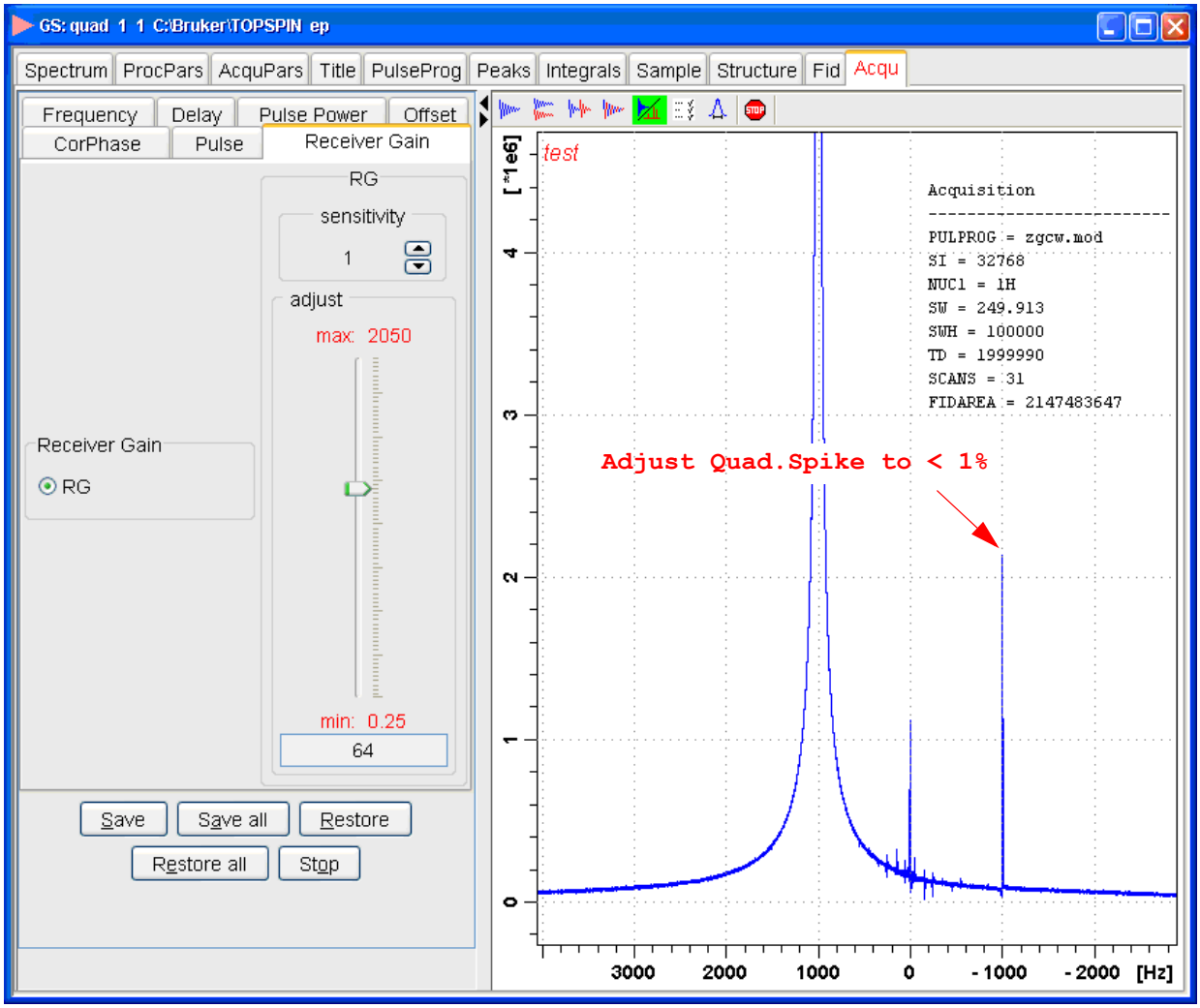
Press in TOPSPIN the button „Execute realtime ft and show spectrum“ (Symbol) and adjust the quadrature image signal with UniTool.

The adjustment procedure is similar to that one for dc offset correction.

For phase/amplitude adjustments select the menu point <Y> `RX DC Offset and Quadrature Adjust (built-in ADC)` and choose one of the following:

```
[C] RX set Quadrature Amplitude DAC  [5] Inc  [6] Dec  [K] Delta
[D] RX set Quadrature Phase DAC      [7] Inc  [8] Dec  [L] Delta
```

Figure 8.8. Example of Quadrature Adjustment



Specifications *8.10*

Frequency Range:

5...432.5 MHz (RXAD400)

5...647.5 MHz (RXAD600)

5...1072.5 MHz (RXAD-BB, RXAD1000)

Frequency Stability: This is governed by the stability of the crystal oscillator on the REF unit which is specified to 3 $x10^{-9}$/day and 1 $x10^{-8}$/year

Frequency Resolution: The local oscillator synthesizer in the AQS RXAD follows the SGU LO signal with its resolution of <0.005 Hz.

LO Phase Settling Time: 2 μs max. (RXAD-BB)

Audio Signal Settling Time: < 2 μs (RXAD-BB)

Gain:

Gain Range: 0...58 dB, 58 dB gain range in 1 dB steps

ADC Resolution:

depends on oversampling rate on AQS DRU:

- up to 200 kHz bandwidth 20 bit
- up to 5 MHz bandwidth 16 bit

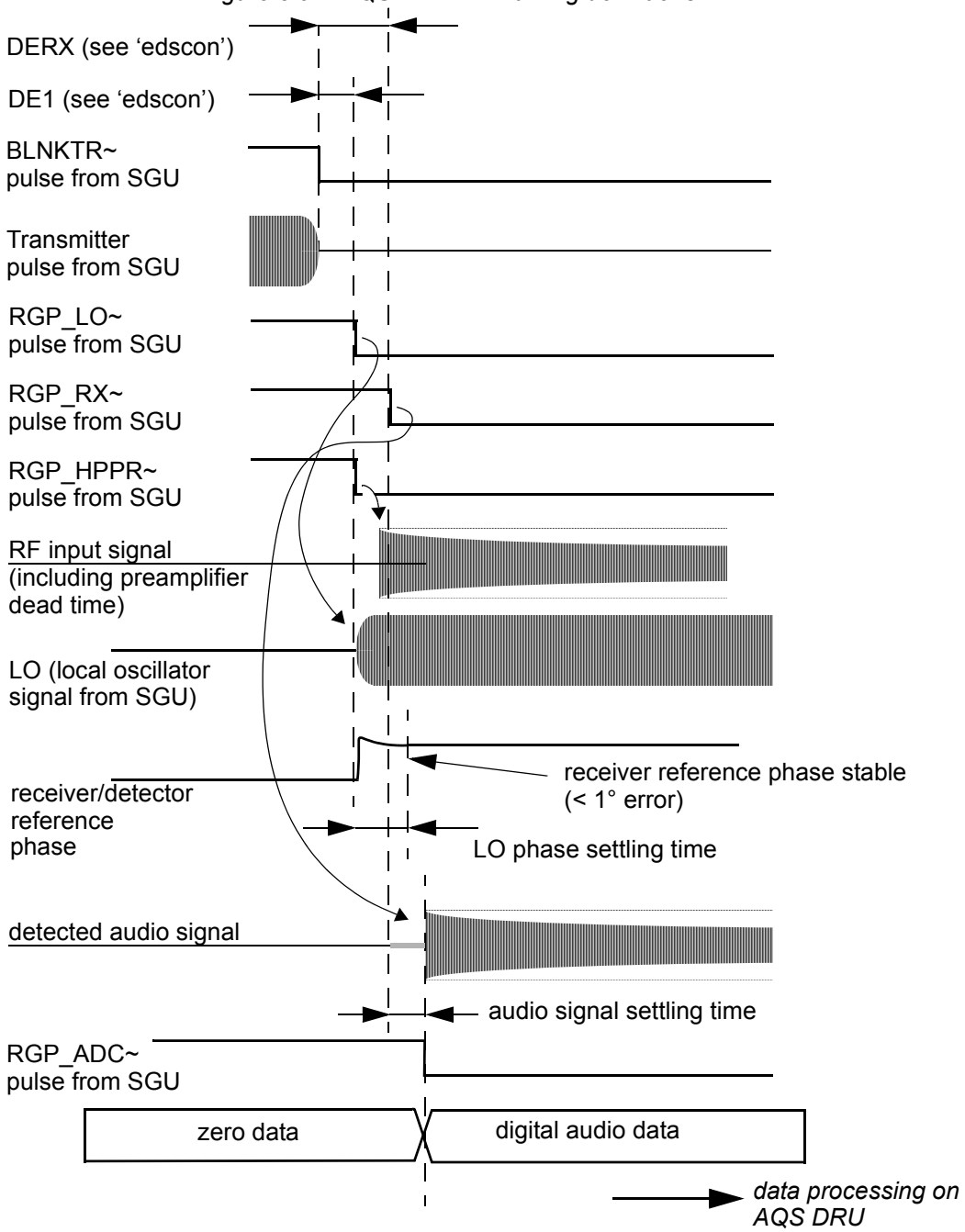
ADC Output Data Rate

28 bit / 20 Mwords per second (560 Mbit/s)

Timing Definitions *8.10.1*

Turn on or settling time of the AQS RXAD-BB are defined as follows:

Figure 8.9. AQS RXAD-BB timing definitions



Power Supply / Fuses *8.11*

See ***8.4.1***

Backplane Connector *8.11.2*

	z	a	b	c	d	e	f
1	GND	GND	RESERVE_1	NC	GND	SAMPLE_INFO0	GND
2	GND	NC	GND	SAMPLE_INFO3	SAMPLE_INFO2	SAMPLE_INFO1	GND
3	GND	GND	NC	RESERVE_2	GND	SAMPLE_INFO4	GND
4	GND	20MHZ_CLK_X	GND	INTERLEAVE_INCR~	ADC_SEL1	ADC_SEL0	GND
5	GND	GND	20MHz_CLK_X~	RESERVE_3	GND	RGP_LO~	GND
6	GND	BLNKTR1~	GND	BLNKTR2	RESERVE_6	RESERVE_4	GND
7	GND	BLNKTR3~	BLNKTR4~	NC	GND	RGP_ADC	GND
8	GND	BLNKTR5~	GND	BLNKTR6~	RESERVE_7	DWL_CLK	GND
9	GND	BLNKTR7~	BLNKTR8~	NC	GND	RGP_RX~	GND
10	GND	SBS_TTL_TX	GND	SBS_TTL_RX	SBS_TTL_TX_ENAB~	RESERVE_5	GND
11	GND	LOCAL_TX	LOCAL_RX	SBS_TTL_WUP~	GND	RGP_HPPR~	GND

red = CCU bus galvanically isolated
blue = Intra Rack Bus

Key Area

15	GND	SLOT2	SLOT1	SLOT0	GND	RESERVE_ADC_1	GND
16	GND	SLOT3	GND	I2C_SDA	RESERVE_ADC_2	GND	GND
17	GND	EMERGENCY_STOP	I2C_BUS_REQ	I2C_SCL	GND	ADC_I2C_SDA	GND
18	GND	NC	GND	I2C_2_SDA	I2C_2_SCL	GND	GND
19	GND	NC	NC	NC	GND	ADC_I2C_SCL	GND
20	GND	NC	GND	P2V	N2.5V	GND	GND
21	GND	P5V	P35V	P9V	P9V	P9V	GND
22	GND	P5V	RACK0	N9V	N9V	N9V	GND
23	GND	P5V	P19V	N19V	RACK1	P12V	GND
24	GND	P5V	P19V	N19V	RACK2	P12V	GND
25	GND	P5V	P19V	N19V	RACK3	P12V	GND

Table 8.4. RXAD extension connector

	z	a	b	c	d	e	f
1	GND	P5V	P5V	P5V	P5V	P5V	GND
2	GND	RESERVE_4	RESERVE_5	GND	RESERVE_3	GND	GND
3	GND	ADC_I2C_SDA	GND	L3_OPT	GND	LCLK_OPT	GND
4	GND	ADC_I2C_SCL	GND	L3_OPT~	GND	LCLK_OPT~	GND
5	GND	GND	L_CLK	GND	L_DATA_3	GND	GND
6	GND	GND	L_CLK~	GND	L_DATA_3~	GND	GND
7	GND	L_OVR0	GND	L_DATA_2	GND		GND
8	GND	L_OVR1	GND	L_DATA_2~	GND		GND
9	GND	GND	L_DATA_1	GND	L_DATA_0	GND	GND
10	GND	GND	L_DATA_1~	GND	L_DATA_0~	GND	GND
11	GND	RESERVE_0	GND	RESERVE_1	GND	RESERVE_2	GND

AQS DRU 9

Introduction 9.1

The AQS DRU (Digital Receiver Unit) is a digital signal processing board implementing an enhanced digital receiver in comparison to the RCU introduced in 1994. It incorporates the digital mixing (LO3) stage for DQD and the ‚on the fly' digital signal processing block for a variety of digital filters within the AQS/2 receiver system.

To achieve a more flexible spectrometer integration (especially with extended multiple receiver systems), accumulation and data buffering is done on board. This allows for data transfer to the workstation to run across a commercial local area network (Fast Ethernet LAN). The omnipresent transfer control protocol / internet protocol (TCP/IP) is used to build the loosely coupled, standardized spectrometer environment, thus allowing flexible extensions in the future.

Distributed communication between the workstation and one or more DRU runs on common object remote broker architecture (CORBA). CORBA is a modern and reliable distributed object middle ware. By implementing a hardware- and operating system independent software interface, it allows in future to communicate with the DRU by any workstation topology (Intel architecture, SGI, etc.) and operating system (JAVA, .NET, etc.)

Diagnosis and servicing access to the DRU relies on hypertext transfer protocol (HTTP) and hypertext markup language (HTML), enabling service access just by any web browser (e.g. Netscape), without the need for special training of service people like the former UniTool.

The AQS DRU is enclosed in an aluminum metal case allowing seamless integration in the AQS chassis - concerning minimized RF interference and design.

The AQS DRU comes in two versions, the DRU and the DRU-E:

AQS DRU, P/N Z100977

This version includes interfaces for automatic tuning and matching (ATMA), probe identification and control system (PICS) and AQS integrated preamplifier modules. It will be mainly used for low field NMR systems.

This version does not include the very high speed interface (digital data output) and has not an expandable ADC word width facility for future RXAD.

A real-time pulse (RCP) input is used to switch the 2H preamplifier module transmit and receive switch according to the lock operation (TP_F0).

AQS DRU-E, P/N Z102520

This version includes a very high speed interface to stream the received data to further signal processing systems for applications requiring more than the 50MBit/s, e.g. for real time decision capability or just for user oriented dedicated solutions.

The protocol has not been defined yet but may be fixed later by downloading new firmware. Such protocols could be CameraLink™ or similar.

It also offers wider ADC data paths to the RXAD. This interface is prepared for the increased dynamic range of future AD converters.

This version does not include interfaces for ATMA, PICS or preamplifier modules. The HPPR/2 system is required for these purposes instead.

A real-time pulse (RCP) output is available to trigger future experiments upon acquiring NMR data (to be defined).

General Functions and Description *9.2*

The basic digital receiver concept of the DRU is designed to fulfill the following tasks:

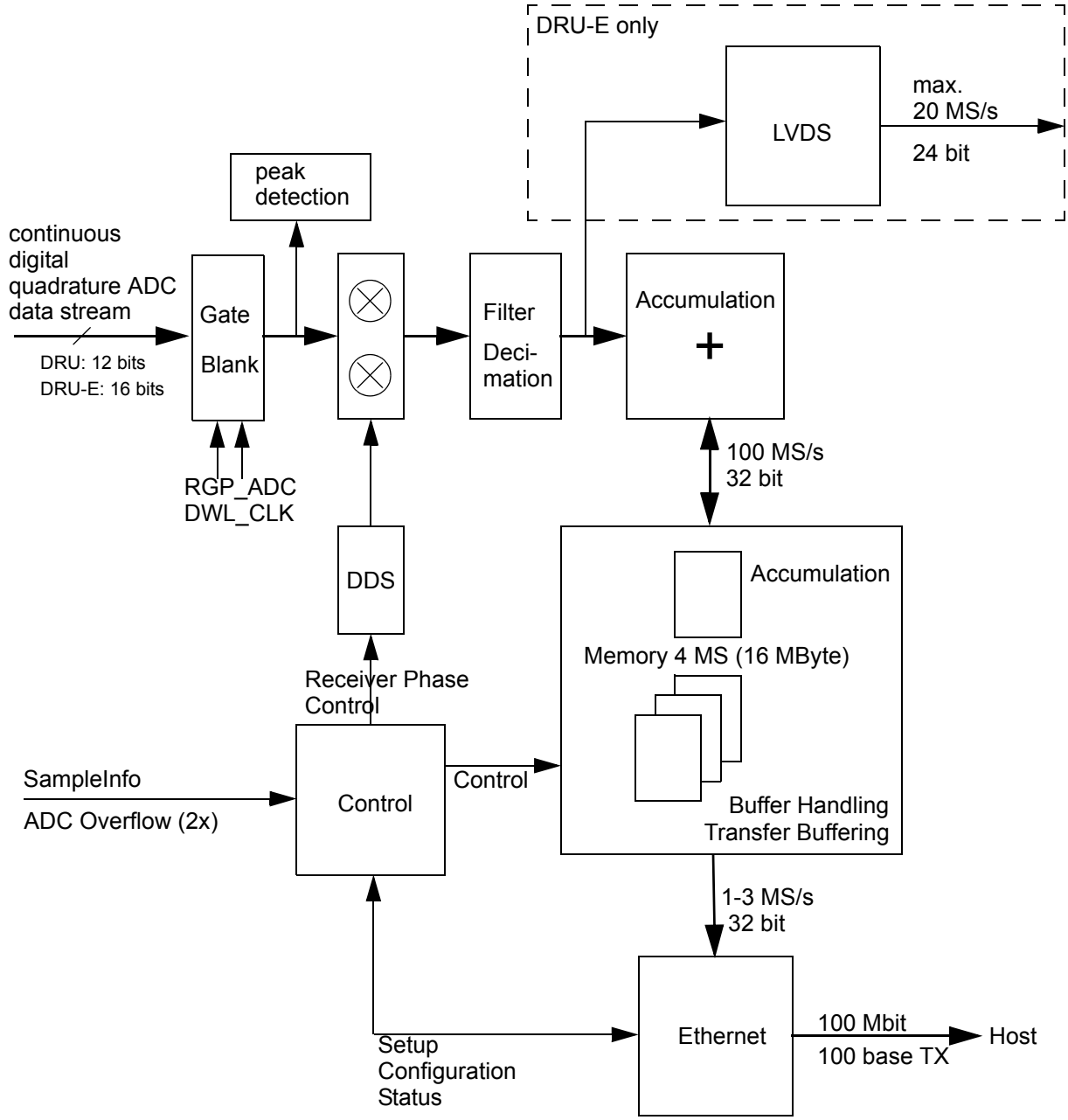
1. Interface to different types of AD converters (for future)
2. Propagate a digitizer overflow condition
3. Capture digitizer peak values (i.e. used for receiver gain adjust)
4. Automatic DC offset calibration (used for AutoZeroCompensation)
5. Digital receiver phase control
6. Digital quadrature detection (LO3)
7. Digital filtering of NMR signals
8. Decimation of NMR signals
9. Accumulation and acquisition, multi buffer handling
10. Data transfer to workstation via ethernet (write to disk, online display)
11. Special fast functions (i.e wobble display, RGA, AutoZeroCompensation)

Most of these operations (scan control) are under real time control by the pulse program via the so called ‚SampleInfo' bus. With this it is possible to handle the ADC data, in the extreme cases each sample, by the information given via this acquisition synchronous system bus. The scan control runs in parallel with the DWELL clock and the RGP_ADC of the digitizer.

Depending on type of DRU, following functional modules are incorporated:

12. Integration of AQS preamplifier controller (DRU only)
13. Real Time Trigger output (to be defined, DRU-E only)
14. High Speed LVDS data output (DRU-E only)

Figure 9.1. DRU Blockdiagram ‚digital receiver‘



Power Supply and Monitoring LED‘s ***9.2.1***

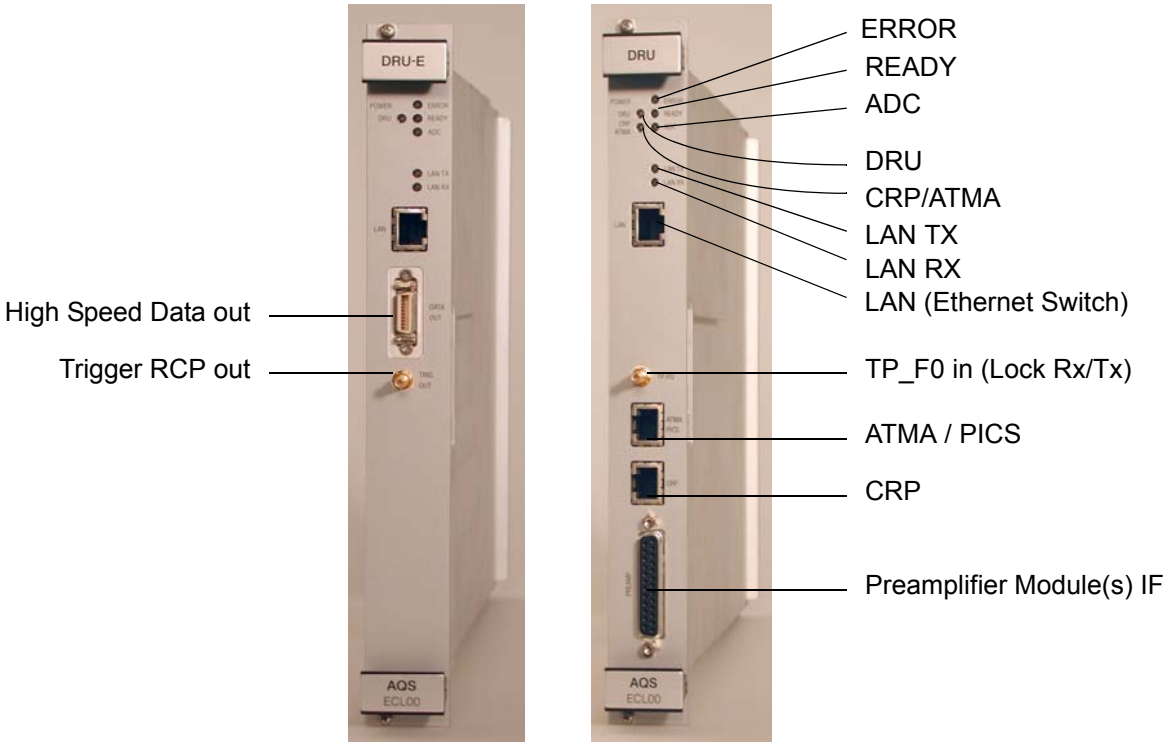
Operation of the *on-board* power stabilization is monitored by the two green LED on the front labeled ‚POWER‘.

The LED labeled ‚DRU' monitors the internal DRU supplies (3.3V, 2.5V, 1.5V). These are all derived from a single 5V AQS backplane supply.

The LED labeled ‚CRP/ATMA' monitors the +/-15V CRP and +9V ATMA voltages. These are derived from the +/-HPPR_19V and HPPR_9V AQS backplane supplies.

Front Panel Wiring / Display *9.2.2*

Figure 9.2. AQS DRU-E and AQS DRU frontside view



Reset and Operation LED Display *9.2.1*

ERROR LED:

The red ‚ERROR' LED indicates a pending ERROR.

READY LED:

Normal operation is indicated by the green ‚READY' LED.

Every 500ms this LED is turned off for 20ms, resulting in a faint flicker. If this flicker is missing, the DRU is not running properly and must be reset by switching off the AQS chassis for about 10 seconds.

ADC LED:

This green ‚ADC' LED indicates a running Acquisition.

LAN TX LED:

This green ‚LAN TX' LED indicates outgoing LAN traffic.

LAN RX LED:

This green ‚LAN RX' LED indicates incoming LAN traffic.

Servicing the DRU *9.3*

Diagnosis and servicing access to the DRU relies on HTTP, enabling service access just by any web browser. This is possible because only basic HTTP V1.1 protocol elements have been used.

Accessing the DRU *9.3.1*

Depending on the slot and the rack code, the DRU adopts one of the following IP addresses. Any illegal or unknown configuration is mapped to DRU1 and the message „Illegal Rack/Slot configuration. Fallback to DRU1 address." is written to the DRU Log.

Table 9.1. IP Addresses for DRU

IP Address	DRU Name
149.236.99.89	dru1
149.236.99.88	dru2
149.236.99.87	dru3
149.236.99.86	dru4
149.236.99.85	dru5
149.236.99.84	dru6
149.236.99.83	dru7
149.236.99.82	dru8

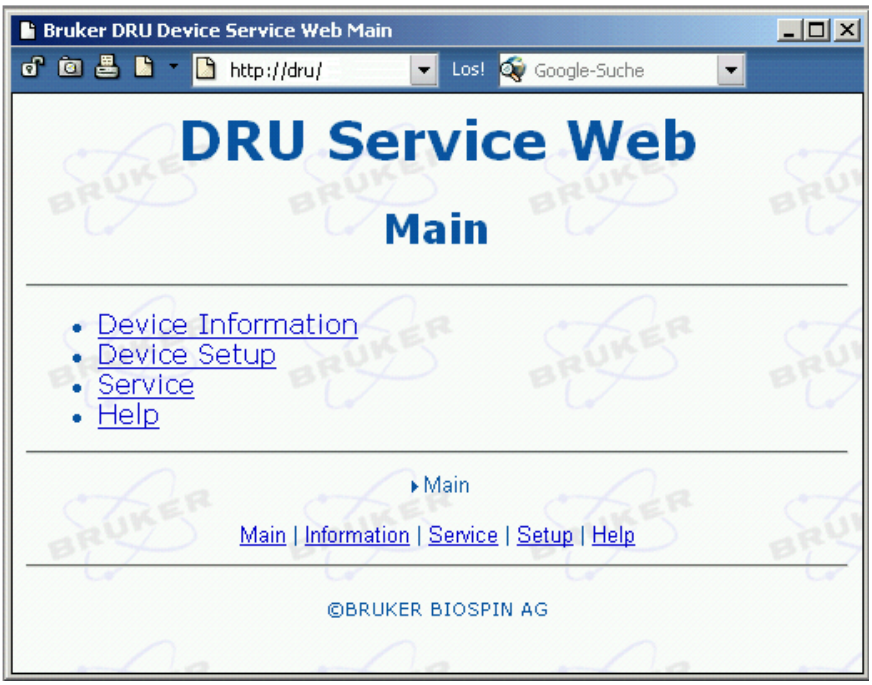
It might be useful to edit the hosts file.

In case of problems:

- check the RJ45 cabling between DRU, Ethernet switch and the workstation
- check the ethernet switch power if appropriate
- check the DRU heart beat (flicker of ‚READY LED)

- ping DRU1 (DRU2...)
- check LAN ‚RX/TX' LED while pinging

To access the DRU, start your favorite web browser and type „dru1" or „149.236.99.89" as URL. You should get the following start screen:



Downloading new firmware *9.3.2*

Main -> Device Information -> DRU Firmware

leads you to a page giving information about the current firmware.

! ***Note: The document caching of the browsers can be tricky - make sure your browser doesn't fool you with old data. Most browsers have some „Reload" button for this purpose.***

Main -> Device Setup -> Load new DRU firmware

leads you to a page allowing to download new firmware. The current firmware file name is displayed together with a prompt for the new firmware file.

The following example explains the naming convention:

```
DRU_firmware_040325.hex
```

040325 is a date code for March 25, 2004. Alphabetically sorted, the newest file is found at the bottom line.

! ***Do not download an older firmware than the currently installed one, except you want to roll back in time.***

Main -> Service -> Display logged messages

shows a page containing the main log. If you are in the situation to report a software bug, it‘s a good idea to include this log. You can copy the text part into an explaining mail or you can save the whole HTML page and attach it.

Technical data *9.4*

ADC Data Input:

Data Rate	2*20	MS/s
Data Format DRU	2 x 12	bits
Data Format DRU-E	2 x 16	bits

NMR Data Output (Ethernet):

Data Rate	0.3 - 10‘000	kS/s[1]
Data Word Width	32	bits

NMR Data Output (LVDS):

Data Format	to be defined

Acquisition Modes:

Quadrature off acquisition (only channel A, analog and digital modes)	QF
Quadrature simultaneous acquisition (analog and digital modes)	QSIM
Acquisition with Digital Quadrature Detection (digital mode only)	DQD

Digital Quadrature Detection (digital down conversion):

DDS frequency range (LO3)	+/-(0...5)	MHz
Digital Mixer Operation	SSB	

Digital Filter type ‚smooth‘:

Passband Error	0.01 %	max
Transition Region	15 %	SWH
Stoppband Attenuation	86 dB	min
Group Delay	20	samples
Bandwidth (SWH)	5 MHz	max

Digital Filter type ‚medium‘:

Passband Error	0.001 %	max
Transition Region	10 %	SWH
Stoppband Attenuation	103 dB	min
Group Delay	36	samples
Bandwidth (SWH)	2.222 MHz	max

Digital Filter type ‚sharp‘:

Passband Error	0.001 %	max
Transition Region	5 %	SWH
Stoppband Attenuation	104 dB	min

1 complex data points

Group Delay	68	samples
Bandwidth (SWH)	1.25 MHz	max

Miscellaneous:

Direct accessible Scan Memory Size	4M	samples
Banked Scan Memory Size	16M	samples
Sustained LAN data rate (depending on Workstation)	45	Mbit/s

Trigger output:

Voltage Level	5	V
Impedance	50	Ohm
max Frequency	1	MHz

Backplane Connectors *9.5*

The DRU accesses the AQS backplane by 2 high density backplane connectors. The common interface is similar to the one used on SGU. The ADC data interface to the RXAD is done by a private additional backplane connector (dedicated DRU slots within the AQS/2 chassis).

Table 9.2. Common AQS backplane connector

	z	a	b	c	d	e	f
1	GND	GND	INTRA_STATUS		GND	SAMPLE_INFO0	GND
2	GND		GND	SAMPLE_INFO3	SAMPLE_INFO2	SAMPLE_INFO1	GND
3	GND	GND	NC	I2C_STATUS	GND	SAMPLE_INFO4	GND
4	GND	20MHZ_CLK_X	GND	INTERLEAVE_INCR~	ADC_SEL1	ADC_SEL0	GND
5	GND	GND	20MHz_CLK_X~	RESERVE_3	GND		GND
6	GND		GND			INTRA_WUP	GND
7	GND		BLNKTR4~		GND	RGP_ADC	GND
8	GND		GND			DWL_CLK	GND
9	GND		BLNKTR8~		GND		GND
10	GND	SBS_TTL_TX	GND	SBS_TTL_RX	SBS_TTL_TX_ENAB~		GND
11	GND	LOCAL_TX	LOCAL_RX	SBS_TTL_WUP~	GND	RGP_HPPR~	GND

red = CCU-Bus galvanically isolated
blue = Intra Rack Bus

Key Area

15	GND	SLOT2	SLOT1	SLOT0	GND	MCODE0	GND
16	GND	SLOT3	GND	I2C_SDA	MCODE3	GND	GND
17	GND	EMERGENCY_STOP		I2C_SCL	GND	MCODE1	GND
18	GND		GND	I2C_2_SDA	I2C_2_SCL	GND	GND
19	GND				GND	MCODE2	GND
20	GND		GND			GND	GND
21	GND	P5V		P9V	P9V	P9V	GND
22	GND	P5V	RACK0				GND
23	GND	P5V	P19V	N19V	RACK1		GND
24	GND	P5V	P19V	N19V	RACK2		GND
25	GND	P5V	P19V	N19V	RACK3		GND

Table 9.3. private DRU - RXAD backplane connector

	z	a	b	c	d	e	f
1	GND	P5V	P5V	P5V	P5V	P5V	GND
2	GND			GND		GND	GND
3	GND	ADC_I2C_SDA	GND	L3_OPT	GND	LCLK_OPT	GND
4	GND	ADC_I2C_SCL	GND	L3_OPT~	GND	LCLK_OPT~	GND
5	GND	GND	L_CLK	GND	L_DATA_3	GND	GND
6	GND	GND	L_CLK~	GND	L_DATA_3~	GND	GND
7	GND	L_OVR0	GND	L_DATA_2	GND		GND
8	GND	L_OVR1	GND	L_DATA_2~	GND		GND
9	GND	GND	L_DATA_1	GND	L_DATA_0	GND	GND
10	GND	GND	L_DATA_1~	GND	L_DATA_0~	GND	GND
11	GND	RESERVE_0	GND	RESERVE_1	GND	RESERVE_2	GND

SGU Signal Generation Unit 10

Introduction 10.6

The SGU is one of the most significant advances in the new AV series. It is the unit where the generation of all analog characteristics of the RF signal takes place. The SGUs are located in the analog section of the AQS rack between the REF unit and either the Router or internal amplifiers. Each RF channel has a dedicated SGU.

On the transmission side the SGU generates the signal frequency, phase and regulates the amplitude (including shape control) as well as the blanking and gating pulses. The information is received from the TCU3 / FCU4 via the LVDS but implemented upon in the SGU. The output of the SGU will be a miniature version of the final transmitted signal. The only change that takes place to the signal after SGU generation is the power increase in the amplifiers. On the receive path the SGU generates the LO frequency as well as the receiver gating pluses.

In hardware terms all SGUs are identical but one SGU will occupy the master (AQS Controller) slot in the AQS and is referred to as the 'rack master', 'master SGU' or even better ‚*AQS controller*'. This AQS Controller SGU recognizes its position automatically and switches into AQS Controller mode whereas all other SGUs are set to slave mode. The slot occupied depends on the jumper setting on the rear side of the backplane (see ***10.7.2***). The SGU AQS Controller communicates with various analog units to reduce the needed communication to a minimum for the CCU10 and the subunits. see ***"AQS signal path" on page 13***.

Note that while the AQS Controller SGU has additional functionality it also performs all the tasks of a standard SGU.The various SGU boards are synchronized by means of a 20 MHz clock signal from the backplane. The clock signal originates on the AQS Reference Board. The synchronization is essential if the various RF channels are to be phase coherent etc.

Apart from the AQS Controller SGU the only other distinction between the various SGUs is that one SGU is pre allocated as the observing SGU and generates the LO as well as the receiver timing. This can be any SGU depending upon which FCU in the edsp menu is chosen as the OBS.

Each SGU has a dedicated hard-wired LVDS link to an FCU (either channel A or B). The high speed link transfers all NMR relevant real-time events in 50ns time slots to the corresponding SGU (e.g. pulses, shapes, phase jumps, frequency shifts etc.). Each rf channel is controlled by a separate high speed link. It is connected via a cable on the front panels of the two units (point to point connection).

NB: The SGU is really a DAC. It does nothing without FCU order. The FCU generates for example blanking signals. It orders the SGU to go high/low/high/low and so the BLANKTR is generated. The LVDS is the bridge between the digital and analog side.

The SGU has access to the various buses along the AQS backplane.

An important feature of the SGU is the extra shielding. This is ensures that the generated RF signals are free of distortion.

Functions / Description *10.7*

The central role played by the SGU is evident from the extensive list of functions below. For further details on some of the specific details below see ***"Important signals" on page 219***

All SGUs.

1. Generation of the precise final transmission frequency by means of an on-board frequency generator. The SGU implements all analog aspects of the signal including frequency, frequency shifts, phase shape etc. The information regarding the precise characteristic of the signal is received from the FCU via the LVDS.

2. Amplitude control both in terms of magnitude (mult) and shape (mod). Although the SGU delivers a max voltage of 1Vpp the linear nature of the amplifiers means that the SGU has exclusive control of the final amplitude.

3. Generation of blanking signals for use in the various amplifiers. The AQS internal amps receive the blanking directly from the backplane, whereas the external amps receives the signals from the PSD which in turn receives the signals from the backplane.

observing SGU only.

4. Generation of gating pulses to be used in the HPPR, Receiver, A/D Converter, RXAD, DRU

5. Generation of the dwell clock (HADC,SADC, FADC) or dwell enable signal for the DRU

6. Generation of LO frequency for the receiver

AQS Controller SGU only

7. Initializes various units after a power up or ‘ii’ command. A proper initialization of all RF units in the AQS mainframe is highly dependent on a correct power up process of the AQS Controller SGU-1.

8. Communication with the CCU10 via the SBSB1 and with other analog units via a I^2C bus.

9. Router control via the backplane. This also includes control of the mini router in AQS internal amplifiers. The information is transmitted via the I^2C bus mentioned above.

SGU-2 only

10. Generation of the ‘wobb’ signal

The LO will be generated on the observing SGU and daisy chained through all the succeeding SGUs to the receiver. This daisy chain is unidirectional in the direction of the receiver. If in a four channel system SGU-2 is the OBS then SGU-2 will generate the LO and this will be daisy chained through SGU-3 and SGU-4 to the receiver. See ***Figure 10.3.***

Figure 10.3. LO daisy-chain for the case where SGU-2 is the observing SGU

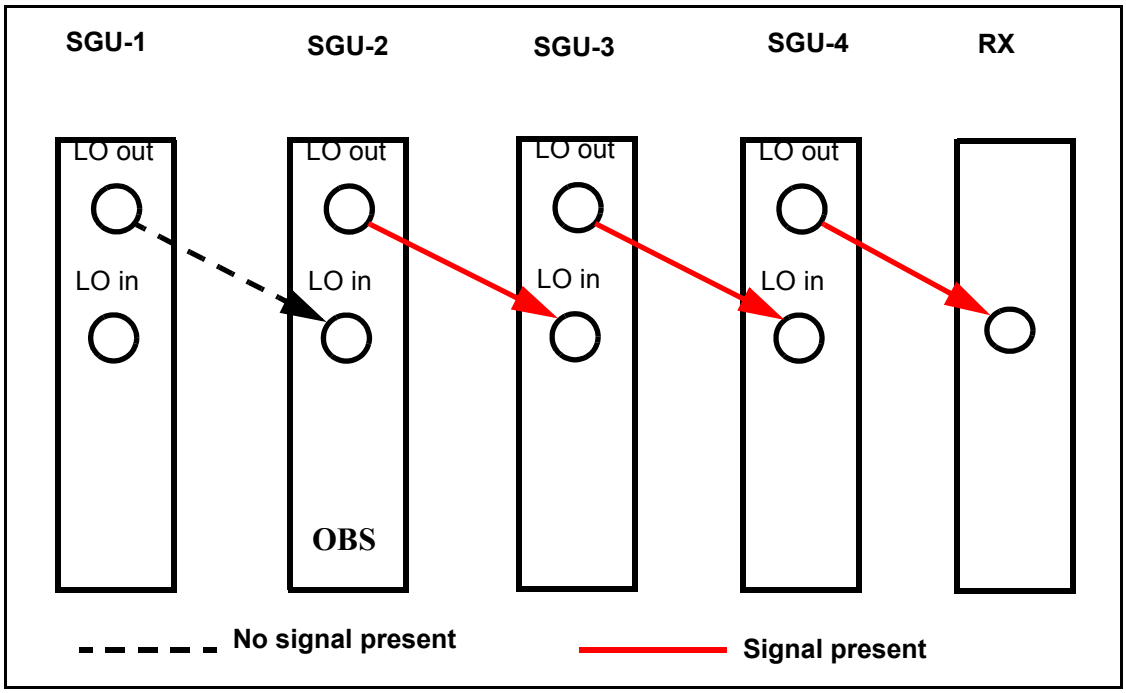
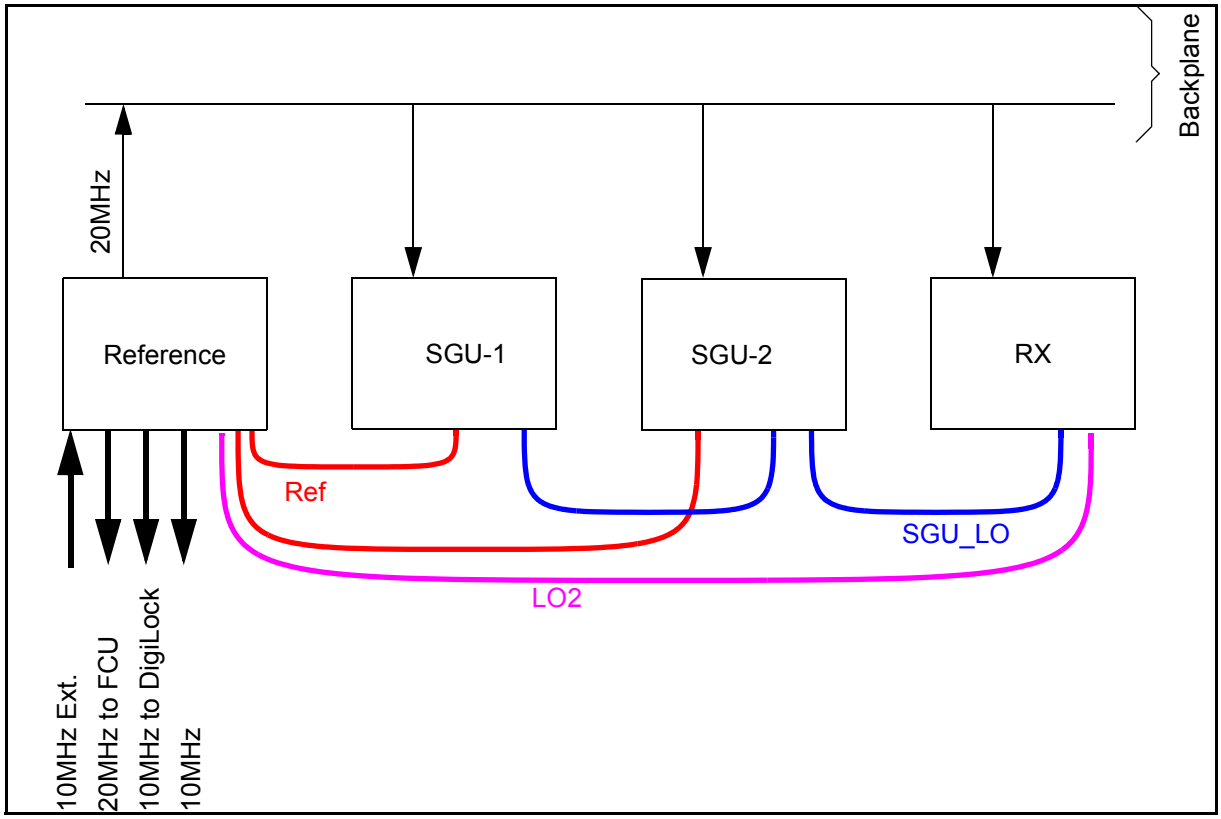
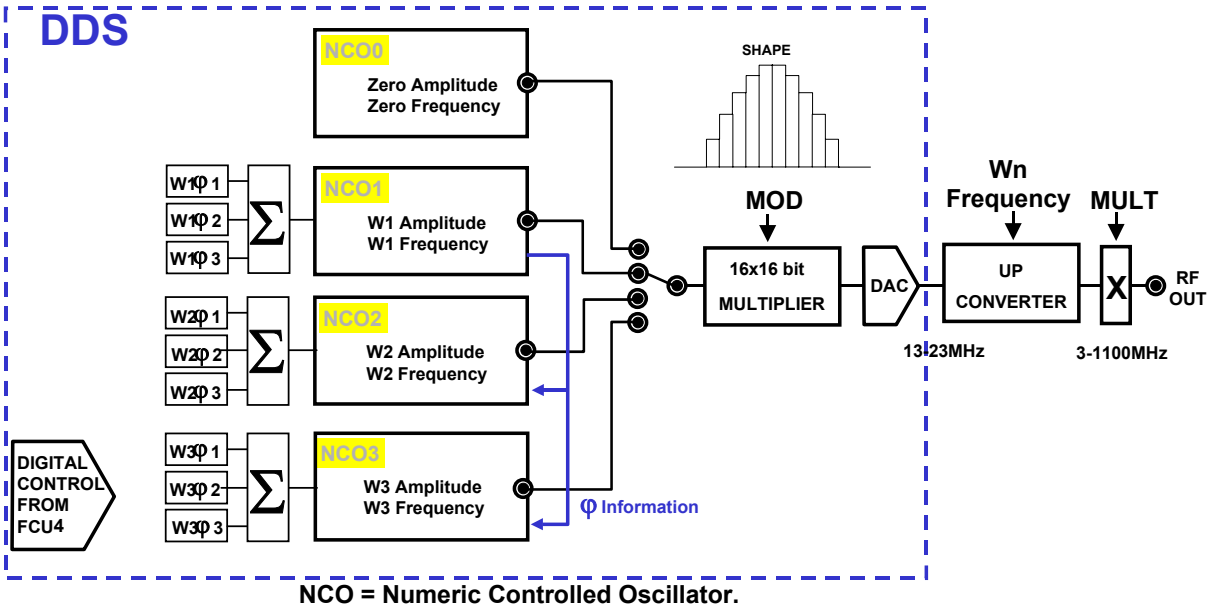


Figure 10.4. SGU RF paths



This is shown schematically in ***Figure 10.6.*** Note that the signal path switching is controlled via the LVDS.

Figure 10.5. signal generation on the SGU



NCO = Numeric Controlled Oscillator.
DDS = Direct Digital Synthesis.

Although from a service point of view the internal workings of the SGU are not relevant, this is such a new unit and plays such a central role in the spectrometer that it is perhaps worth making a short description of its main features.

At the heart of the SGU are three NCOs (Numerically Controlled oscillators) NCO1, NCO2, NCO3. A fourth NCO, NCO0 is actually a virtual oscillator in that it does not physically exist but is used to represent zero transmission, i.e. all three physical oscillators are switched off.

NCO0 is always used for zero transmission.

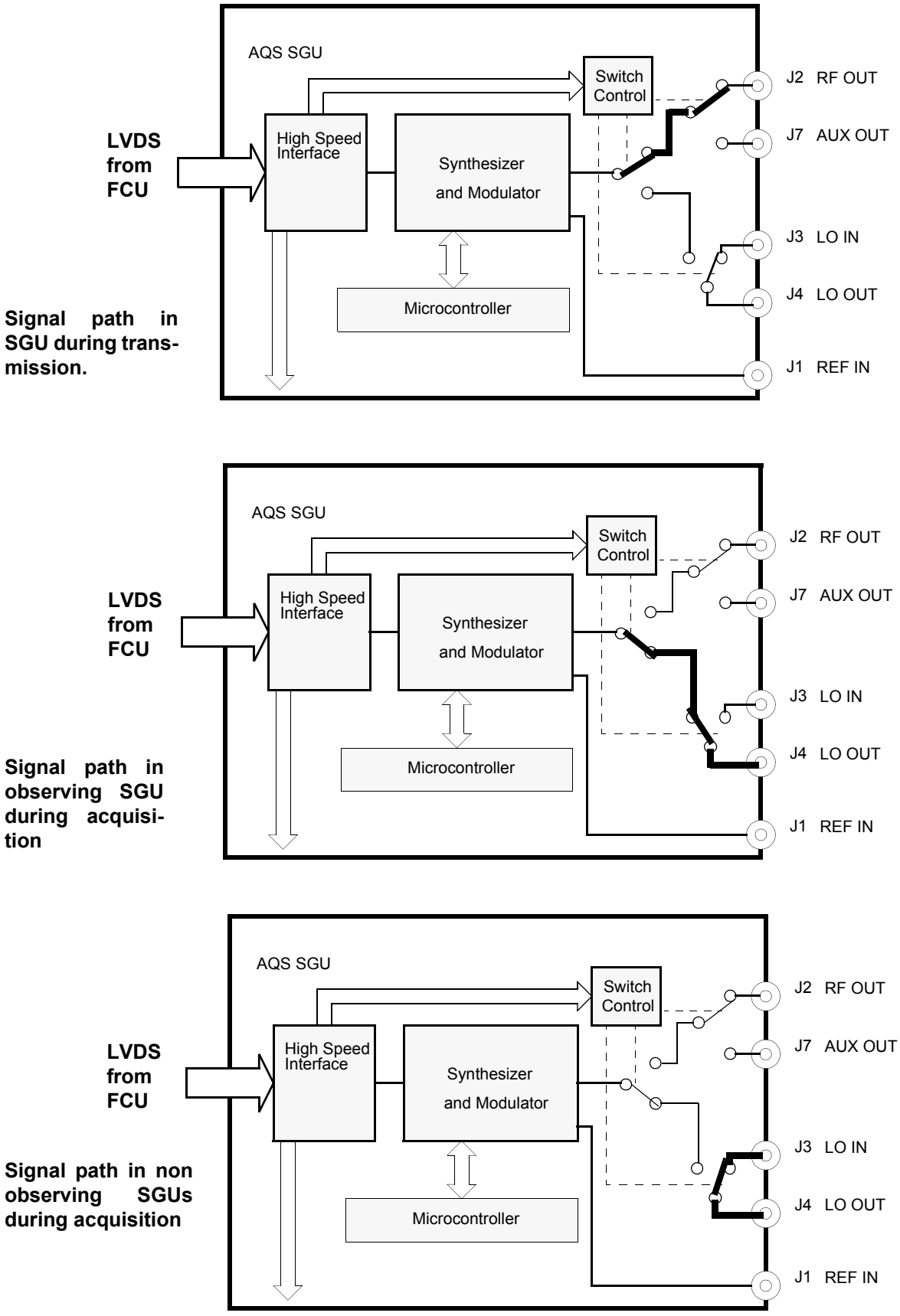
NCO1 is always used for the OBS frequency

Any shifts in frequency are implemented using NCO2.

NCO3 is always used for the LO frequency. This assignment of the various NCOs is illustrated in ***"NCO allocation" on page 208***

The advantage of using multiple NCOs is that frequency, amplitude and phase information can be loaded simultaneously. This facilitates instantaneous switching from one phase or frequency to another etc.

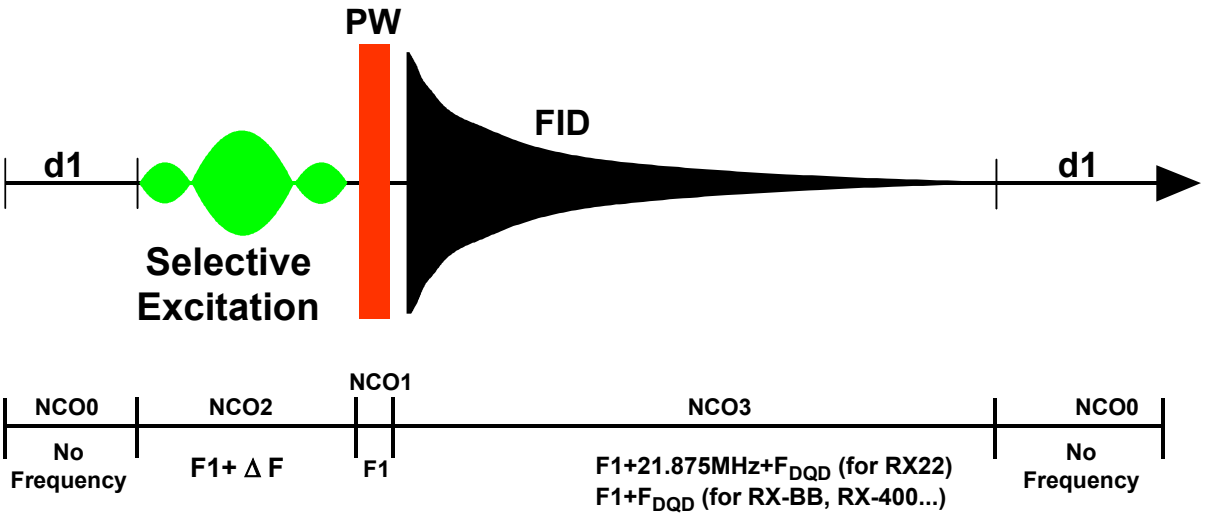
Figure 10.6. Signal paths within the SGU



The timing of the NCO output is controlled by a series of instructions delivered by the FCU via the LVDS with a 12.5ns timing resolution.

The output of the various NCOs is a digital representation of all characteristics of the required signal. This digital signal is then modulated using the 'MOD' input to implement the shape of the signal. The signal is still purely digital in nature but is then passed through a DAC to produce an analog output. The frequency at this stage is still not the final frequency, this only happens at the UP Converter which mixes the oscillator frequency with the appropriate frequency from the REF unit to produce the final transmission frequency. The last step is the application of the 'MULT' which sets the overall amplitude of the RF output.

Figure 10.7. NCO allocation



AQS Controller slot detection *10.7.2*

One SGU within the AQS chassis acts as low level bus controller AQS Controller) and initializes devices with I2C bus. The slot position of these SGU depends on the jumpers on the rear side of the AQS User Bus. For correct settings consult the chapters on configurations. With AQS/2 chassis the current and valid jumper setting is also apparent from the label below the mains selector on the rear side of the chassis.

- In **AQS** chassis jumper E must always be set
- In **AQS/2** chassis jumper E and F must always be set except in **multi receiver** systems, where these jumpers allow to separate the RGPs between two receiver sections

Unit Configuration / Version / Jumpers *10.8*

Five versions of SGUs have been produced.

- SGU-C Part-No. Z003329, output frequency range limited to 325MHz
- SGU400 Part-No. Z003642, output frequency range limited to 430MHz
- SGU600 Part-No. Z003831, output frequency range limited to 643MHz
- SGU1000 Part-No. Z003330, output frequency range limited to 1072MHz
- SGU-FTMS Part-No. Z003643, output frequency range limited to 10MHz

Key specifications and digital control behavior remain the same for all versions

Through the ‘cf’ routine the number and location of all installed SGUs including the AQS Controller SGU is determined. Each SGU in the user bus has a unique address by virtue of its physical position and this is used to distinguish the various SGUs from each other. There are no jumpers that need to be set.

Regardless of the system the units are lined up immediately to the left of the REF. unit.

A micro bay system will accommodate up to three SGUs.

A one bay system will accommodate up to four SGUs (three if internal amps are used)

A two bay system will accommodate up to 8 SGUs (4 attached to REF1 and 4 attached to REF2)

Any of the SGUs may be selected as the Observe SGU. In the ‘edsp’ menu the FCU number is equivalent to the SGU number and so this menu will easily tell the operator which SGU is the observing SGU.

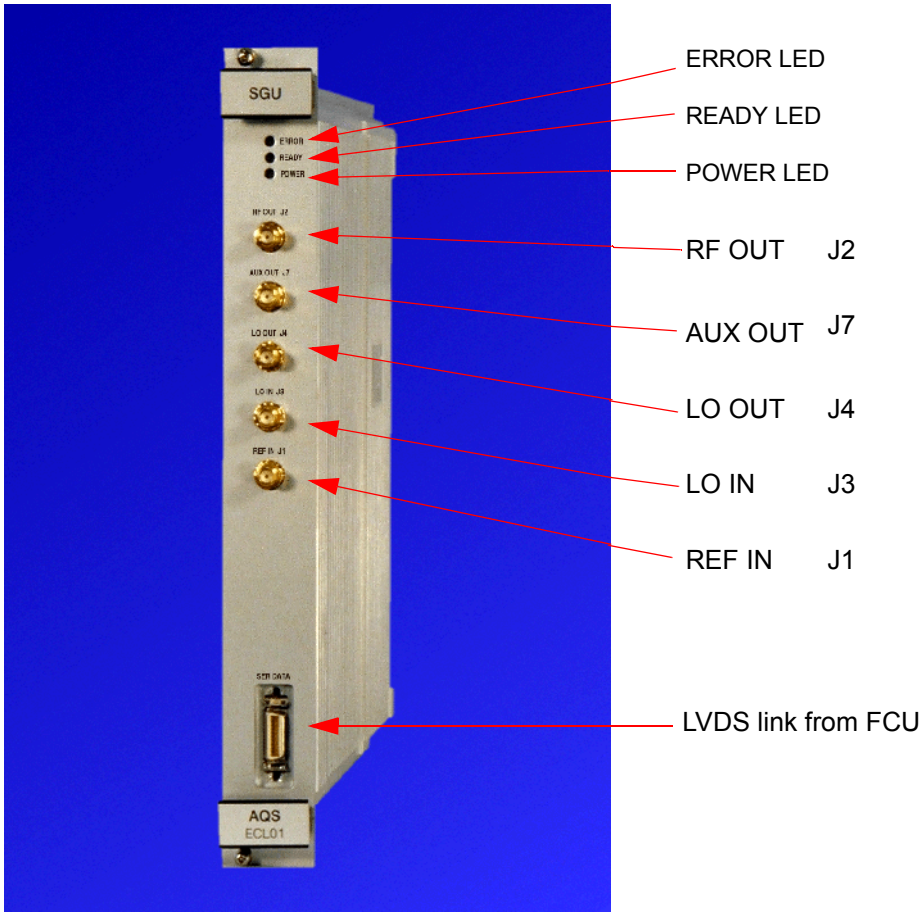
Table 10.4. Assignment of SGUs

Physical SGU	Physical FCU	edsp display
1	FCU1 Channel A	FCU1
2	FCU1 Channel B	FCU2
3	FCU2 Channel A	FCU3
4	FCU2 Channel B	FCU4

Differences from previous versions *10.8.3*

This is a completely new development for the AV series and the SGU does not have a counterpart in the AVANCE series.

Figure 10.8. SGU front panel



RF OUT J2

This is the single rf output which will be connected either directly to an internal amplifier input or to the router on its way to an external amplifier. This signal will have a max amplitude of 1Vpp at a power setting of -6db. The signal will only be present during pulse transmission as the blanking takes place on the SGU itself.

AUX OUT J7

The wobb signal ALWAYS comes from the AUX out of SGU-2 since this is hard wired to the 'Tuning in' input of the HPPR cover display module. On all other SGUs this output is left unconnected except for the case of SGU-1 where it can be connected to the 2HTX on an AQS with no router. The wobb signal will appear as a swept frequency whose variations in frequency will depend on the setting of 'wb-sw'. On the scope it appears typically as a pulsing frequency of maximal 1Vpp. (note that the wobble signal amplitude for HPPR/2 can be set by software, typical values are around 150mVpp)

The LO for the WOBB routine will come from the observing SGU LO OUT. This will also appear as a swept frequency except that this time the central frequency will be the wobble frequency + detection offset frequency (LO, DQD).

Since all SGU are physically identical the AUX OUT output would be capable of transmitting RF signal from any SGU but this would require explicit pulse programming.

LO OUT J4

RF signal for the receiver (1.0Vpp at 50 Ohm). The signal is generated on the observing SGU and then daisy chained through successive SGUs in the direction of the receiver. This signal will only be present during AQ (acquisition time) and if the SGU in question is the observing SGU or is located to the right (further along the daisy chain) of the observing SGU.

LO IN J3

This signal will only be present if the SGU in question is located to the right (further along the daisy chain) of the observing SGU (1.0Vpp at 50 Ohm).

REF in

Input RF signal from the REF. unit. This is a mixture of frequencies which are used to generate the final transmission frequencies.

Front Panel SGU-FTMS

The SGU FTMS has slightly different output connectors, because of the different receiver concept.

LO-I OUT J4

SYNT_0 signal for the ICR AQS FTMS HFU-RX A3147. This signal will only be present during AQ (acquisition time) and if the SGU in question is the observing SGU (-2dBm, 0.5Vpp at 50Ohm).

LO-Q OUT J3

SYNT_90 signal for the ICR AQS FTMS HFU-RX A3147. This signal will only be present during AQ (acquisition time) and if the SGU in question is the observing SGU (-2dBm, 0.5Vpp at 50Ohm).

LED Display *10.9.4*

Power LED:

The power LED indicates that **all** necessary voltages are present and at the correct level. If the voltage level drops then the LED will go out. Thus once the power LED lights then further investigation of the backplane to check the precise voltage is unwarranted.

The table below summarizes the states of the three front panel LEDS.

Table 10.5. LED States

ERROR (red)	READY (green)	POWER [a] (green)	Description
-	-	off	- Power supply not on or operating incorrectly
off	on	on	- **Normal sleep mode** - ready for operation - SGU microcontroller is powered down
off	periodically flashing, approx. twice a second	on	**With SGU firmware version birdal.hex or birdbg.hex and newer:** READY LED on the SGU front panel indicates with a ‚Heart Beat' flashing that the microcontroller is running. With all previous firmware versions the LED did not give any hint if the microcontroller is alive or not. During acquisition the microcontroller on the SGU is in power save or sleep mode and the READY LED must be in a steady state. The SGU board should always be in sleep mode, unless TopSpin is writing new configuration information or during ‚gs' or wobble. The sleep mode reduces power consumption, increases component reliability, improves thermal equilibrium and avoids electrical noise. For that Top-Spin 1.3 pl2 is necessary.
off	on resp. short-time flickering	on	- Communication LED. The unit has received a command from the RS485 bus master. The LED switches to off as soon as the SGU acknowledges the command.
blinking slowly (approx. 3 Hz)	on	on	- Indicates warning and not error. The sleep mode during acquisition is disabled (‘gs’ mode). Caution: Sensitive NMR experiments are not possible in this mode due to disturbances of the controller system.
blinking slowly (approx. 3 Hz)	off	on	- An error has occurred on the SGU
blinking fast	-	on	- Boot-mode Board not initialized yet or no application firmware found (e.g. because of power failure during firmware update).

a The power LED indicates that **all** necessary voltages are present and at the correct level. If any voltage level drops then the LED will go out. Thus once the power LED lights, further investigations on the backplane to check the precise voltage are unnecessary.

Part Numbers and Cables *10.10*

- SGU-C Part-No. Z003329 (325MHz)
- SGU400 Part-No. Z003642 (430MHz)
- SGU600 Part-No. Z003831 (643MHz)
- SGU1000 Part-No. Z003330(1072MHz)
- SGU-FTMS Part-No. Z003643 (10MHz)

Troubleshooting / Unit replacement / Tips 'n' Tricks *10.11*

General *10.11.5*

1. All SGUs are identical and as such are fully interchangeable. If units are swapped it is advisable to reconfigure to ensure that there are no inconsistencies in unit recognition. Note that for best performance all the SGUs should be of the same type. If SGU with different ECL were mixed ensure that the SGU with highest ECL is used as SGU-1.
2. Ensure that all SGUs are using the same firmware. This can be done using UniTool.
3. Even upon rebooting after a power off, the error LED on the AQS Controller SGU may light. It may be necessary to enter the command 'ii' (initialize interfaces) to clear this error.
4. Do not open the SGU in the field.
5. Ensure that the 20 pin cable to the FCU is connected before powering up the AQS. This will ensure the correct termination and also prevent the SGU from hanging.

Error Messages *10.11.6*

Description of possible error messages:

Table 10.6. AQS SGU error messages

Error No..	Error Message	Description	Possible cause
Error No. 1	Serial RS485 timeout	slave device did not answer in expected time	slave device probably not initialized, check connections
Error No. 2	Checksum	wrong firmware checksum	internal hardware error or download failed
Error No. 3	Watchdog	hardware malfunction, on-chip diagnostic activated	hardware failure
Error No. 4	Serial RS485 command, checksum error	RS485 protocol violation	spectrometer control software failure
Error No. 10	RAM selftest error	RAM test failed	hardware failure
Error No. 11	no application firmware found	ROM test failed	hardware failure or firmware download failed
Error No. 13	Power failed	indicate that a power up has happened and the system is not initialized	ordinary power up or a power breakdown during an experiment
Error No. 15	Parameter exceeds valid range	value out of range	spectrometer control software failure or faulty input using Unitool
Error No. 17	Function not supported by board hardware version	selected feature not supported by actual hardware version	spectrometer control software failure, wrong command selected using UniTool
Error No. 18	Unknown version index in configuration page	internal validation of calibration data failed	hardware error
Error No. 20	Syntax error	selected feature not supported by actual firmware, board does not understand command	spectrometer control software failure, wrong board selected, hardware feature not supported by actual version
Error No. 22	RTX create error	operating system error	firmware or hardware error on SGU
Error No. 23	RTXmemory allocation error		
Error No. 24	RTX memory free error		
Error No. 25	RTX communication pool exhausted		
Error No. 26	RTX send signal error		
Error No. 27	RTX interrupt handling error		
Error No. 28	RTX semaphore waiting list full		
Error No. 29	RTX pool create error		

Table 10.6. AQS SGU error messages

Error No..	Error Message	Description	Possible cause
Error No. 36	Flash byte program error"	failure during FLASH memory programming	hardware failure
Error No. 37	Flash erase error		
Error No. 40	Flash erase timer expired		
Error No. 41	Error in flash command sequence		
Error No. 42	Flash page mismatch, storing terminated		
Error No. 43	No valid calibration data		
Error No. 50	RAM selftest error	RAM test failed	hardware failure
Error No. 51	No application firmware found (wrong firmware checksum)	ROM test failed	download error or wrong firmware downloaded
Error No. 52	No application firmware found (wrong firmware name)	ROM test failed	download error or wrong firmware downloaded
Error No. 53	No application firmware found (wrong firmware ID)	ROM test failed	download error or wrong firmware downloaded
Error No. 58	Corrupt BIS on board	BIS (Board Information System) test failed	hardware failure
Error No. 59	BIS checksum error	BIS (Board Information System) test failed	hardware failure
Error No. 60	Unknown rack code	Unknown rack code	invalid jumper setting on chassis user bus
Error No. 100	Serial DAC bus (SPI, 8420) error	on board serial DACs for calibration can not be set	hardware failure
Error No. 101	Serial ASIC bus (JTAG) error	SGU on board hardware bus can not be written to or devices on internal JTAG bus can not be initialized	Reference signals from AQS REF not connected, coaxial cable defect or ACB/PSD defect
Error No. 102	Missing valid configuration page	configuration data (calibration data) not available	hardware failure
Error No. 105	Flash table does not exist, using default table	configuration data (calibration data) not available	hardware failure
Error No. 107	Table address or identifier exhausts range	selected table not supported by actual hardware version	spectrometer control software failure, wrong command selected using UniTool
Error No. 108	SGU PLL lock lost or PLL unlocked error	diagnostic detected improper hardware state	hardware failure
Error No. 109	SGU frequency range exceeded	value out of range	spectrometer control software failure or wrong SGU type in chassis (e.g. SGU400 in a AV600 system)
Error No. 110	Emergency stop activated, SGU reseted	an emergency stop signal from backplane detected	emergency stop signal activated by any spectrometer unit or BSMS keyboard

Table 10.6. AQS SGU error messages

Error No..	Error Message	Description	Possible cause
Error No. 111	FCU - SGU link checksum error, SGU reseted	indicate parity error, checksum of high speed data is not correct	illegal command from FCU, clock signal to FCU (High Speed Transmitter) not properly connected, high speed link cable not connected or frequency mixture from Reference Board not connected
Error No. 112	SBSB Wake-Up occurred during acquisition, SGU uP booted	SGU has been set to generate LO signal while the on-board microcontroller was running spectra may show spikes	spectrometer control software failure
Error No. 113	Function not allowed in present mode		spectrometer control software failure
Error No. 115	Board overheated, check AQS cooling and ventilation system !	on-board diagnostic detected board temperature of > 75°C	fans/ventilation broken down, power supply defect
Error No. 116	Power supply failure detected	on-board diagnostic detected drop of power supply voltages below specified range	power supply defect or on board voltage regulator failure
Error No. 200	Can not initialize board	AQS Controller cannot initialize salve board while power up chassis scan sequence	firmware version not compatible, hardware failure on AQS Controller or slave backplane connection
Error No. 201	Can not read board information	AQS Controller cannot get board information from slave unit while power up chassis scan sequence	firmware version not compatible, hardware failure on AQS Controller or slave backplane connection
Error No. 202	Can not read board firmware version	AQS Controller cannot read board firmware version from salve board while power up chassis scan sequence	firmware version not compatible, hardware failure on AQS Controller or slave backplane connection
Error No. 203	Can not write board identifier to slave	AQS Controller cannot write board identifier to salve board while power up chassis scan sequence	firmware version not compatible, hardware failure on AQS Controller or slave backplane connection
Error No. 204	Can not write SBSB address to slave	AQS Controller cannot write SBSB address to salve board while power up chassis scan sequence	firmware version not compatible, hardware failure on AQS Controller or slave backplane connection
Error No. 210	Serial DAC bus (SPI, 8420) error	serial DACs for calibration on REFERENCE BOARD can not be set	hardware failure
Error No. 211	No I2c acknowledge received	AQS Controller can not access backplane I2C bus	one of the AQS units blocks up the backplane I2C bus or on board hardware failure
Error No. 212	I2c EEROM program timer expired	EEPROM for BIS entries can not be accessed	one of the AQS units blocks up the backplane I2C bus or on board hardware failure
Error No. 213	Serial ASIC bus (JTAG) error	REFERENCE BOARD on board hardware bus can not be written to or devices on internal JTAG bus can not be initialized	hardware failure
Error No. 215	Rack I2c bus not released error	AQS Controller can not access backplane I2C bus	one of the AQS units blocks up the backplane I2C bus or on board hardware failure

Table 10.6. AQS SGU error messages

Error No..	Error Message	Description	Possible cause
Error No. 216	Unknown board in rack	AQS Controller cannot identify board while power up chassis scan sequence	firmware version not compatible, incompatible board in chassis
Error No. 217	Rackconfiguration not allowed	improper combination of boards in chassis detected by AQS Controller	some boards are not compatible to each other (e.g. REF22 and AQS RX-BB)
Error No. 218	Illegal slot occupation detected (I2C and SBSB device use same slot address)	I2C and SBSB device use same slot address	wrong AQS chassis code set in 2 chassis systems, hardware failure on backplane or according units
Error No. 220	Board timeout	slave board answered not within specified time	firmware version not compatible or hardware failure
Error No. 221	Rackmaster task interrupted by slave behavior	slave board answered not in expected order	firmware version not compatible or hardware failure
Error No. 222	Reference Board missing or can not be detected	no reference board found during rack scan	BIS error on REF, I2C bus failure, PSD board failure, wrong rack code jumper setting
Error No. 232	Different SGU firmware in AQS detected, download latest version on all SGU's	AQS Controller detected different SGU fimrware version that may cause improper operation	firmware version different, download latest version on all SGU's
Error No. 249	serious amplifier malfunction, error can not be deleted	hardware diagnostic on BLA2BB can not be reseted	hardware failure on BLA2BB or power supply
Error No. 250	no amplifier housing information in BIS, using default address	no amplifier housing information in BIS found while power up chassis scan sequence	no amplifier housing information in BIS
Error No. 251	multiple amplifier housing information in BIS, using default address	not valid amplifier housing information in BIS found while power up chassis scan sequence	not valid amplifier housing information in BIS found
Error No. 252	general fault detected	hardware diagnostic on BLA2BB detected	hardware failure on BLA2BB
Error No. 253	thermal fault detected	hardware diagnostic on BLA2BB detected	
Error No. 254	power supply fault detected	hardware diagnostic on BLA2BB detected	

Diagnostic Tests *10.12*

Not applicable

Power supplies and board temperature are checked periodically by the on-board microcontroller.

Software / Useful Pulse Programs 10.13

Each SGU has 10 RTP outputs. They are set automatically with the go command in pulse programs. To set specific RTPs permanently, the syntax

setrtp<sgu1..8> | <bit0-8> ^ <bit0-8> is used.

Example:

setrtp1|0|1|2|8^7

; set bits 0,1 , 2 and 8 and clear bit 7 on SGU 1

The RTP-bit-settings of different SGUs are combined at the backplane of the acquisition rack, so in fact it doesn't matter which SGU issues these pulses, but in order to avoid conflicts one should use the observe SGU for them.

Table 10.7. real time pulses

Bit #	Name	Meaning
Bit 0	RGP_ADC	ADC gating pulse
Bit 1	RGP_RX	Receiver gating pulse
Bit 2	RGP_HPPR	Preamplifier gating pulse
Bit 3-5	reserve	
Bit 6	INTERLEAVE_INCR	selector for gain switching in receiver
Bit 7	DWL_CLK or DWELL ENABLE	dwell time for receiver ADC
Bit 8	ADC_SEL0[a]	selects HADC/2 or SADC+
Bit 9	ADC_SEL1[b]	selects FADC

a not used in systems with DRU

b not used in systems with DRU

Fast Real Time Pulses (FRTP) 10.14

Each SGU has 4 FRTP outputs. They are set automatically with the pulse commands in pulse programs and CPD programs. To set specific FRTPs permanently, the command setfrtp<sgu1..8>|<bit0-8>^<bit0-8> is used.

Example:

setfrtp1|1

; set bit 1 on SGU 1 into FRTP register.

Bit1 is used for the amplifier blanking, Bits 0, 2 and 3 are reserve.

The amplifier blanking information is routed to the correct amplifier according to the router setting (edasp command and parameter RSEL, respectively).

Homodecoupling 10.14.7

The following SGU versions are equipped with an additional feature:

- SGU400 Part-No. Z003642 (430MHz) ECL 03 and higher

- SGU600 Part-No. Z003831 (643MHz) ECL 01 and higher
- SGU1000 Part-No. Z003330(1072MHz) ECL 04 and higher

These boards allow the usage of one FRTP pulse for gating another SGU synchronously. While one SGU controls the experiment by generating the LO signal and the real-time pulses for acquisition another SGU may be used as decoupling SGU. The observing SGU can now gate the decoupling SGU with a pulse in a way that the MOD and MULT are set to zero and the most conceivable suppression of the decoupling signal is achieved.

Important: When using this feature, all SGU involved in the experiment must have the same hardware version (minimal required ECL is given above).

Important signals *10.15*

All signals described below are active low and TTL except for the blanking signals which use an open drain configuration.

BLKTR (amplifier blanking pulses)

A SGU can control up to 8 power amplifiers with the corresponding BLKTR. The timing of the blanking pulses is controlled by the FCU via the LVDS which delivers real-time instructions in 50ns second bursts. All SGUs are capable of generating blanking pulses.

The internal amps receive the blanking directly from the backplane, whereas the external amps receives the signals from the PSD which in turn receives the signals from the backplane.

RGP_PA~ (Preamplifier receiver gating pulse)

This pulse is generated by the observe SGU and is used to gate the OBS module on the HPPR and used to implemented the transmit/ receive switching. The timing of the pulse can be modified with the ‘edscon’ parameters. This signal is routed via the ACB-S standard (or PSD) to the observe module in the preamplifier HPPR or HPPR/2. All other non lock HPPR modules are left permanently in transmission mode. In contrast to AVANCE systems, the preamplifier RGP will not be connected to the AQR RX22. The EP-HPPR output of the RX22 is left unconnected.

RGP_LO~ (Local oscillator gating pulse)

This pulse is generated by the observe SGU and initiates the frequency step to generate the LO frequency (SFO1+22MHz). The pulse is also used to control the LO output of the REF unit which will only be present when *RGP_LO* goes active low.

RGP_RX~ (Receiver gating pulse)

This pulse generated by the observing SGU controls the opening and closing of the receiver (RX22, RX-BB, RXAD) and is transmitted directly over the backplane. The timing of the pulse can be modified with the ‘edscon’ parameters.

RGP_ADC~ (ADC gating pulse)

This pulse (also driven by the observe SGU) controls the ADC data. If the pulse is low and a dwell clock (RCU systems) or dwell enable (in DRU systems) is applied,

the ADC will perform a conversion. If the pulse is high and a dwell clock / dwell enable is applied, the ADC generates ‘zero’ data. The RGP_ADC is routed over backplane to the ADC. This signal is specially used for digital homodecoupling with oversampling.

Dwell_Clk~ (ADC dwell clock for systems with RCU)

The signal is driven by the observe SGU and is used to control the timing of the AD conversions. Every falling edge of the dwell clock executes an ADC conversion. Although the signal is generated on the SGU, the timing is controlled totally by the FCU via the LVDS. The pulse is routed over the backplane to the ADC via the RX22. Homodecoupling experiments are treated as typical pulse programs.

DWELL_ENABLE~ (ADC dwell clock enable for systems with DRU)

The signal is driven by the observe SGU and is used to control the timing of the AD conversion. A low level of this signal enables ADC conversion. Although the signal is generated on the SGU, the timing is controlled totally by the FCU via the LVDS. The pulse is routed over the backplane to the RXAD.

SEL_ADCx~ (Select A/D converter, ONLY systems with RCU)

The signal is applied to select a required ADC in the case of configurations with more than one ADC. The signal is generated by the observe SGU and is wired directly via the backplane to the specified ADCs. see ***"real time pulses" on page 218***

Specifications *10.16*

Timing

Minimum Pulse or delay duration: see specification of TCU/FCU

Time Resolution: 12.5ns

The resolution is set by the internal 80MHz clocking frequency on-board the TCU3. Pulses or delays between pulses can thus be set to 50, 62.5, 75, 87.5ns, etc.

Frequency

Frequency Range SGU-C:	5-325	MHz
Frequency Range SGU400:	5-430	MHz
Frequency Range SGU600:	5-643.450	MHz
Frequency Range SGU1000:	5-1072.625	MHz
Frequency Range SGU-FTMS:	0,003-10	MHz

Frequency Stability: This is governed by the stability of the crystal oscillator on the REF. unit which is specified to 3 $x10^{-9}$/day and 1 $x10^{-8}$/year

Frequency Resolution: The DDS is clocked by 80MHz and the frequency setting is stored in a 34 bit register $\rightarrow$ 80 MHz/2^{34} <0.005 Hz.

Frequency Switching Time:

Instruction time for frequency steps: 100ns with resolution of 12.5ns

Further information on response time of analog hardware: see section ***"Hardware response" on page 222***

Phase

Phase Resolution: A 16 bit register is used to store phase values.
$\rightarrow$ 360°/2^{16} < 0.006°

Phase Switching Time:

Instruction time for phase steps: 50ns with resolution of 12.5ns

Total response time for any phase step to a phase error with less than 1° <300ns

Further information on phase settling time: see section ***"Hardware response" on page 222***

Amplitude

Modulator Range: The Modulator values are stored in a 16 bit register which equates to a voltage dynamic range of 96dB. (20 log(2^{16}) =96 dB).

Power Level Range: The Power Level values are stored in a 15 bit register which equates to a voltage dynamic range of 90dB. (20 log(2^{15}) =90 dB)

Power Level resolution: 0.1 dB

Amplitude switching time:

Instruction time for amplitude: 50ns

Response time of analog hardware: <100ns

Hardware response *10.16.8*

The SGU frequency registers can be set within 25ns, the actual update rate is limited by the serial link and the event synchronization to 100ns. The SGU phase, shape (MOD) or amplitude (MULT) registers can be set within 12.5ns each, the actual update rate is limited by the serial link and the event synchronization to 50ns. There is a finite bandwidth within the analog sections of the SGU resulting in a response or settling time respectively.

The settling time is independently of change frequency or phase. A quite hard test is to change phase by 180° and measure the time elapsed to achieve an remaining error of <1°.

Figure 10.9. Response 180° phase step

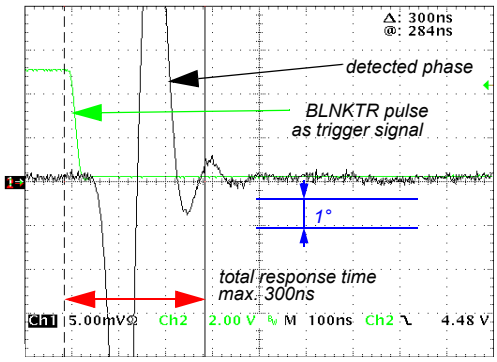
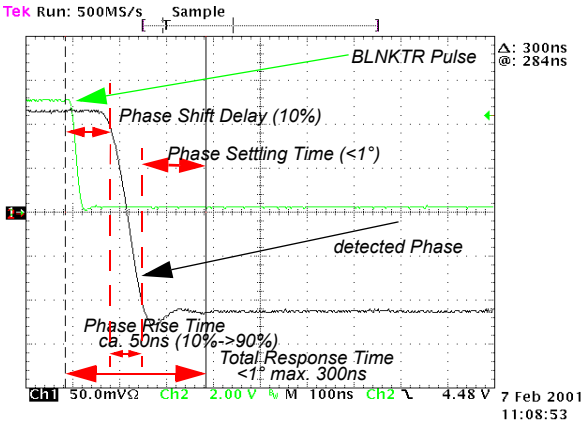


Figure 10.10.Response 90° step (45°/+135°)



Power Supply / Fuses *10.17*

See ***10.9.4***

Backplane Connector *10.17.9*

Table below is a list of the various signals transmitted to all user slots via the middle rear 110 pin connector J0.

Table 10.8. Backplane Connector

	z	a	b	c	d	e	f
1	GND	GND	RESERVE_1	NC	GND	SAMPLE_INFO0	GND
2	GND	NC	GND	SAMPLE_INFO3	SAMPLE_INFO2	SAMPLE_INFO1	GND
3	GND	GND	NC	RESERVE_2	GND	SAMPLE_INFO4	GND
4	GND	20MHZ_CLK_X [a]	GND	INTERLEAVE_INCR	ADC_SEL1	ADC_SEL0	GND
5	GND	GND	20MHz_CLK_X	RESERVE_3	GND	RGP_LO	GND
6	GND	BLNKTR1	GND	BLNKTR2	RESERVE_6	RESERVE_4	GND
7	GND	BLNKTR3	BLNKTR4	NC	GND	RGP_ADC	GND
8	GND	BLNKTR5	GND	BLNKTR6	RESERVE_7	DWL_CLK/DWL_EN	GND
9	GND	BLNKTR7	BLNKTR8	NC	GND	RGP_RX	GND
10	GND	SBS_TTL_TX	GND	SBS_TTL_RX	SBS_TTL_TX_ENAB	RESERVE_5	GND
11	GND	LOCAL_TX	LOCAL_RX	SBS_TTL_WUP	GND	RGP_HPPR	GND

Magenta = CCU-Bus galvanically isolated
Blue = Intra Rack Bus

Key Area

15	GND	SLOT2	SLOT1	SLOT0	GND	NC	GND
16	GND	SLOT3	GND	I2C_SDA	NC	GND	GND
17	GND	EMERGENCY_STOP	I2C_BUS_REQ	I2C_SCL	GND	NC	GND
18	GND	NC	GND	I2C_2_SDA	I2C_2_SCL	GND	GND
19	GND	NC	NC	NC	GND	NC	GND
20	GND	NC	GND	P2V	N2.5V	GND	GND
21	GND	P5V	P35V	P9V	P9V	P9V	GND
22	GND	P5V	RACK0	N9V	N9V	N9V	GND
23	GND	P5V	P19V	N19V	RACK1	P12V	GND
24	GND	P5V	P19V	N19V	RACK2	P12V	GND
25	GND	P5V	P19V	N19V	RACK3	P12V	GND

a x = Slot-No. (20MHZ_CLK_1 until 20MHZ_CLK_8)

AQS Pulse & RF-Splitter 11

Introduction 11.1

The AQS PULSE SPLITTER and AQS RF-SPLITTER boards are used for the following signal distribution between AQS/2 or AQS/3 and AQS/2-M chassis:

- 20MHz clock
- 11 receiver (RX) pulses (RGP_LO~, RGP_ADC~, RGP_RX~, RGP_HPPR~, DWL_ENAB, INTRLEAVE_INCR~, SAMPLE_INFO[0:4] ~)
- LO-signal
- LO2-signal

The PULSE SPLITTER board is situated in one of the AQS slots in the front of the AQS/2 or AQS/3 chassis, the RF-SPLITTER in the rear of the AQS/2-M chassis.

PULSE and RF-SPLITTER are connected via a twisted pair cable with Mini-Delta-Ribbon (MDR) connectors. The cable has a differential impedance of 100Ω.

One PULSE SPLITTER can support up to 5 AQS/2-M chassis. Each AQS/2-M chassis needs one RF-SPLITTER board.

LO- and LO2-signals are split in the RF-SPLITTER. Each splitter has one input and 10 outputs. The LO-splitter has an additional input and LO-switch. All splitters are unity gain calibrated. Up to 3 RF-SPLITTER boards can be cascaded.

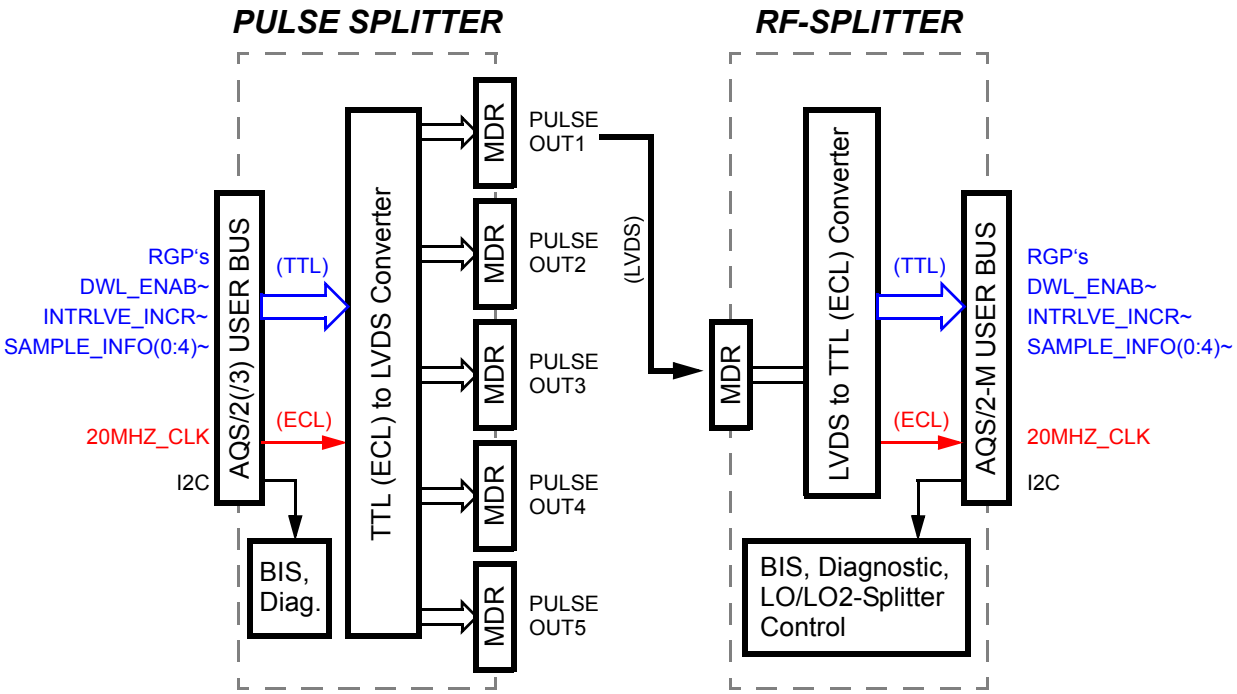
Both units are equipped with I2C-bus and LED indicator diagnostic features. Gain calibration and LO-switch of the splitters are I2C-bus controlled.

Functions/Description 11.2

20MHz Clock and RX-Pulse Distribution 11.2.1

The PULSE SPLITTER board receives both clock and RX-pulses from the user bus and converts them to LVDS-logic level signals. These are transmitted via the MDR-cable to the RF-SPLITTER. It converts them back to their former logic levels and routs them to the user bus.

Figure 11.1. Clock & RX-Pulse distribution



LO- & LO2-Splitter **11.2.2**

Both LO- and LO2-splitters are integrated into the RF-SPLITTER unit.

The LO-output signals from SGU1 and SGU2 are fed into the inputs LO_IN1 and LO_IN2. The outputs are either connected to a RXAD or a LO-splitter input on another RF_SPLITTER unit.

The LO2 output signal from the REFERENCE board is fed into the LO2_IN1. The outputs are either connected to a RXAD or a LO2-splitter input on another RF_SPLITTER unit.

Figure 11.2. LO/LO2- Splitter

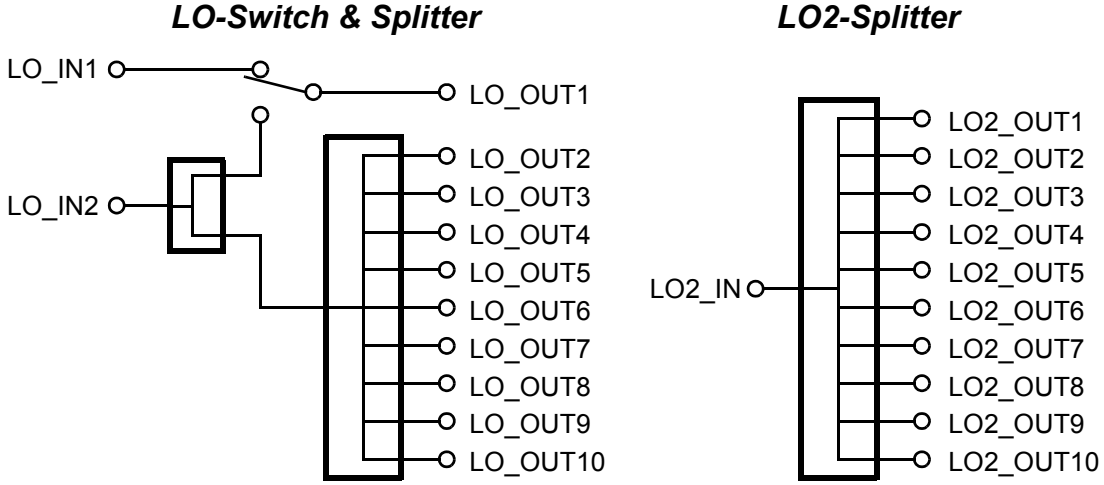
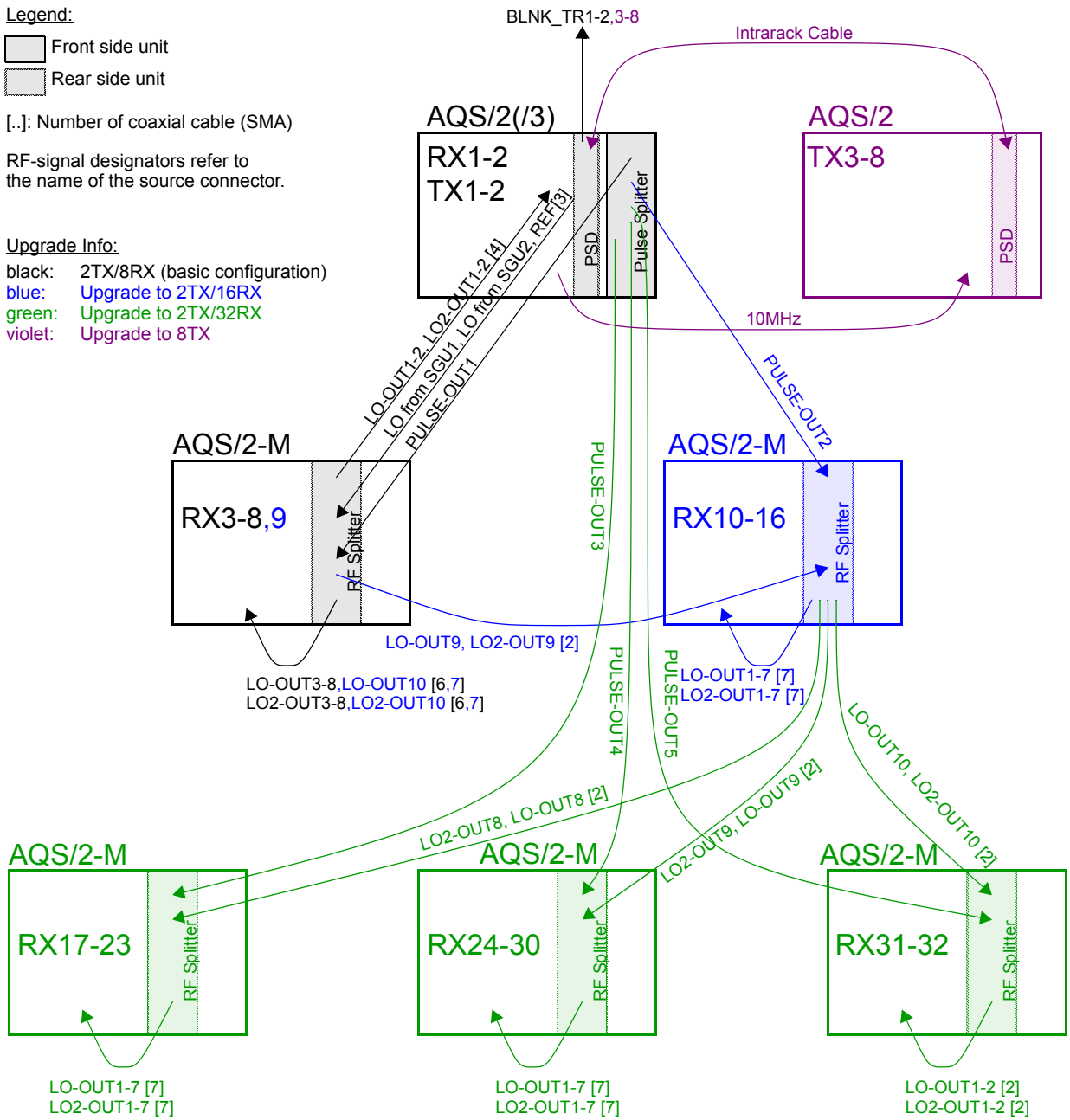
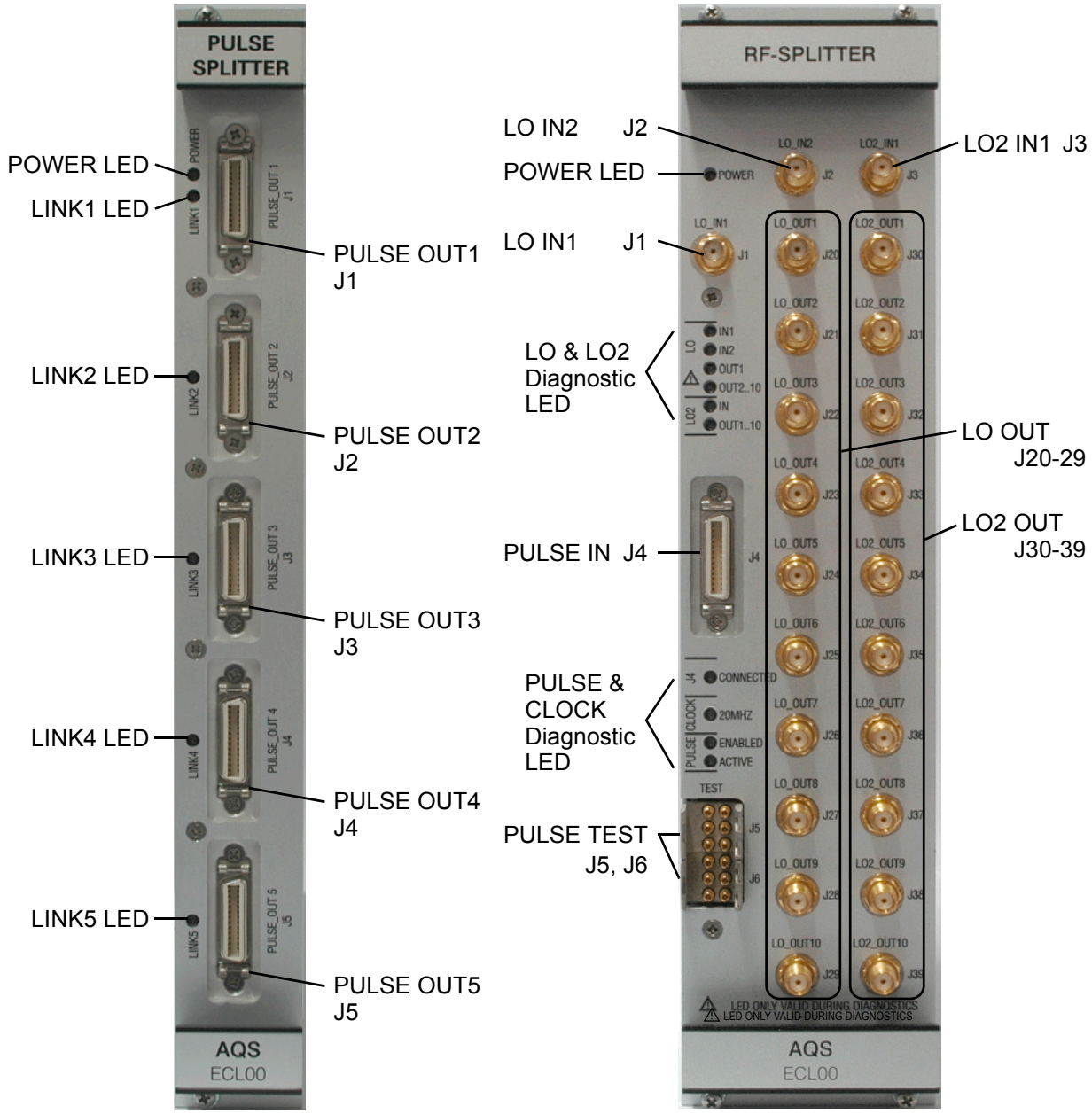


Figure 11.3. PULSE & RF-SPLITTER Wiring Diagram



Front Panel *11.4*

Figure 11.4. AQS PULSE- & RF-SPLITTER boards front panel view



LED Indicators 11.4.1

Table 11.1. PULSE SPLITTER LED Error Description

LED Name	Color	Error Description (LED OFF)
POWER	green	power supply failure
LINK1 LINK2 LINK3 LINK4 LINK5	green	MDR cable not connected to AQS RF-SPLITTER

Table 11.2. RF-SPLITTER LED Error Description

LED Name		Color	Error Description (LED OFF)
POWER		green	power supply failure
LO	IN1 IN2 OUT1 OUT2-10	yellow [a] yellow [a] yellow [a] yellow [a]	no RF-input signal no RF-input signal no RF-output signal no RF-output signal
LO2	IN OUT1-10	green green	no RF-input signal no RF-output signal
J4	CONNECTED	green	MDR cable not connected to AQS PULSE SPLITTER, no pulse output
CLOCK	20MHZ	green	no clock output signal
PULSE	ENABLED ACTIVE	green yellow [a]	pulse buffer disabled, no pulse output no pulse active

a Short pulses may not be visible in OBSERVE mode.

Front Panel Connectors PULSE SPLITTER 11.4.2

J1-J5 PULSE OUT1-5

Pulse and clock output to RF-SPLITTER board. All signals are in LVDS logic (Low Voltage Differential Signal). These signals can only be measured with proper LVDS termination (100Ω differential).

J1 LO_IN1

LO input signal (1Vpp at 50Ω load) from SGU1 or SGU LO-chain. This signal is only present during observe. It can be routed via the internal LO-switch to LO_OUT1 (J20).

J2 LO_IN2

LO input signal (1Vpp at 50Ω load) from SGU2 or SGU LO-chain. This signal is only present during observe. It is split and routed to LO_OUT2-10 (J21-29). It can also be routed via the internal LO-switch to LO_OUT1 (J20).

J3 LO2_IN1

LO2 input signal (1Vpp at 50Ω load) from REFERENCE board. This signal is split and routed to LO2_OUT1-10 (J30-39).

J4 PULSE IN

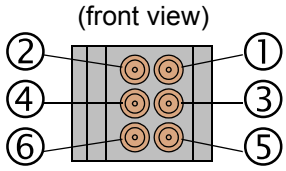
Pulse and clock input from PULSE SPLITTER. All signals are in LVDS logic.

J5/J6 TEST

Pulse and clock output test connector. Signal level = 1/10 TTL at 50Ω load.

Table 11.3. Pining J5/J6 Pulse Test Connector [1]

	J5		
RGP_ADC~	②	①	RGP_LO~
RGP_HPPR~	④	③	RGP_RX~
20MHZ_CLOCK	⑥	⑤	DWL_ENAB~
	J6		
SAMPLE_INFO(0)~	②	①	INTRLVE_INCR~
SAMPLE_INFO(2)~	④	③	SAMPLE_INFO(1)~
SAMPLE_INFO(4)~	⑥	⑤	SAMPLE_INFO(3)~



J20-29 LO_OUT1-10

LO output signal (1Vpp at 50Ω load) to RXAD or another RF-SPLITTER. These signals are only present during observe.

J30-39 LO2_OUT1-10

LO2 output signal (1Vpp at 50Ω load) to RXAD or another RF-SPLITTER.

1 Pin numbers according to test cable HZ10124 (CABLE 6P300 COAXIPACK ADAP BNC)

Diagnostics 11.5

The input signals of the PULSE SPLITTER and the output signals of the RF-SPLITTER are monitored by diagnostic circuits. Their status is displayed with LED indicators on the front panel of the units. Please refer to ***"LED Indicators" on page 229***.

The same information is accessible for the AQS controller via I2C bus. The information may be accessed via the DRU web interface.
(Service web of DRU in Slot 1, see Main / Hosted Devices)

Figure 11.5. Pulse Splitter Device and Diagnostic Status

Device Status

Ready

Diagnostic

Diagnostic Testpoint	Description	Status
①	Power Supply Monitor (+3.3V, +5V)	o.k.
②	Pulse Input *	all pulses inactive
③	20MHz Clock Input	o.k.
④	LINK 1 (PULSE_OUT 1 J1)	connected
⑤	LINK 2 (PULSE_OUT 2 J2)	not connected
⑥	LINK 3 (PULSE_OUT 3 J3)	not connected
⑦	LINK 4 (PULSE_OUT 4 J4)	not connected
⑧	LINK 5 (PULSE_OUT 5 J5)	not connected
Refresh	Refresh F5	

click picture to enlarge

* pulses only active during acquisition

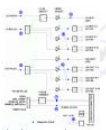
Figure 11.6. RF-Splitter Device and Diagnostic Status

Device Status

Ready

Diagnostic

Diagnostic Testpoint	Description	Status
①	LO IN1 *	inactive or failed
②	LO IN2 *	inactive or failed
③	LO OUT1 *	inactive or failed
④	LO OUT 2-10 *	inactive or failed
⑤	LO2 IN	failed
⑥	LO2 OUT 1-10	failed
⑦	Pulse Output *	all pulses inactive
⑧	20MHz Clock Output	ok
⑨	Power Supply Monitor (+3.3V, +5V)	ok
Refresh	Refresh F5	

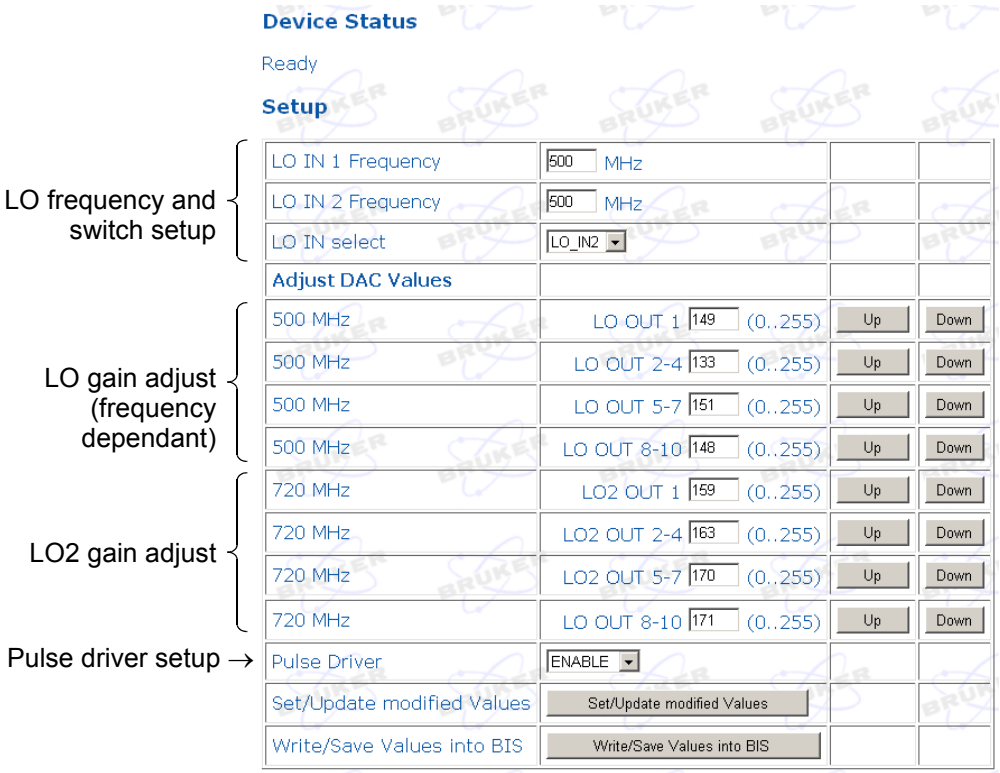


click picture to enlarge

* LO and pulses only active during acquisition

RF-Splitter Setup and Gain Adjust 11.6

Figure 11.7. RF-Splitter Setup Window



Setup 11.6.1

LO IN 1, LO IN 2 Frequency:

- Enter SGU frequency and press [Set/Update modified Values]

The adjust DAC values are set according to the calibration data list stored in the unit BIS. The controller uses the calibration data closest to the entered frequency value. The frequency display changes to the chosen data set.

LO IN select:

LO switch setting (see also ***"LO/LO2- Splitter" on page 226***)

- LO_IN1 = LO_IN1 → LO_OUT1 and LO_IN2 → LO_OUT2-10
- LO_IN2 = LO_IN2 → LO_OUT1-10

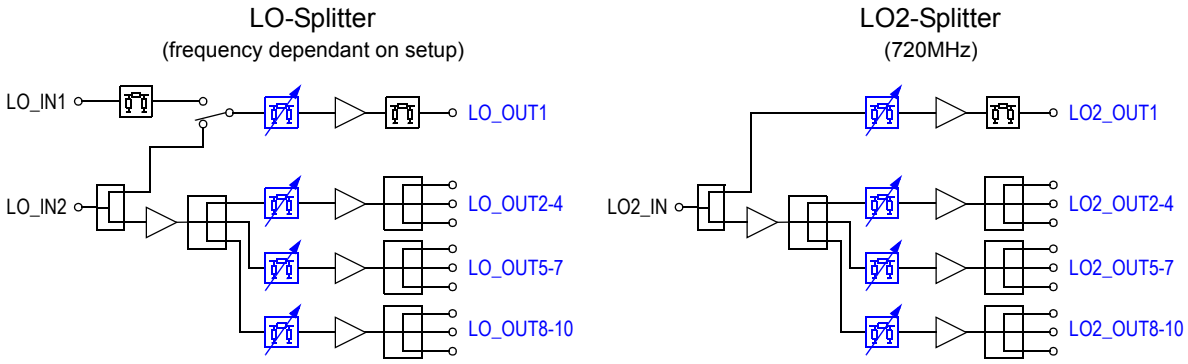
Pulse Driver:

- ENABLE = pulse driver from RF-Splitter to backplane enabled (Default)
- DISABLE = pulse driver from RF-Splitter to backplane disabled (only used when SGU in AQS/2-M Chassis)

Gain Adjust 11.6.2

The gain off the LO and LO2 splitters is adjusted to unity gain at the factory. This includes the connecting cables[1]. However if other cables are used or several RF-Splitters are cascaded, a fine adjust may be necessary. The gain adjusts are bundled as follows:

Figure 11.8. RF-Splitter gain adjust DAC



Gain Adjust Procedure:

- Disconnect the LO(2)_OUT cable from the RXAD and connect it to a power meter
- Check/set the correct RF-Splitter frequency
- Adjust the gain of the LO channel with the [Up] and [Down] buttons (Adjust value see ***"LO-Performance:" on page 234***)
- Save the DAC values with [Write/Save Values into BIS]
- Repeat the procedure for other frequencies or other LO channels

! ***Important Note:***

- Make sure that all unused outputs are properly terminated (50Ω)
- The four gain adjusts of the splitters are somewhat dependant on each other. If one channel is coarse adjusted, the other channels may detune slightly.

Part Numbers and Cables 11.7

- Z104431 AQS PULSE SPLITTER
- Z104432 AQS RF-SPLITTER
- HZ13238 CABLE RD 26P 3M MDR

Test Equipment:

- HZ10124 CABLE 6P300 COAXIPACK ADAP BNC

1 2x CABLE COAX ELSPEC 2000 SMA/SMA (HZ04329)

Technical Data *11.8*

PULSE SPLITTER *11.8.1*

Pulse Performance:

Pulse Input:	+5V TTL Logic Level
20MHz Clock Input:	+2/-2.5V ECL Logic Level
LVDS Output:	LVDS Logic Level

RF-SPLITTER *11.8.2*

LO-Performance:

Input Power:	+4.5 ±0.5	dBm
Frequency Range:	50..800	MHz
Insertion Loss: LO_IN1 → LO_OUT1 (dual LO mode)	0 ±0.5	dB
Insertion Loss: LO_IN2 → LO_OUT1..10	0 ±0.5	dB
LO-Switch Isolation: LO_IN1 → LO_OUT1 (single LO mode)	> 20	dB
LO-Switch Isolation: LO_IN1 → LO_IN2 (dual LO mode)	> 20	dB
VSWR: all Ports	≤ 1.4	

LO2-Performance:

Input Power:	+4 ±0.5	dBm
Frequency:	720	MHz
Insertion Loss : LO2_IN → LO2_OUT1..10	0 ±0.5	dB
VSWR: all Ports	≤ 1.4	

Pulse Performance:

LVDS Input:	LVDS Logic Level
Pulse OUT:	+5V TTL Logic Level
20MHz Clock OUT:	+2/-2.5V ECL Logic Level
Pulse & Clock Test OUT: (at 50Ω load)	1/10 TTL Logic Level

Power Supply / Fuses *11.9*

Both units are powered via their backplane connector from the user bus. For power supply status see ***11.4.1***. The units do not contain any fuses.

Backplane Connector *11.9.1*

Table 11.4. Pining user bus connector PULSE-SPLITTER (Slot 1-10, AQS/2, AQS/3)

	z	a	b	c	d	e	f
1	GND	GND			GND	SAMPLE_INFO0	GND
2	GND		GND	SAMPLE_INFO3	SAMPLE_INFO2	SAMPLE_INFO1	GND
3	GND	GND		I2C_STATUS_INT~	GND	SAMPLE_INFO4	GND
4	GND	20MHZ_CLK_X [a]	GND	INTERLEAVE_INCR~			GND
5	GND	GND	20MHz_CLK_X~ [a]		GND	RGP_LO~	GND
6	GND		GND				GND
7	GND				GND	RGP_ADC~	GND
8	GND		GND			DWL_ENAB~	GND
9	GND				GND	RGP_RX~	GND
10	GND		GND				GND
11	GND				GND	RGP_HPPR~	GND

Key Area

15	GND	SLOT(2)	SLOT(1)	SLOT(0)	GND		GND
16	GND	SLOT(3)	GND	I2C_SDA		GND	GND
17	GND		I2C_BUS_REQ~	I2C_SCL	GND		GND
18	GND		GND	I2C_2_SDA	I2C_2_SCL	GND	GND
19	GND				GND		GND
20	GND		GND			GND	GND
21	GND	P5V					GND
22	GND	P5V					GND
23	GND	P5V					GND
24	GND	P5V					GND
25	GND	P5V					GND

a x = Slot-Nb.

Table 11.5. Pining user bus connector RF-SPLITTER (Slot RF-SPLITTER (AUX2), AQS/2-M Rear Side)

	z	a	b	c	d	e	f
1	GND	SLOT4	SLOT3	SLOT2	SLOT1	SLOT0	GND
2	GND	I2C_SCL	I2C_SDA	I2C_BUS_REQ~	I2C_2_SCL	I2C_2_SDA	GND
3	GND	LOCAL_TX	LOCAL_RX	INTRA_STATUS_INT~	I2C_STATUS_INT~		GND
4	GND						GND
5	GND	GND	GND	GND	GND	GND	GND
6	GND	P12V	P12V	P12V	P12V	P12V	GND
7	GND						GND
8	GND	RESERVE(5)	RESERVE(4)	EMERGENCY_STOP~			GND
9	GND						GND
10	GND	P5V	P5V	P5V	P5V	P5V	GND
11	GND	GND	GND	GND	GND	GND	GND

Key Area

15	GND	GND	GND	GND	GND	GND	GND
16	GND	P9V	P9V	P9V	P9V	P9V	GND
17	GND	N9V	N9V	N9V	N9V	N9V	GND
18	GND	GND	GND	GND	GND	GND	GND
19	GND						GND
20	GND						GND
21	GND	GND	GND	GND	GND	GND	GND
22	GND			SAMPLE_INFO(0)	DWL_ENAB~	RGP-LO~	GND
23	GND	GND	SAMPLE_INFO(2)	SAMPLE_INFO(1	GND	RGP_ADC~	GND
24	GND	20MHZ_BACK_IN	GND	SAMPLE_INFO(3)	INTRLVE_INCR~	RGP_RX~	GND
25	GND	GND		SAMPLE_INFO(4)	GND	RGP_HPPR~	GND

AQS Service Tool (Unitool) 12

Introduction 12.1

For service purpose BRUKER has developed an universal service tool (named Unitool) that allows access to boards with Unitool support for diagnostic, check and firmware upgrade over the RS485 serial bus (SBSB, description can be found on ***page 15***).

The Unitool acts as a browser, all menus are provided by the units themselves. Board specific Unitool access can be achieved by starting the Unitool with the matching SBSB address (for addresses see ***"AQS address mapping" on page 238***)

With firmware release 'AD' and newer (see later how to determine), the following devices support Unitool within the AQS Chassis:

- AQS Controller (virtual, provided by one of the SGU)
- all SGU variants
- all AQS RX and RXAD variants
- all AQS internal amplifiers (reduced function)
- AQS FADC (reduced function)

FTLP4/M, HADC, SADC and Router can not be accessed by UniTool, but via the AQS Controller (formerly named ‚master) menu these boards are shown if available.

! ***The AQS Controller is a (virtual) device with its own SBSB address, although this function is provided physically on a SGU hardware. The AQS Controller is a separate task within the SGU firmware.***

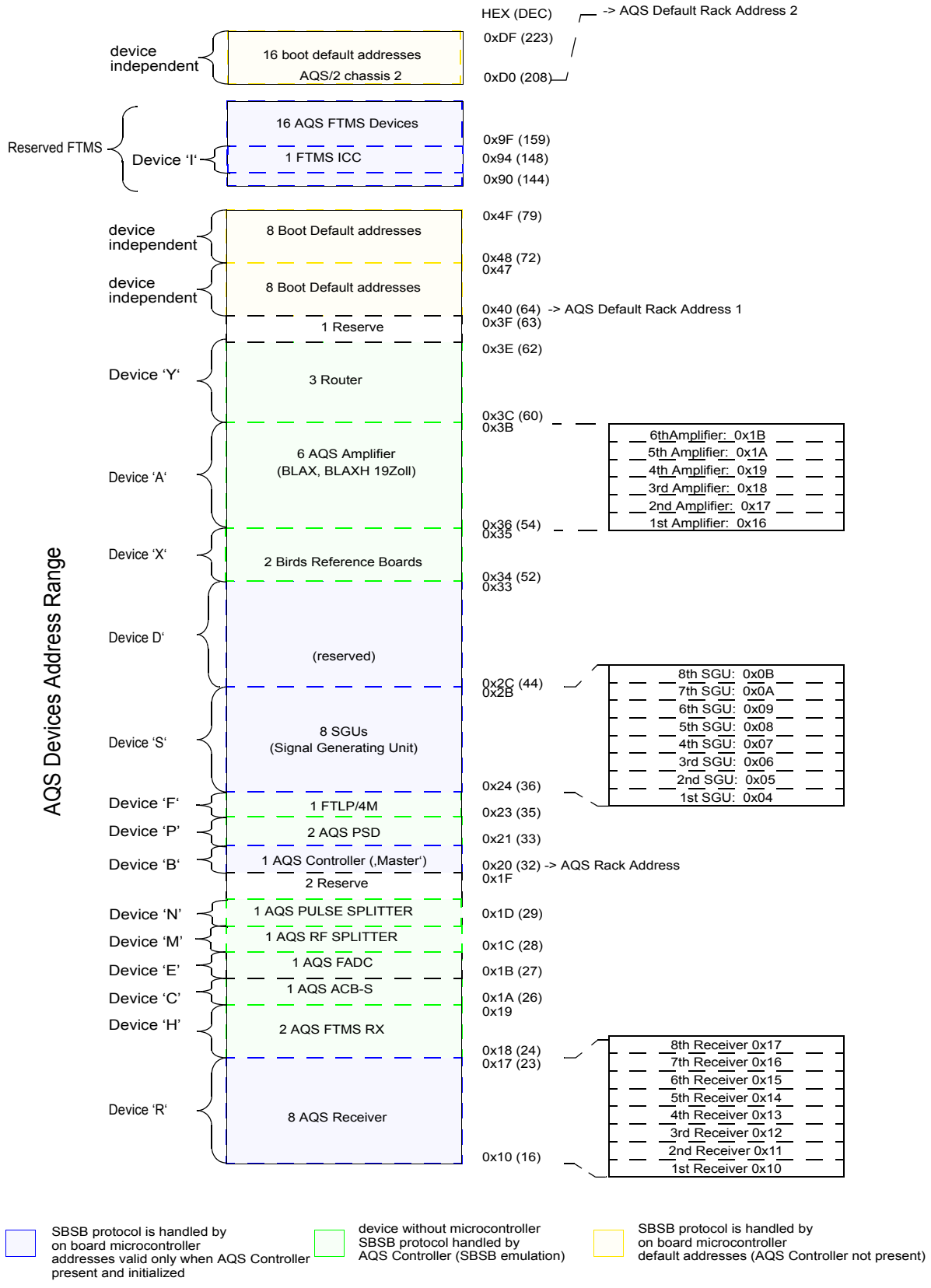
The AQS Controller function can be accessed on the AQS Controller address decimal 32 although the physical address of the SGU function is called on address 36.

! ***Older firmware releases do not support the AQS Controller Unitool function. Please follow the instructions to identify the actual firmware release first (see "Identification of the firmware release" on page 240)***

AQS address mapping *12.2*

Configuration and SBSB addresses can be found in
the ../conf/instr/<curinst> directory in the file uxnmr.info
or by ***"Identify your chassis configuration" on page 240*** using the Unitool.

Figure 12.1. SBSB addresses



Identification of the firmware release *12.3*

1. Open a shell or the command prompt in the BRUKER Utilities folder when using Windows.
2. Start the UniTool: `xwinnmr -e UniTool or topspin -e UniTool`
3. -> `aqs`, confirm
4. -> decimal address for e.g. SGU-1 is 36 or RX-1 is 16, confirm
5. Choose -> 1, confirm

You will be given the details of firmware and boot software version.

! Boards programmed in factory may show a different application firmware checksum compared to boards downloaded with UniTool

```
--------- Example how to start UniTool -----------
45% xwinnmr -e UniTool
Enter device name ['?' for details]  (aqs) >
Enter decimal SBSB address for board in AQS rack (36) > 36
device name taken from already existing configfile: /dev/tty10
B r u k e r  U n i T o o l
 Version: 1.0
 Compilation date: 000921
 W A R N I N G:
 This is a hardware level debug tool.
 Improper operation may damage your hardware.
 Connecting SBSB address 36 (0x24).
---------------- End Example -------------------------
```

Identify your chassis configuration *12.4*

! Older firmware releases do not support the AQS Controller Unitool function. Please follow the instructions to identify the actual firmware release first (see "Identification of the firmware release" on page 240)

1. Open a UNIX shell or the command prompt in the BRUKER

   Utilities folder when using Windows

2. Start the UniTool: xwinnmr -e UniTool
3. -> aqs, confirm
4. -> decimal address for the AQS Controller is 32, confirm
5. Choose -> [1], Rack Configuration, confirm

With the AQS Controller UniTool menu configuration information can be traced.

When finished a power up of the chassis is necessary because the AQS Controller has to re-scan the chassis.

Figure 12.2. Determine chassis configuration

```
------------------  Example ------------------------
45% xwinnmr -e UniTool
Enter device name ['?' for details]  (aqs) >
Enter decimal SBSB address for board in AQS rack (36) > 32
device name taken from already existing configfile: /dev/tty10

B r u k e r  U n i T o o l
   Version: 1.0
   Compilation date: 000921

W A R N I N G:
   This is a hardware level debug tool.
   Improper operation may damage your hardware.

Connecting SBSB address 32 (0x20).

>>>   Rackmaster  Menu   <<<
============================
[0] Init Rack
[1] Rack Configuration
[2] Rack Delete Error
[3] Rack Querry Request
[A] Service Functions
[X] eXit UniTool
    your choice:1
```

! ***The Re-Scan can be started using UniTool. Start UniTool on address 32 and select menu point [A] Service Functions and follow the instructions.***

Board type codes are shown in the following table:

Table 12.1. Birds Board Type Identifier Codes

board type	board type	board description	BRUKER number
0x00	0	SGU-C (frequency range 5..430MHz, print index C) SGU (regular frequency range 5..<643.45MHz, print index D)	Z003329 Z003642
0x01	1	board not inserted	
0x02	2	AQS Reference Board for AQS Receiver (REF400)	Z003265
0x03	3	AQS Reference Board with 22MHz IF output for RX22 (REF400-22)	Z003351
0x04	4	AQS Router Combiner	Z003624
0x05	5	AQS BLA2BB 150-60 dual amplifier 20-400MHz	W1345049
0x06	6	AQS BLAX300 single 300W X Amplifier	W1345052
0x07	7	AQS Controller	
0x08	8	AQS FTLP/4M filter board	Z002812
0x09	9	AQS ACB standard	H9488
0x0A	10	AQS PSD power supply distribution board	H9530
0x0B	11	AQS RECEIVER BOARD RXAD FTMS	Z102501
0x0C	12	AQS FTMS PSD power supply distribution board	A3142
0x0D	13	AQS FADC	H9685
0x10	16	SGU400 (frequency range 5..430MHz)	Z003642 ab ECL2.0
0x18	24	SGU600 (frequency range 5..<643.45MHz)	Z003831
0x28	40	SGU1000 (extended frequency range 5..1072.625MHz)	Z003330 ECL2.0 and newer
0x30	48	SGU-FTMS (ICR frequency range 5..10MHz, print index D	Z003643
0x42	66	AQS RXAD600 (standard frequency range 5..645MHz)	Z102117
0x52	82	AQS RXAD1000 (extended frequency range 5..1077.5MHz)	Z102118
0x60	96	AQS RX-E (extended frequency range 5..1077.5MHz)	Z003689
0x61	97	AQS RX-BB (extended frequency range 5..1077.5MHz)	Z003689
0x62	98	AQS RXAD-BB (extended frequency range 5..1077.5MHz)	Z102119
0x72	114	AQS RXAD400 (base frequency range 5..430MHz, ...)	Z102116
0xC0	192	AQS Reference Board for AQS Receiver RX600 (REF600)	Z003936
0xC1	193	AQS Reference Board for AQS Receiver RX1000 (REF1000)	Z003937
0xC2	194	AQS Reference Board with 22MHz IF output for RX22 (REF600-22)	Z003938

Table 12.1. Birds Board Type Identifier Codes

board type	board type	board description	BRUKER number
0xC3	195	AQS Reference Board with 22MHz IF output for RX22 (REF1000-22)	Z003939
0xC4	196	AQS BLA2BB 150-60 dual amplifier 20-500MHz	W1345072
0xC5	197	AQS 1to4 Router	Z101247
0xC6	198	AQS/2 Chassis	Z101618
0xC7	199	AQS 2H-TX BD 200-400	Z103550
0xC8	200	AQS 2H-TX BD 500-1000	Z103551
0xC9	201	REF/2 1000	Z104236
0xCA	202	AQS RF SPLITTER BOARD	Z104432
0xCB	203	AQS PULSE SPLITTER BOARD	Z104431
0xCC	204	AQS/2-M Chassis	Z104493

Download new SGU firmware *12.5*

Please refer to the BRUKER Service Information to check out if a download is necessary.

! ***The download of the newest firmware is not always necessary or makes sense, please read instructions carefully***

! ***If you download new firmware ensure that the AQS Controller SGU has always the newest firmware. For proper operation all SGU with same ECL must have identical firmware versions.***

Important: Download the correct firmware on the corresponding SGU engineering change level (see ***Table 12.2.***), e.g. firmware birdbg.hex is ***not compatible*** to older ECL of AQS SGU and is labeled by an increment in the major release character (bird***b***g.hex instead of bird***a***l.hex).

As mentioned above, SGUs with different ECLs can be mixed in an AQS. Be sure that in this case all SGUs have load down the **newest** corresponding firmware version:

- Download latest firmware from ftp://ftp.bruker.ch/pub/NMR/download/servtools/firmware/aqs/ and copy it to the UniTool directory on your workstation (see details in ***"Download new SGU firmware" on page 244***).
- Read the release notes carefully
- Start an *Auto Download* using UniTool. The download routine checks if a download is necessary.

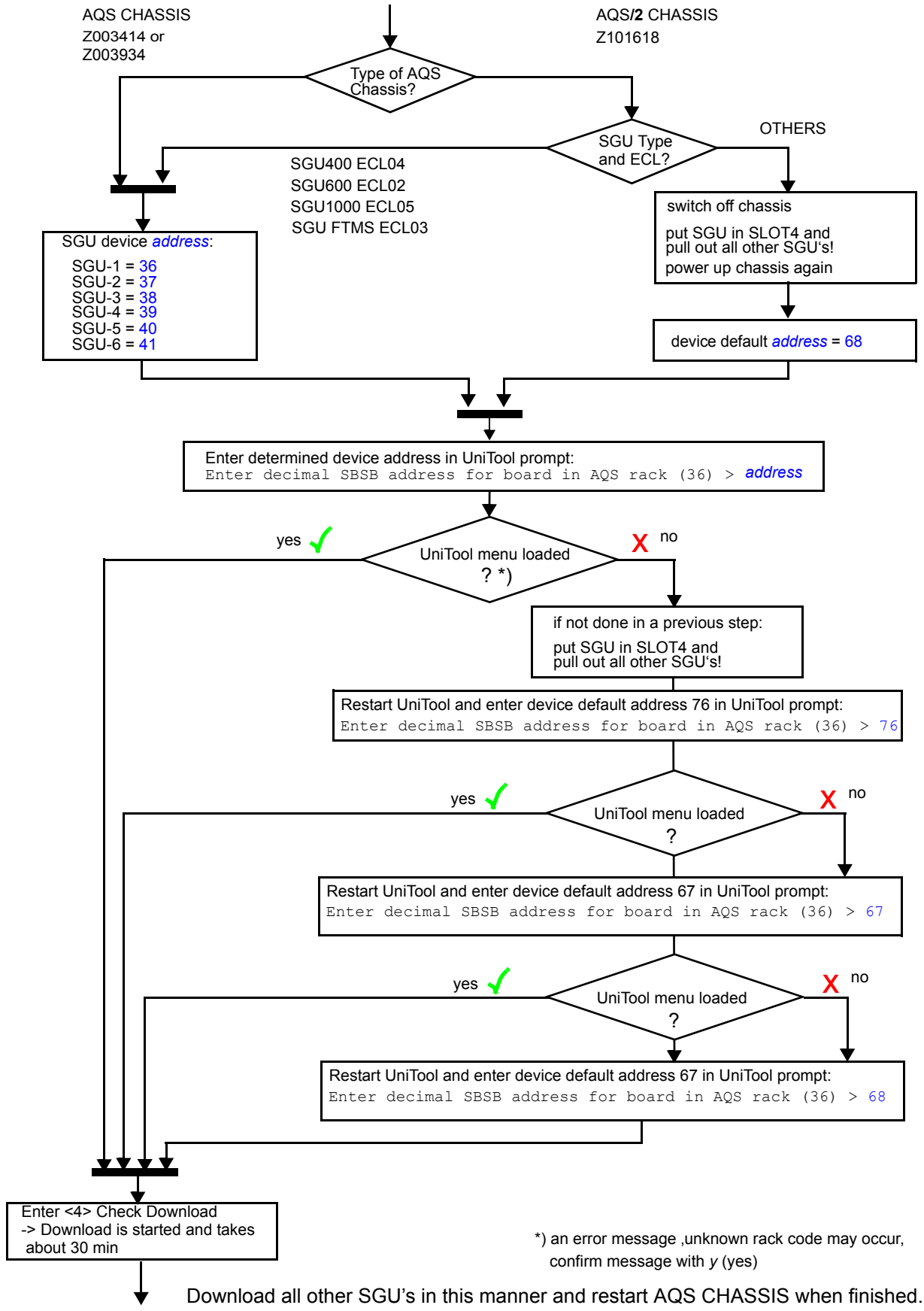
Further information about the demand of new firmware can also be found on the FTP server of BRUKER AG (B-CH):

ftp://ftp.bruker.ch/pub/NMR/download/servtools/firmware/aqs/

Follow these instructions:

1. Check if the directory (/Bruker/<`xwinnmr/topspin release`>/conf/instr/servtool/UniTool/files/birds) exists. Otherwise create it.
2. Copy the firmware birdbg.hex into the directory /Bruker/<`xwinnmr/topspin release`>/conf/instr/servtool/UniTool/files/birds
3. Open a shell or the command prompt in the BRUKER Utilities folder when using Windows.
4. Start the UniTool: `xwinnmr -e UniTool or topspin -e UniTool`
5. -> `aqs`, confirm
6. Determine decimal address for SGU to be load down (36 for SGU-1, 37 for SGU-2 etc. or check the flow chart in ***Figure 12.3.***)

Figure 12.3. SGU download



*) an error message ,unknown rack code may occur, confirm message with *y* (yes)

Download all other SGU's in this manner and restart AQS CHASSIS when finished.

Error handling 12.6

Network failures / connection lost 12.6.1

The download can be restarted on the same address as before.

System power down 12.6.2

If a *power dow*n occurred while loading new firmware the restart of the download is different. The red LED of the SGU in boot mode is blinking *fast*.

Check if the AQS Controller has found all SGU's at power up (see slot list/configuration ***"Identify your chassis configuration"***). If the SGU in boot mode has not been found (corresponding line in the slot list is empty) a default SBSB address in accordance with the procedure described in ***Figure 12.3.*** has to be entered when starting UniTool.

The download can be restarted. When finished, a power up of the chassis is necessary because the AQS Controller has to re-scan the AQS chassis.

Problems starting UniTool? 12.6.3

UniTool is running on the SBSB libraries from XWINNMR or TOPSPIN, so a complete installation, valid paths and environment are necessary. Essentials for serial RS-485 / SBSB communication:

1. The directory <XWINNMRHOME>/conf/instr/spect/rs232_device/ must exist
2. In this directory the corresponding files must be created and edited: aqs and preamp1, e.g.

```
# XWIN-NMR TTY configuration file
# created automatically by 'cf'
# do not edit, changes are lost after next 'cf'
unit = AQS-Rack
host = spect
device = /dev/tty10
stty = 9600 min 1 time 50 cs8 hupcl cread clocal
```

3. The file <XWINNMRHOME>/conf/instr/curinst must contain the name 'spect' (otherwise edit). curinst is the link between `<XWINNMRHOME> and /conf/instr/...`
4. Before starting UniTool set the shell variable XWINNMRHOME

```
Linux(bash): export XWINNMRHOME=/opt/xwinnmr or

Linux(bash): export XWINNMRHOME=/opt/TOPSPIN

Windows(cmd): set XWINNMRHOME=C:/Bruker/xwinnmr or

Windows(cmd): set XWINNMRHOME=C:/Bruker/TOPSPIN
```

ECL and required Firmware Versions for AQS/2 *12.7*

The following table gives an overview of a necessary download for **AQS/2** CHASSIS support:

Table 12.2. Overview firmware version and SGU ECL

SGU Type	Part Number	ECL	Required firmware release
SGU400	Z003642	00, 01, 02	birdal.hex
		03, 04, 05, 06	birdbg.hex
SGU600	Z003831	00	birdal.hex
		01,02,03, 04	birdbg.hex
SGU1000	Z003330	00,01,02,03	birdal.hex
		04,05,06,07	birdbg.hex
SGU FTMS	Z003643	00, 01	birdal.hex
		02,03,04,05	birdbg.hex

Download new AQS Receiver (RX) Firmware *12.8*

1. Check if the directory (/Bruker/<`xwinnmr/topspin release`>/conf/instr/servtool/UniTool/files/birds) exists. Otherwise create it.
2. Copy the new firmware e.g. **rxs**_ap.hex into the directory Bruker/<`xwinnmr/topspin release`>/conf/instr/servtool/UniTool/files/birds
3. Open a shell or the command prompt in the BRUKER Utilities folder when using Windows.
4. Start the UniTool: `xwinnmr -e UniTool or topspin -e UniTool`
5. -> `aqs`, confirm
6. -> decimal address for RX-1 is **`16`**, confirm
7. When the UniTool Menu is loaded, enter `<4> Auto Download` -> download is started. The download takes about 22 minutes
8. If you have more than one RX, do the same as above with address **`17, 18,`** and so on.

New configuration of the AQS amplifiers *12.9*

! ***Remember that the Unitool is a hardware level debug tool. Improper operation may damage your hardware. Please read the following lines carefully.***

According to the document “BIS Groups and Values” (Andreas Hünnebeck (AH), version 2.6 and higher), the amplifiers provide a housing information in its BIS that allows the software to determine an SBSB address.

Later versions of the amplifiers have this entry in their BIS. If an error message like

"no amplifier housing information in BIS, using default address " or

"multiple amplifier housing information in BIS, using default address "

is printed out you should read the following lines.

For future 3 channel configurations with internal AQS amplifiers, housing information must be programmed in the BIS

Default values *12.9.1*

Default values in the amplifier BIS should be:

BLA2BB: Housing, Hsg = 1 (amplifier 1)

BLAX300: Housing, Hsg = 2 (amplifier 2)

In a 2 channel AV with one BLA2BB without a housing entry, no error or warning messages is given (backward compatibility to most used configurations). BLA2BB is amplifier 1.

For a 3 channel AV with BLA2BB and BLAX300, where both amplifier do not have a housing entry, warning messages are given and default values are set. These values can be modified using the UniTool with the BLA SBSB address.

Default SBSB addresses, ***when no housing*** is originally programmed

1. 1 BLA2BB in Slot 8: 0x36
2. BLA2BB (Slot 8), BLAX300 (Slot 6, on the left side of BLA2BB):

   BLA2BB: 0x36 (decimal 54)

   BLAX300: 0x37 (decimal(55)

Check the addresses before changing any entry. This can be done by starting the UniTool at the AQS Controller address:

1. Start the UniTool in a Shell: `xwinnmr -e UniTool`
2. -> `aqs`, confirm
3. -> decimal address of the AQS Controller is **32**, confirm
4. Select 1, Configuration-> a list is shown (see ***"Identify your chassis configuration" on page 240***) with the SBSB addresses of the devices.

Adding Housing Setting *12.9.2*

Follow these instructions to add the housing information to amplifiers with old BIS.

Conditions:

- BLA2BB in Slot 8
- BLAX300 in Slot 6

1. Power up the AQS Chassis
2. Start the UniTool in a Shell: `xwinnmr -e UniTool or topspin -e UniTool`
3. -> `aqs`, confirm
4. -> SBSB address of the amplifier BLA2BB is hex 0x36 resp. decimal **54**, confirm,
5. Change at menu Point 2 the housing information (1 for BLA2BB recommended). The setting is saved automatically. Exit UniTool.
6. Start the UniTool in a Shell: `xwinnmr -e UniTool or topspin -e UniTool`
7. -> `aqs`, confirm
8. -> SBSB address of the amplifier BLAX300 is hex 0x37 resp. decimal **55**, confirm,
9. Change at menu Point 2 the housing information (2 for BLAX300 recommended). The setting is saved automatically. Exit UniTool.
10. Perform an AQS power down
11. Power up the AQS chassis and initialize the spectrometer with “cf”
12. Check SBSB addresses with UniTool on AQS Controller address 32:
13. BLAX300 in Slot 6 with housing 2: 0x37, amplifier is AMP2
14. BLA2BB: in Slot 8 with housing 1: 0x36, amplifier is AMP1

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