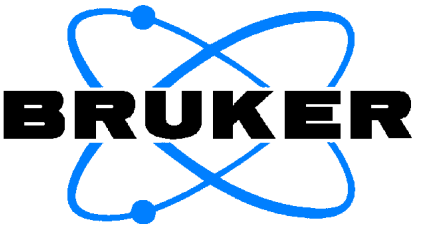


AQR / AQS

HADC/2 Technical Manual

Version 002

BRUKER

Verteiler:

Änderungshistorie:

Index:	Datum:	Text:	Visum:
002	04.04.2000	Neu erstellt	RO

This manual was written by

Pietro Lendi / Michael Schenkel

Fällanden, Switzerland
P/N: Z31414
DWG-Nr: 1126002

Contents

Contents

Index

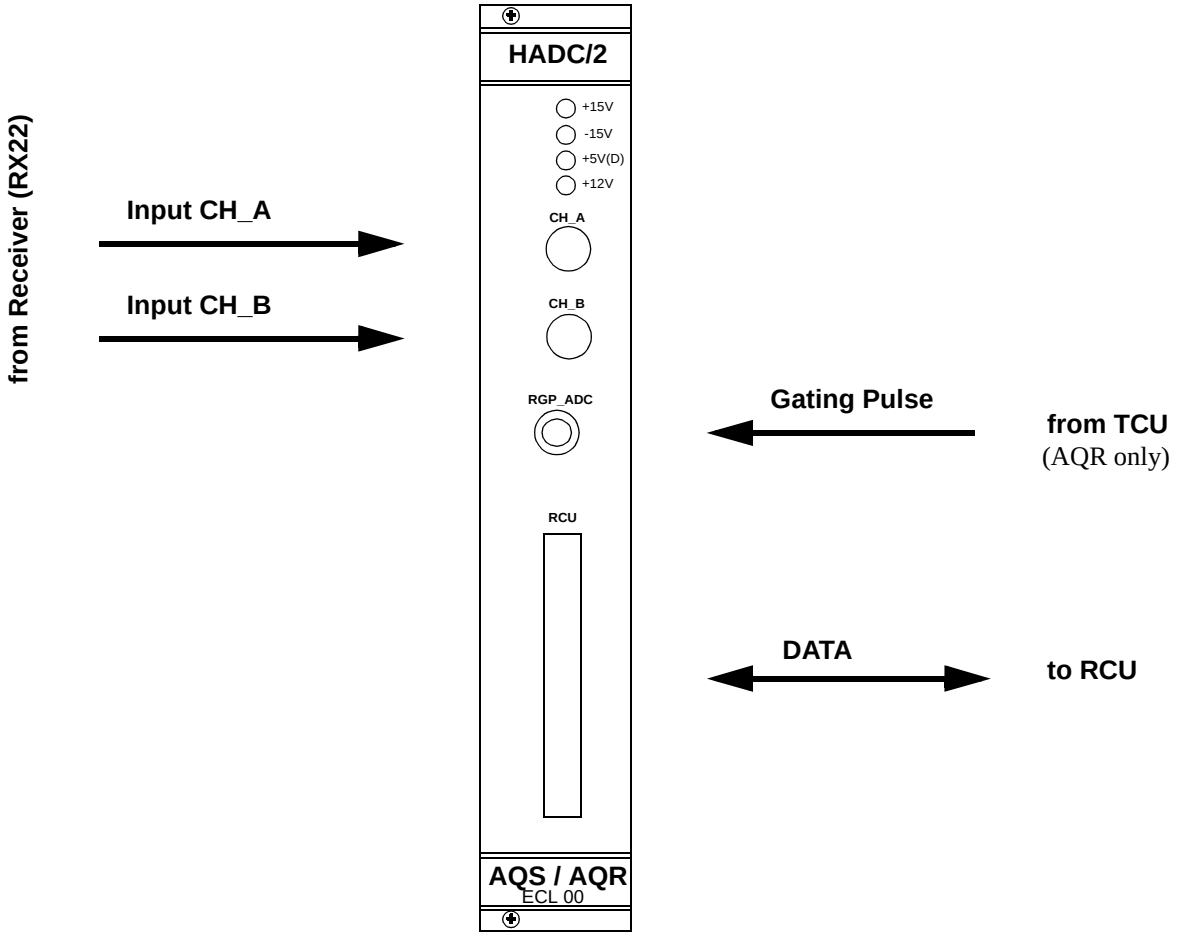
Index

General Description 1

General 1.1

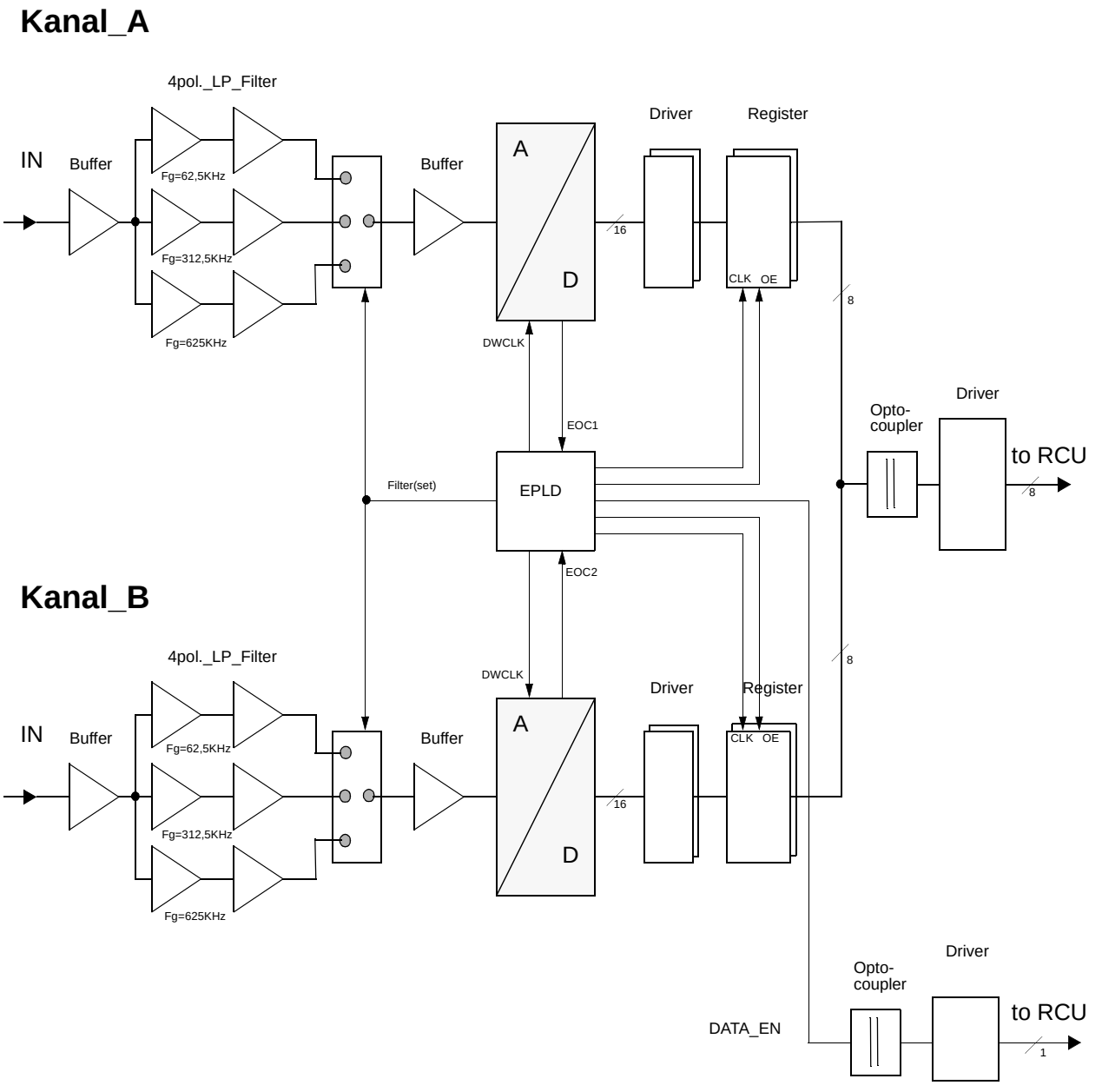
The HADC/2 unit called **H**igh **r**esolution is a **16 Bit system** for a spectral width of 1MHz. Because of the quadrature detection method in NMR, this system is composed of 2 channels. Each channel has its own anti-aliasing filterbank. **The Throughput rate for each channel is 1MS/s.** Because of the oversampling techniques, a reduced set of anti-aliasing filters are required. The HADC/2 is very similar to the BRUKER AQR HADC.

Figure 1.1. System Configuration



Functional block diagram *1.2*

Figure 1.2. Dataflow



Connection to RCU (Receiver Control Unit) 1.3

The differential line tranceivers on the HADC/2 - board and the differential line receivers on the RCU guarantee a reliable data transfer between the HADC/2 and the RCU. To prevent any noise pickup through the cabling, all transmission lines are galvanically isolated.

I2C Bus 1.4

For control purpose an I2C bus is implemented. Via this bus the HADC/2 can be reset, the antialiasing filter can be selected and the acquisition mode can be set. Normaly this configuration will be done by the RCU, which is controlled by the acquisition software XWINNMR.

Filter settings

There are 3 analog filters with different corner frequency for each channel. It is always the same corner frequency that is set at Channel_A and Channel_B.

Realtime Control 1.5

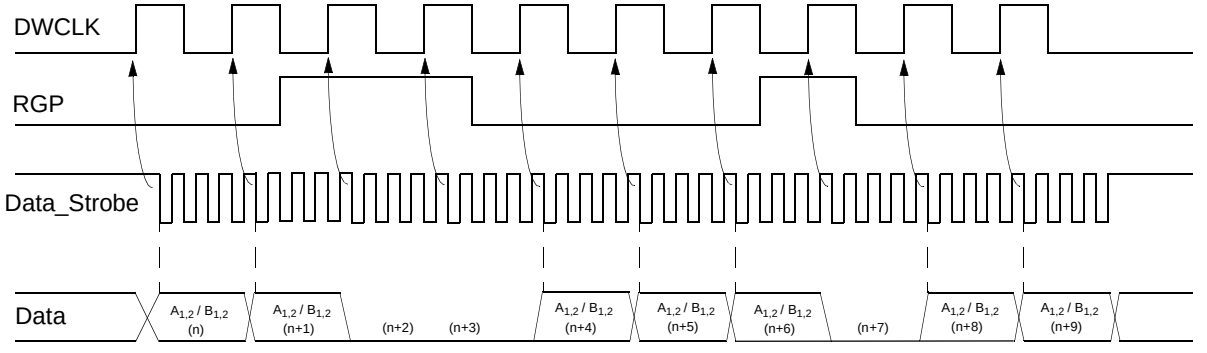
*DWCLK (D*well_*C*lock*)*

The DWCLK is the convert pulse of the ADC it will be generated by the observing SGU for AQS type or by the RCU for AQR type.

*RGP (R*eceiver *G*atting *P*ulse*)*

This signal will be generated by the SGU for AQS type or by the TCU for AQR type. When this signal is active (high) no data will be sent from the HADC/2 to the RCU. During the active period of the RGP pulse the value of the data which will be transmitted is ‚0'. See ***Figure 1.3.***

Figure 1.3. RGP pulse timing



Power Supply 1.6

The HADC/2 is located in the AQR - or AQS Rack with access at the front to the Channel_A & Channel_B inputs, the RGP input, the connector to the RCU as well as the power LEDs. At the rear there is only one connector fitting the AQR -, AQR/P or AQS-Rack. The power is primarily drawn from the rack side. The different HADC/2-Versions consume different supply currents. See ***Table 1.1.***

Table 1.1. DC specification typical value

Parameter Conditions	ADC4320	ADS937	ADS931
Supply current (+19V)	460mA	405mA	600mA
Supply current (-19V)	240mA	260mA	370mA
Supply current (+9V)	180mA	190mA	190mA
Supply current (+12V)	480mA	480mA	480mA

Piggy Back 1.7

The A/D-Converters are on an additional board which is connected to J2,J3,J4,J5 on the BasicBoard. See ***Figure 1.9.*** There is also an additional cable from the PiggyBack to the BasicBoard which is the RGP cable. This cable has to be soldered to the locations listed in ***Table 1.2.***

Table 1.2. RGP cable

PiggyBack Board No.:	J6 / [1)]Pin1	J6 / Pin5
Z4P3097...	VPWRGND_solder spring	IC49 / Pin2 (R182)
Z4P3101...	VPWRGND_solder spring	IC49 / Pin2 (R182)
Z4P3102...	DGND_solder spring	IC49 / Pin6 (R189)

1) Note: Pin1 of the connector J6 on the PiggyBack is the Pin with the square pad of the J6 shape.

Figure 1.4. Connector HADC/2 - RCU

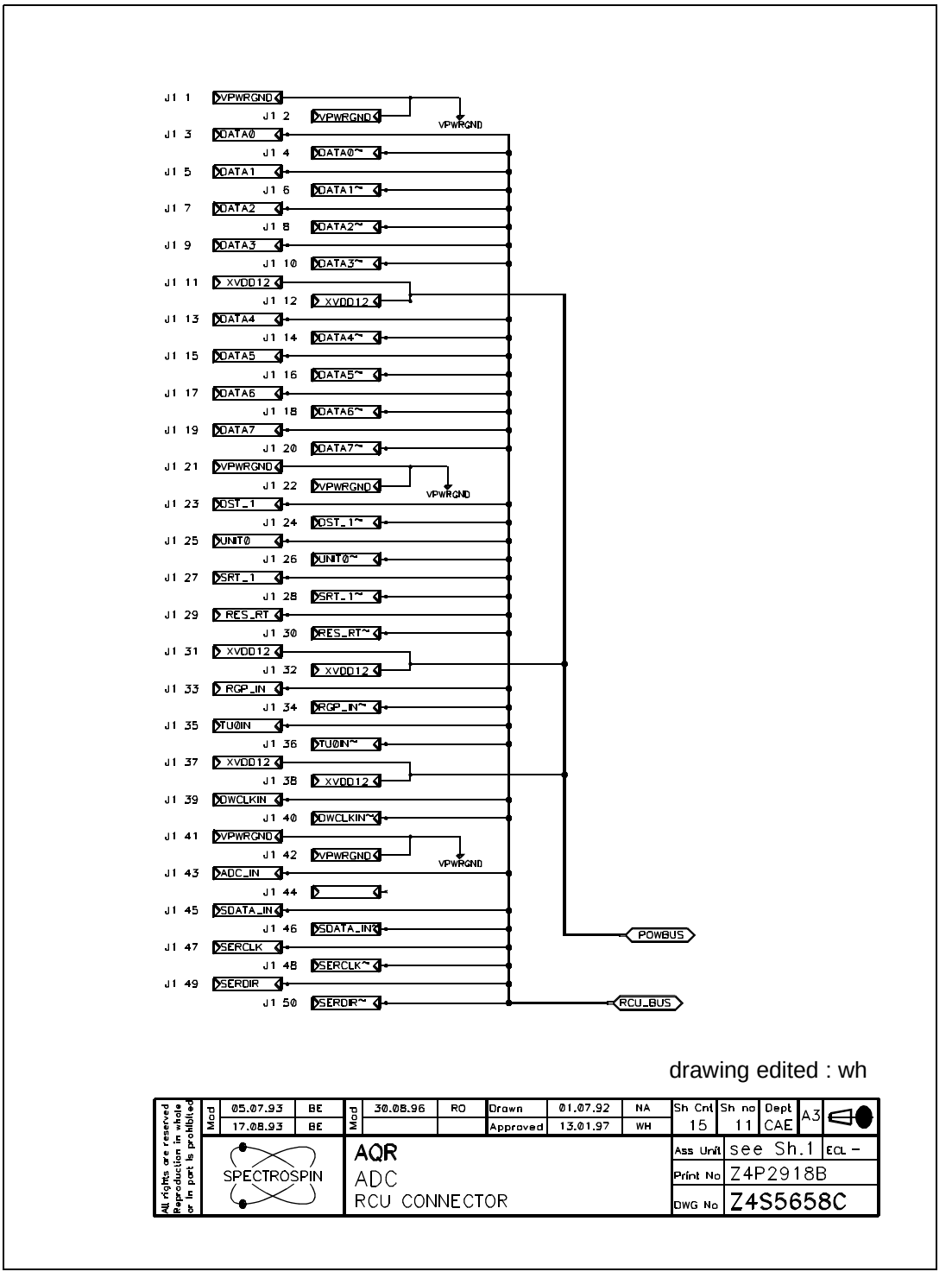


Figure 1.5. Connector HADC/2 - AQR Rack

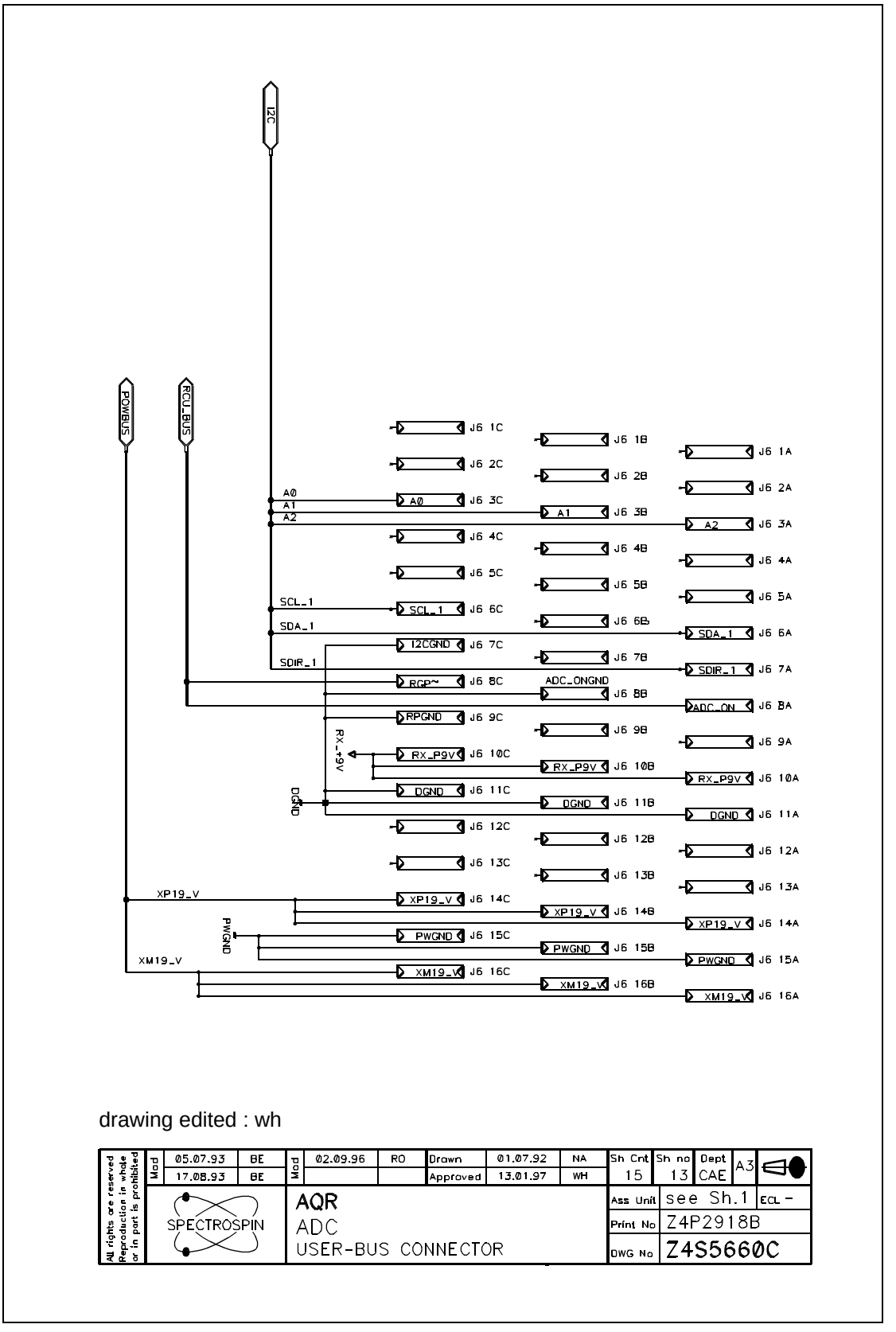


Figure 1.6. Connector HADC/2 - AQS - Rack

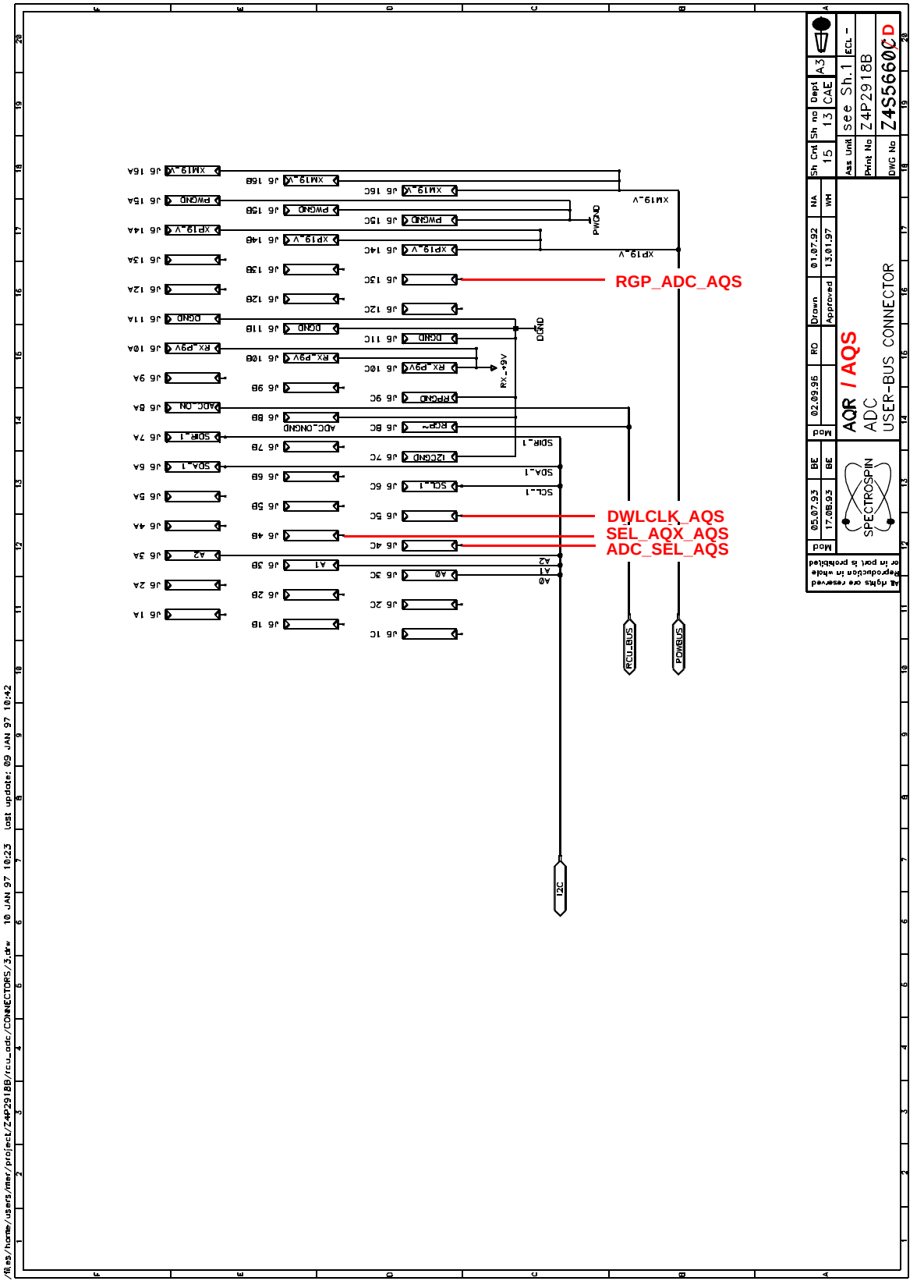
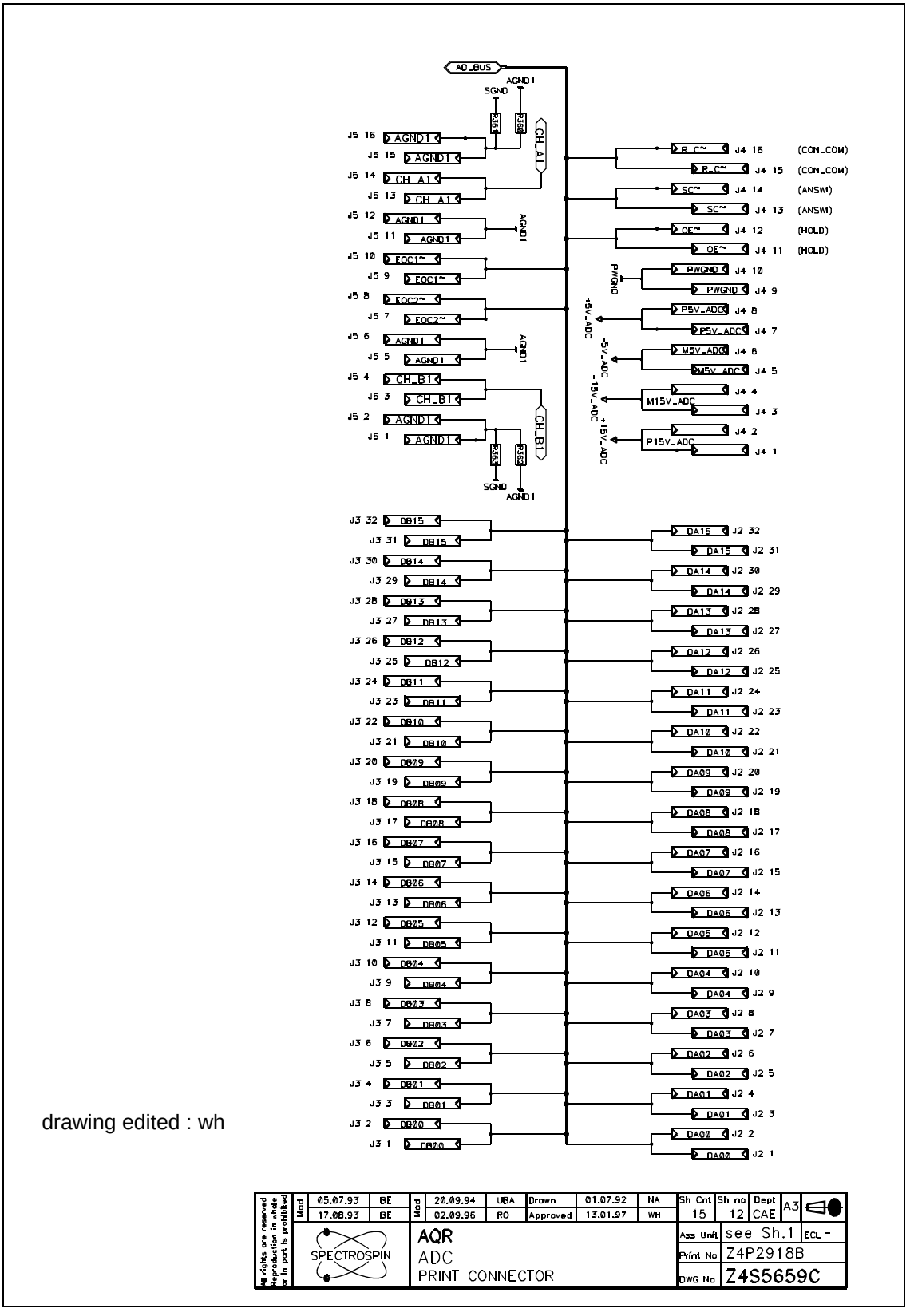


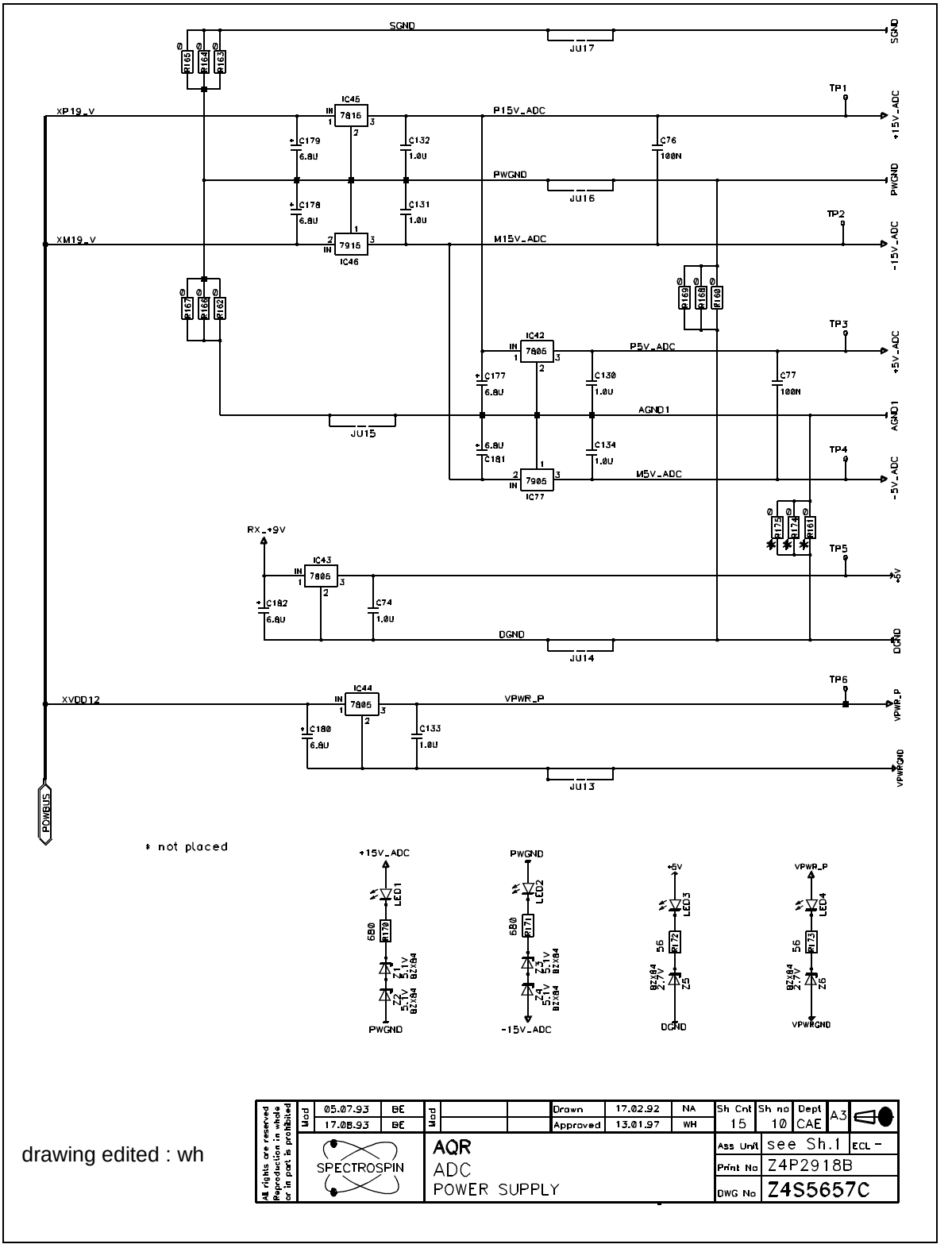
Figure 1.7. Connector BasicBoard - PiggyBack



drawing edited : wh

Power Supply *1.9*

Figure 1.8. Power Supply of the HADC/2 BasicBoard



Assembly map HADC/2 *1.10*

Figure 1.9. Assembly map AQR HADC/2 basic board

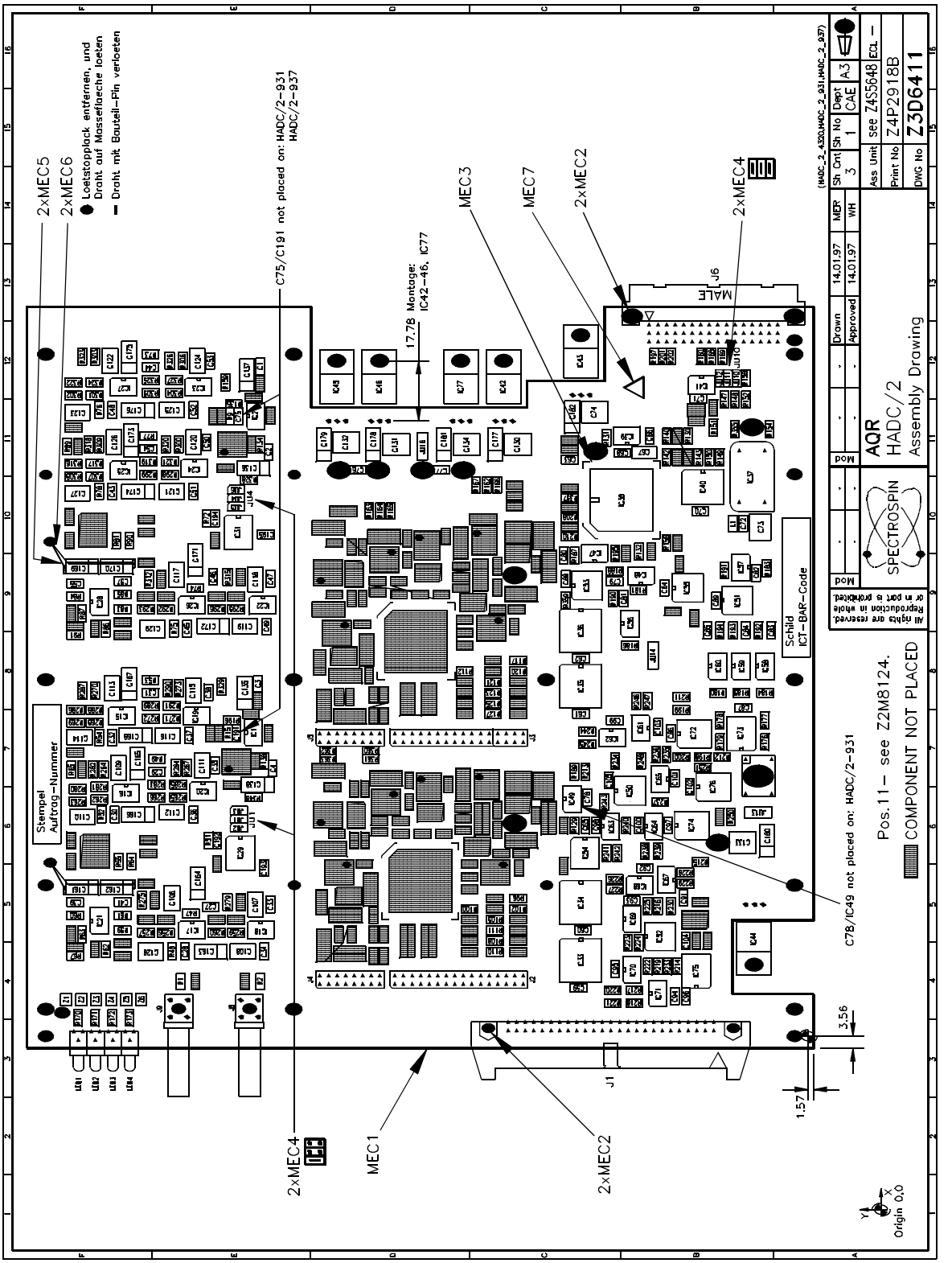
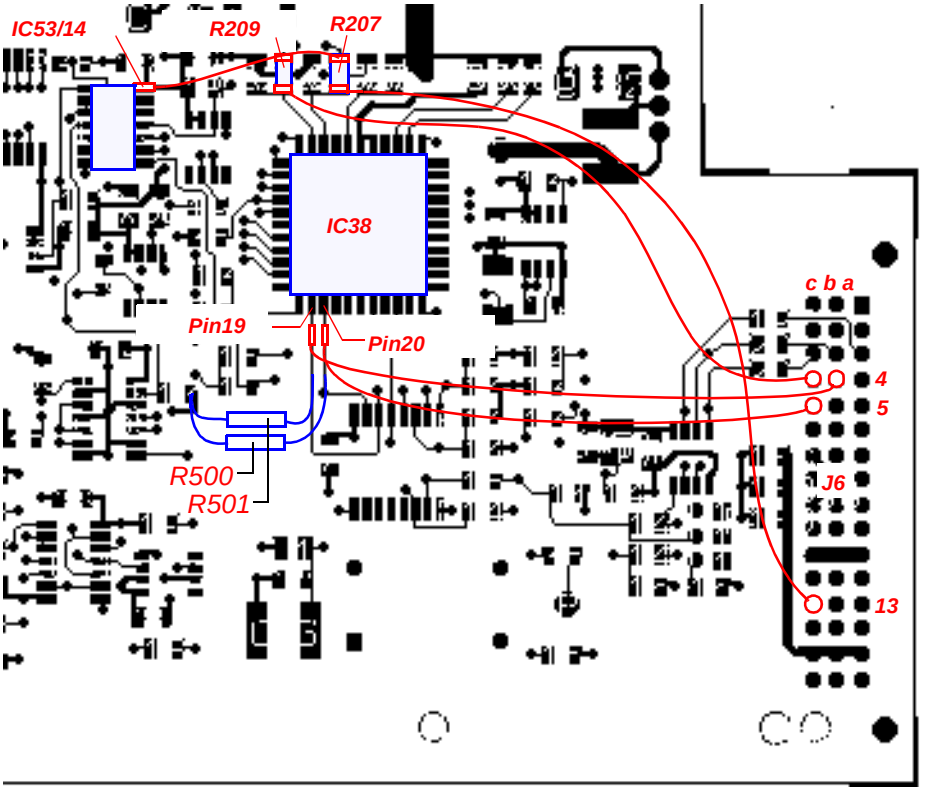


Figure 1.10. Modifikation for AQS HADC/2 basic board



Figures

Figures

Tables

Tables