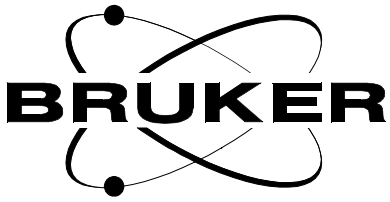

GREAT 1/10

Technical manual
GREAT 1

Version 003

BRUKER

The information in this manual may be altered without notice.

This manual was written by

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Wissembourg, France

Manual P/N: Z31351
DWG-Nr: 1060003

Contents

Contents

Index

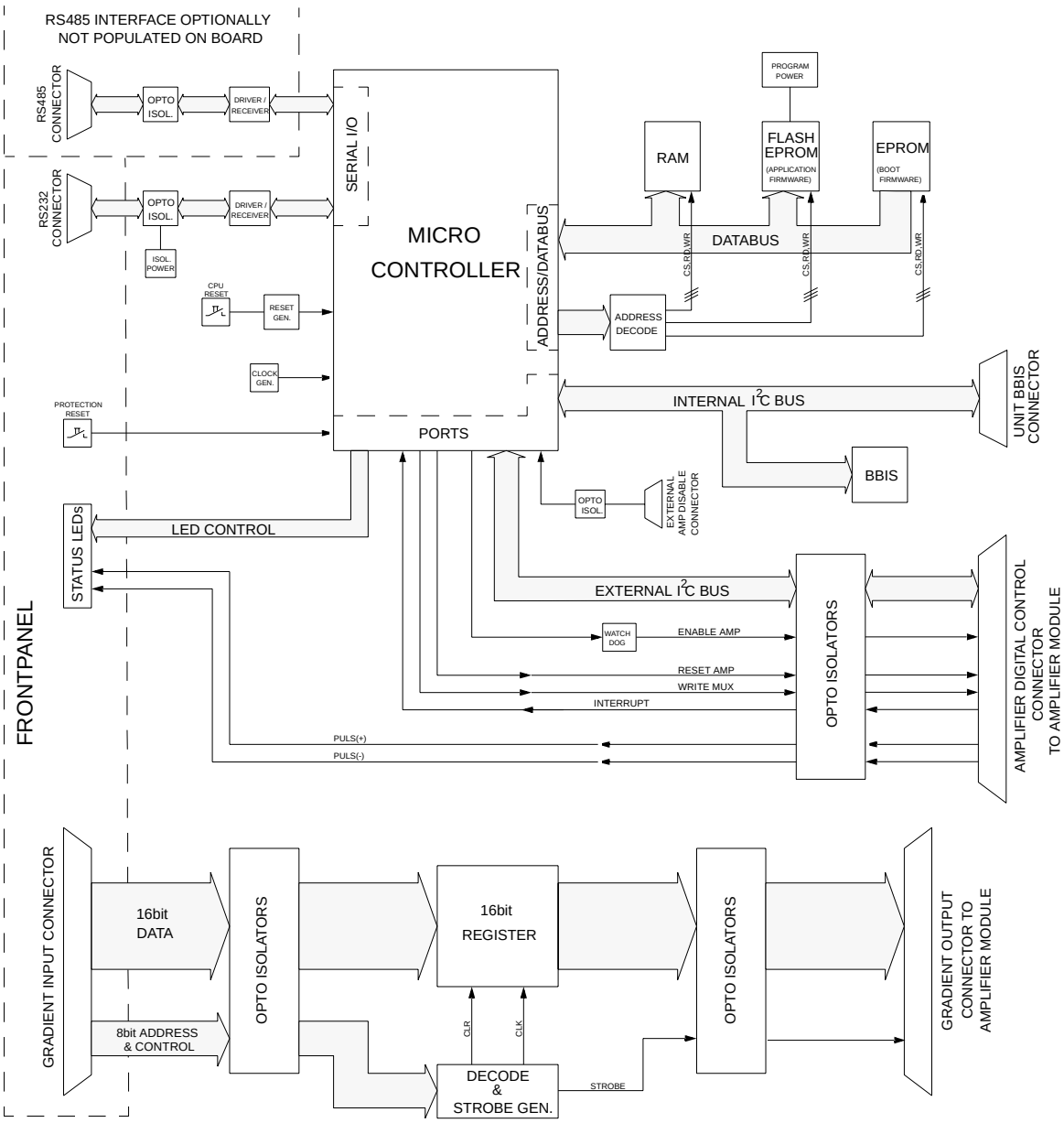
Index

General

1

GREAT Interface Board Description 1.1

Figure 1.1. GREAT Interface Board Block Diagram



The GREAT Interface Board consists of two main sections, the Microcontroller section for digital control of the amplifier functions and the Gradient Input section to interface the 10A gradient amplifier module with the Gradient Control Unit (GCU).

Microcontroller section *1.1.1*

The microcontroller (Siemens 80C535) communicates with the Communication Control Unit (CCU) via serial I/O. A galvanically isolated RS232 connection is used. RS485 is a possible option but is not populated.

Memory consists of a 32kByte RAM, a 32kByte EPROM for boot firmware and a 32kByte FLASH EPROM for application firmware. Application firmware is downloadable via serial I/O. This is controlled by the boot firmware in the EPROM. Address decoding is done by the PAL18P8 labelled „GRT0AA01-KE“.

An internal I^2C bus communicates with the BBIS („Bruker Board Information System“) of the GREAT Interface Board and via a flat cable connector with the BBIS of the complete GREAT unit, both storing their data in serial EEPROMs.

The gradient amplifier module is controlled via the external I^2C bus. It connects to the BBIS and to various 8bit port chips on the amplifier. The port chips are used to load PreEmphasis, Offset- and Loop-parameters, the High/Low impedance state and to read the error status of the amplifier. Additional lines are used for a „WRITE MUX“ signal which is a clock for several parameter registers of the amplifier, the reset signal for the amplifier, an interrupt signal which causes an interrupt on the micro controller if an error occurs and the enable signal for the amplifier. This enable signal is monitored by a retriggerable monostable as a watchdog. The watchdog disables the amplifier in case of an error in the application firmware about 1 second after the enable signal stops toggling. All signal lines to the amplifier module are galvanically isolated.

On the frontpanel is the RS232 connector, a button for protection reset and various status LEDs. The following status signals are displayed: PreEmphasis on, amplifier enabled, low impedance, high impedance load, amplifier ready and error. Two additional LEDs display the positive and negative output pulses of the amplifier.

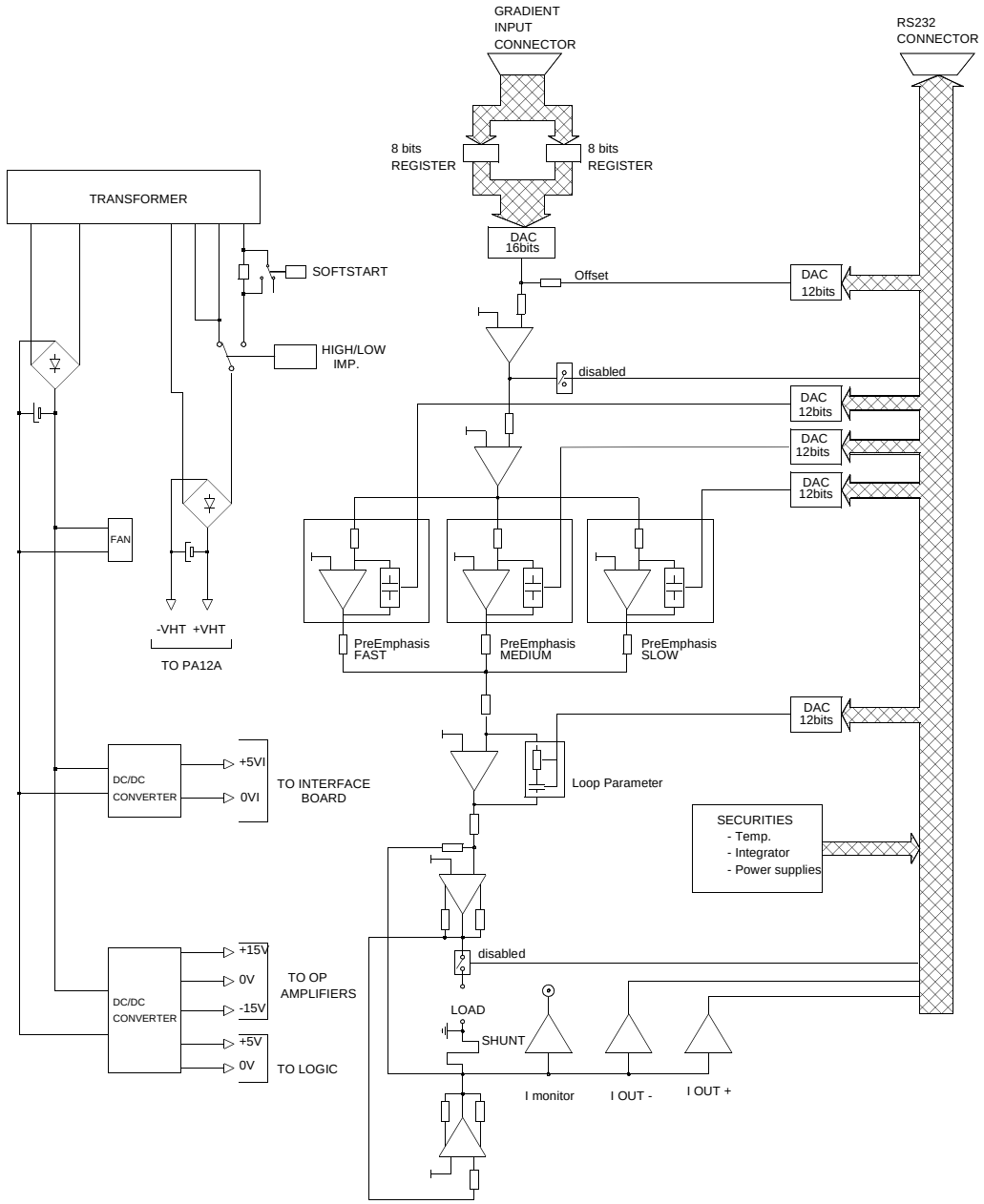
Gradient Input section *1.1.2*

The gradient input signals (16bit data, 4bit address and 4bit control signals) are delivered via a 50pin SCSI connector. The data is stored in a 16bit register. The PAL18P8, labelled „GRT0AA02-KE“ and monostables work as decoder and strobe generator.

The interface is galvanically isolated by opto isolators in both directions: i.e. to the GCU as well as to the amplifier module.

Amplifier Module Description *1.2*

Figure 1.2. Amplifier Module Block Diagram



The power module is fitted with 2 parts :

- the power supply part (section)

- the power amplifier part (section)

The module controls are delivered by I2C bus via RS232 connector;those of the rapid bus for DAC702 are delivered via connector SCSII 50 pins GRAD IN.

The amplifier module part is composed of different sub-assemblies :

- the power amplifier,

- the DAC 16 bits digital control,

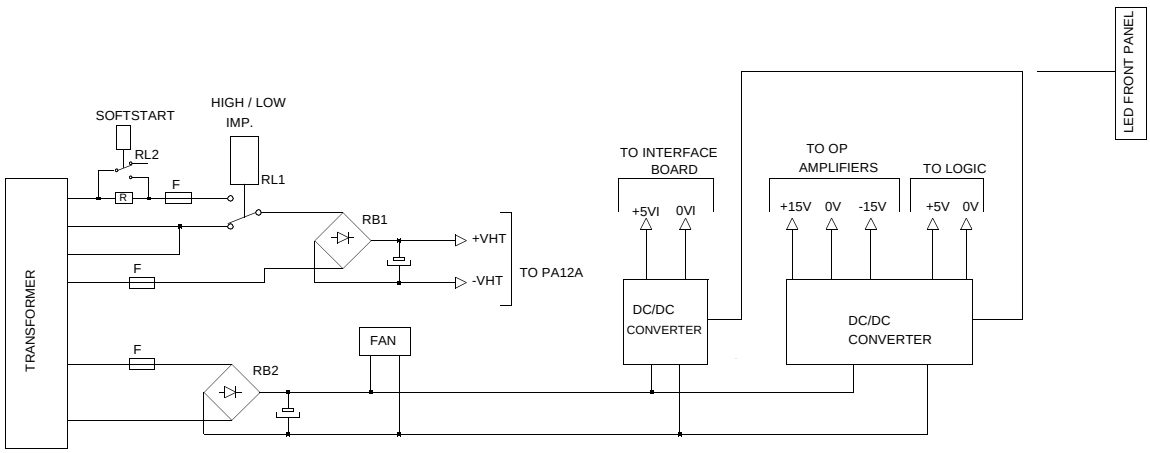
- the preEmphasis,

- the securities,

All these sections as well as the power supply section above will be described with more on following pages.

Power Supply section *1.3*

Figure 1.3. Power Supply block diagram



The GREAT power supply section is provided via the power block which is foreseen to feed all the boards inside the unit, for example the interface and the amplifier board.

The supply is composed of 2 power rectifiers foreseen to supply on one hand the DC/DC converters and the fan, and on the other hand the 2 operating power amplifiers.

The HIGH/LOW commutation is done via a power relay which allows the commutation of the 2 serial windings.

The resistor, placed in serial with the second winding, is useful as softstart so that the voltage on the caoacitors terminals will not raise too fast.

The HIGH/LOW control is delivered by I2C bus via the amplifier board (pinA11).

The fuses for the security are resetable thermic fuses type Polyswitch.

The kind of these fuses cuts off when overheating and stays in position 'OPEN' as long as there is a voltage presence.To reset the unit, cut off the main with button 'POWER ON' and wait until the fuse has a normal temperature and that the defect is deleted;

On the front panel you have a display which shows you the different power voltages used on the unit.

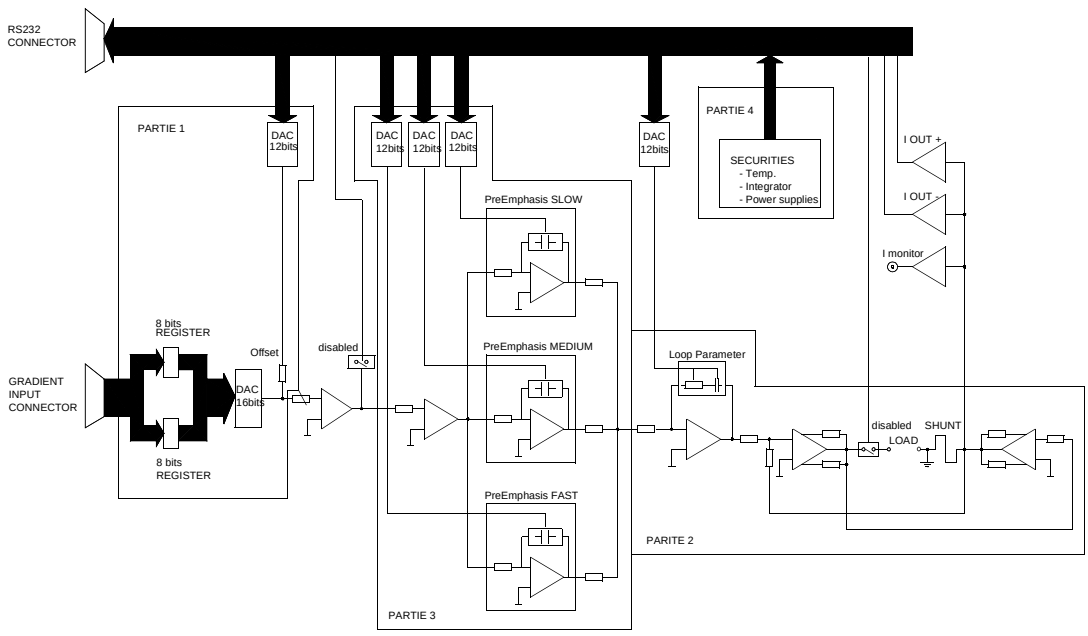
For the display of the voltages VHIGH and VLOW, don't forget that each of the 2 voltages is displayed individually so the 2 leds are always ON.

During special tests (silent test on spectrometers) it is possible that no LED(VHIGH and VLOW) lighs on for a moment.

The reason is the big voltage variation on the power rectifier which is due to a strong load during the pulse.This defect is ignored by the control if it does not persist over 50ms.

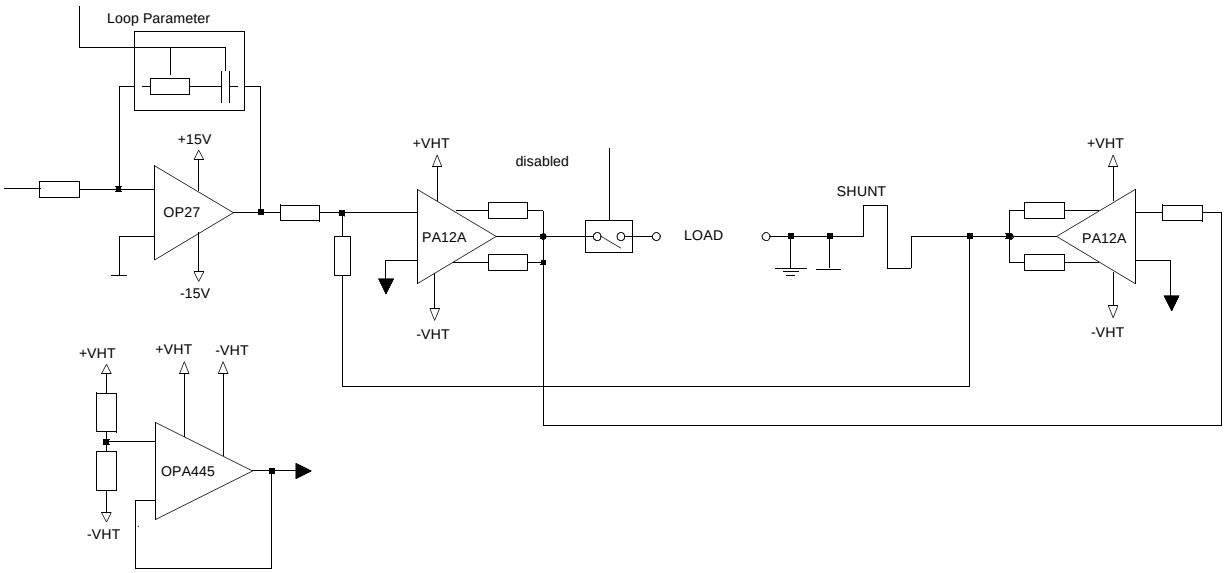
Power amplifier module section *1.4*

Figure 1.4. Amplifier module block diagram



Power stage and regulation amplifier section *1.4.1*

Figure 1.5. Power stage and regulation block diagram



The power module assembly is based on a current regulation controlled via DAC which gives the pulsed reference.

The regulation section is provided via an operating amplifier type OP27 which compares this reference to a voltage, issued from the internal shunt of 0.33Ohm/ 5ppm, allowing to have a signal increase and an optimal stability.

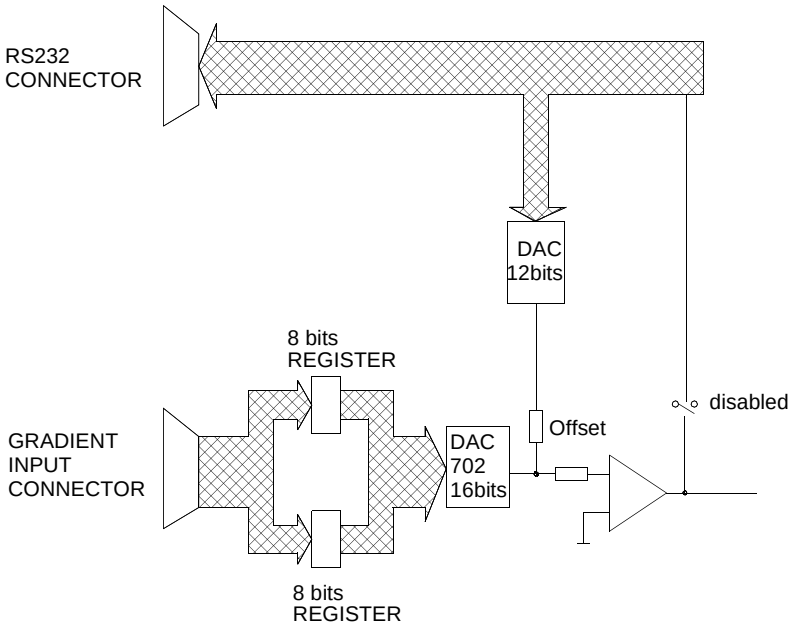
The regulation loop optimalization is done via analog switches commutating 8 resistors and 8 capacitors allowing a fine and gradual adjustement.

The output amplifier stage is fitted with 2 operating power amplifiers type PA12A mounted in H.This system is fully floatend and allows a regulation according to a point 0 (false) reference via an operating high voltage amplifier type OPA 445.

The power interruption is done via 2 MOS transistors. During this operation, the reference is set to zero in order to minimize the output field of the power stage, this one is no more looped on the reference.

Gradient input and commands section *1.4.2*

Figure 1.6. Gradient input and commands



The DAC and commands section is made up of 3 subsets :

The DAC section:

It is joined to the main component, the DAC702 which is a digital/analogic converter with a current output.It has following required features:a stabiltty of +/-6ppm per degree and a slew rate of 10v/us.

The commands come from an interface panel via the GRAD.IN (50 pins SCSII) as a 16 bits word and are locked by two 8 bits registers 74als273 before driving the DAC inputs.

The offset section:

It allows the user to adjust the offset of the apparatus long-distance (from the spectrometer) via the linking RS232 serial (cannon connector 9 pins).

The command arrives by the I2C bus before beeing decoded by the special circuits PC8574 which transform it into a 12 bits word expected to drive the DAC AD7547 input.

The adjustement you can get at the DAC'S output is about +/-5V, that is to say a current of +/-100mA.

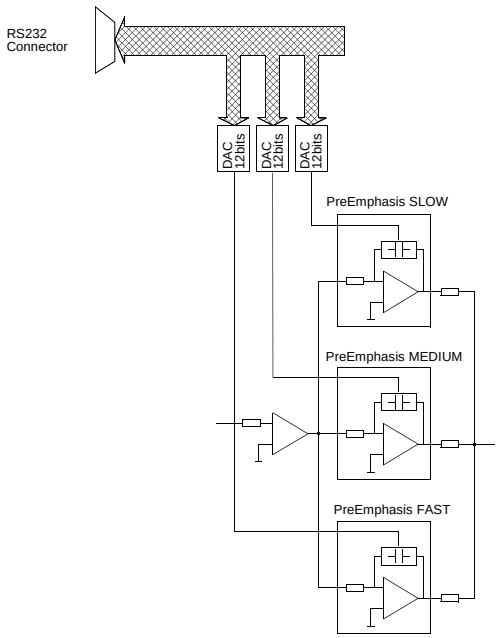
The disabled command section:

This command allows you to interrupt the power as it is described in paragraph ***"Power stage and regulation amplifier section" on page 12***.

The section of this paragraph consist in pulling down the reference at zero during a command.This information comes from the I2C bus as a +5V level and promotes an analogical DG201 switch.

PreEmphasis section *1.4.3*

Figure 1.7. PreEmphasis block diagram

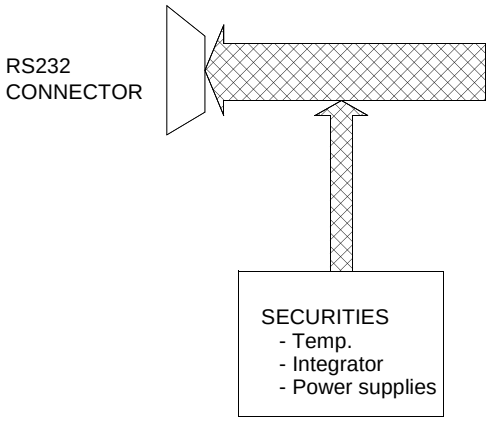


The pre-emphasis adjustement experiment should show up the smallest amount of residuel eddy currents and, for that reason, uses a gradient pulse much longer than normally employed in spectroscopy experiments.

The command section comes from the I2C bus like the offset adjustement, via the RS232 and, after the decoding, it will drive the 3 DAC'S 12 bits expected for the adjustement of the 3 pre-emphasis chanels.

The software allows a precise adjustement of the different time, gain and constants from the spectrometers console ; cursor make this possible.

Figure 1.8. Securities block diagram



The securities section is managed by a PAL which gets information from the different detection points.

This section is divided in 3 securities :

Temperature security

It is carried out by a 50 degrees thermoclip which opens as soon as the temperature exceed this value.

The thermoclip comes to the initial position after a while, if the overheating phenomenon has completely disappeared.

The integrator security :

This security is expected to protect the gradient coil in case the pulse would get too large (>100ms at 100% of the current with a cyclic ratio of 10) or in case of a DC current which is higher than the current which can be supported by the coil.

The adjustement of the release point (TP6) is fixed to 1.5V.As soon as this value is reached, the operating amplifier U15A releases.

Supply security :

This security is forseen in case of the supplies is missing,i.e :

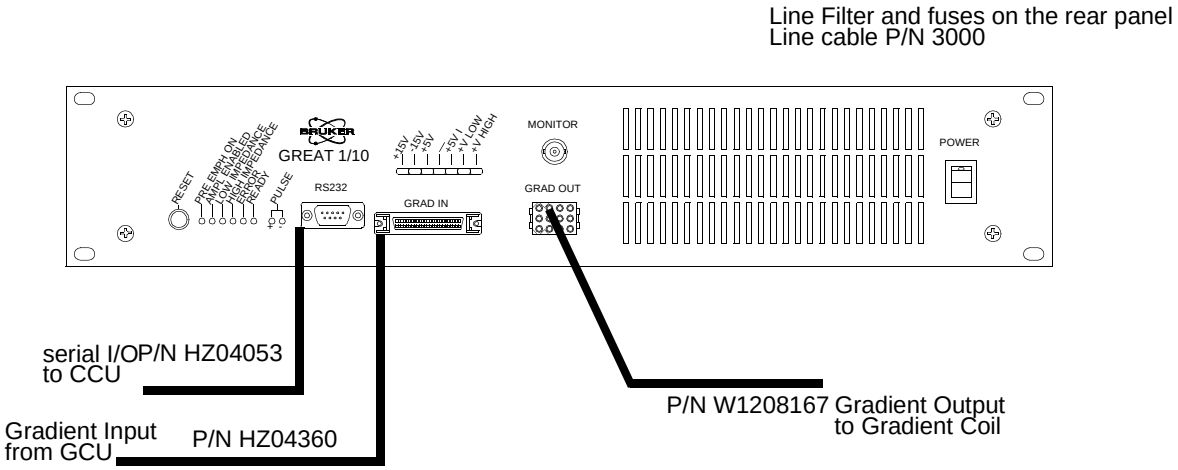
- +5VI which supplies the interface panel

- +5V which supplies all logical circuits of the power ampli panel.

- +/-15V which supplies all analogical circuits of the panel.

Gradient unit GREAT 1/10 *1.5*

Figure 1.9. Connections to GREAT 1/10



BBIS 2

General information about BBIS in the GREAT unit 2.1

BBIS („Bruker Board Information System“) data is stored in serial EEPROMs with an I^2C bus interface. There are three BBIS devices in the GREAT unit. The first is on a little PCB mounted directly to the case and contains data about the complete GREAT unit, the second is on the GREAT Interface Board and contains data about this board and the third is on the amplifier board and contains data relevant to it.

Every BBIS is seperated into four data blocks. The first data block is written during board- or unit test. It contains data about the board or unit in the state after production, details are described below. The second block contains actual data about the state of a board or unit after service. Block 3 and 4 are used for application specific data e.g. calibration values, parameters etc.

Unit BBIS Block 1 2.2

The Unit BBIS block 1 contains the following data:

1. BBIS Version for Block1:2
2. Protocol device name:<*blank*>
3. Shortname:GRTC
4. Part No.:W1207698
5. Serial No.:<Serial No.>
6. Print No.:<*blank*>
7. HW-Code after production:<HW-Code>
8. Date of production:<date of production>
9. Place of production:W
10. Department:<code of department>
11. Tester:<shortname of testing person>
12. Test place:<test place no.>
13. ECL after production:<EC level after production>

BBIS Block 1 on GREAT Interface Board *2.3*

The BBIS block 1 on the GREAT Interface Board contains the following data :

1. BBIS Version for Block1:2
2. Protocol device name:G
3. Shortname:GRT_
4. Part No.:H5785
5. Serial No.:<Serial No.>
6. Print No.:H4P2263B
7. HW-Code after production:<HW-Code>
8. Date of production:<date of production>
9. Place of production:H
10. Department:<code of department>
11. Tester:<shortname of testing person>
12. Test place:<test place no.>
13. ECL after production:<EC level after production>

BBIS Block 1 on Amplifier Module *2.4*

The BBIS block 1 on the amplifier board contains the following data :

1. BBIS Version for Block1:2
2. Protocol device name:<*blank*>
3. Shortname:GRTA
4. Part No.:W1207675
5. Serial No.:<Serial No.>
6. Print No.:W4P123740
7. HW-Code after production:<HW-Code>
8. Date of production:<date of production>
9. Place of production:W
10. Department:<code of department>
11. Tester:<shortname of testing person>
12. Test place:<test place no.>
13. ECL after production:<EC level after production>

Error Messages 3

Depending on whether the GREAT runs in boot firmware or in application firmware (usual case) the following error messages will be sent in the case of an error.

Table 3.1. Error messages from boot firmware

Error No.	Error message	Description
20	GRT_Order error	Unknown command or syntax error
2	GRT_Check sum error	Wrong command string checksum
37	GRT_Erase fail	Download: Flash EPROM erase failed or not complete
36	GRT_Programmer fail	Download: Flash EPROM programming failed or not complete
33	GRT_Wrong rec type	Download: record is not Intel hex format
32	GRT_Wrong address	Download: address out of valid Flash EPROM address range
34	GRT_Wrong checksum	Download: wrong checksum in Intel hex record
38	GRT_Wrong transmission check	Download: wrong EOF record
31	GRT_Wrong data count	Download: wrong length of Intel hex string
11	GRT_ROM error	no valid application software on Flash EPROM
15	GRT_BBIS error	no BBIS available
16	GRT_BBIS checksum error block1	wrong data in BBIS block1
17	GRT_BBIS checksum error block2	wrong data in BBIS block2
18	GRT_BBIS checksum error block3	wrong data in BBIS block3
19	GRT_BBIS checksum error block4	wrong data in BBIS block4

Table 3.2. Error messages from application firmware

Error No.	Error message	Description
20	GRT_Order error	Unknown command or syntax error
2	GRT_Check sum error	Wrong command string checksum
16	GRT_??Corrupt data in BBIS ? block1, bus ?	wrong data in BBIS No.?, bus No.?, block1
17	GRT_??Corrupt data in BBIS ? block2, bus ?	wrong data in BBIS No.?, bus No.?, block2
18	GRT_??Corrupt data in BBIS ? block3, bus ?	wrong data in BBIS No.?, bus No.?, block3
19	GRT_??Corrupt data in BBIS ? block4, bus ?	wrong data in BBIS No.?, bus No.?, block4
15	GRT_??BBIS ? bus ? not responding	no BBIS No.?, bus No.? available
71	GRT_Error in record length	wrong record length of PreEmphasis parameter string
72	GRT_Pointer out of range	pointer to PreEmphasis parameter out of buffer range
73	GRT_Amplifier error	security relevant error on amplifier module, amplifier is disabled
74	GRT_No response from status port	no response from status port chip on amplifier module via I2C bus
75	GRT_No response from PreEmph port	no response from PreEmphasis parameter port chip on amplifier module via I2C bus
76	GRT_No response from loop param port	no response from loop parameter port chip on amplifier module via I2C bus
77	GRT_I2C Parallel Port Error	no response from I2C bus parallel port (only with test command „G1“)
97	GRT_PreEmphasis Bypass is ON	you tried to load PreEmphasis parameter while Bypass is switched ON

Connector Pinout

4

Connector X6: Gradient Input from GCU 4.1

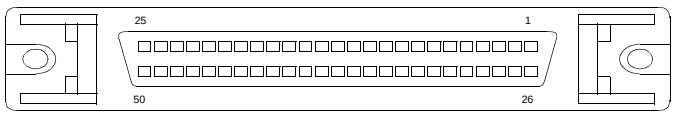


Table 4.1. Pinout Connector X6

Pin	Signal	Pin	Signal
1	NGI-	26	GD+3
2	NGI+	27	GD-4
3		28	GD+4
4		29	GD-5
5	DAS-	30	GD+5
6	DAS+	31	GD-6
7	GDTR-	32	GD+6
8	GDTR+	33	GD-7
9	WRS-	34	GD+7
10	WRS+	35	GD-8
11	GADD-0	36	GD+8
12	GADD+0	37	GD-9
13	GADD-1	38	GD+9
14	GADD+1	39	GD-10
15	GADD-2	40	GD+10
16	GADD+2	41	GD-11
17	GADD-3	42	GD+11
18	GADD+3	43	GD-12
19	GD-0	44	GD+12
20	GD+0	45	GD-13
21	GD-1	46	GD+13
22	GD+1	47	GD-14
23	GD-2	48	GD+14
24	GD+2	49	GD-15
25	GD-3	50	GD+15

Connector X3: RS232to CCU 4.2

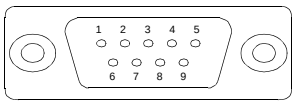


Table 4.2. Pinout Connector X3

Pin	Signal
1	GND_RS232
2	
3	DTR
4	CTS
5	/TXD
6	RTS
7	/RXD
8	DSR
9	

Connector X2: I^2C Bus to Universal BBIS Board 4.3

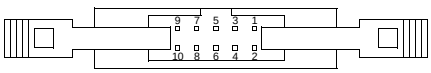


Table 4.3. Pinout Connector X2

Pin	Signal
1	VCC
2	VCC
3	GND
4	GND
5	GND
6	SCLK
7	SDATA
8	GND
9	GND
10	GND

Connector X7: Gradient output to amplifier module *4.4*

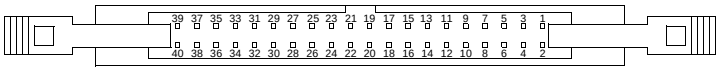


Table 4.4. Pinout Connector X7

Pin	Signal	Pin	Signal
1	+5V_AMP	2	+5V_AMP
3	GND_AMP	4	ZDOUT0
5	GND_AMP	6	ZDOUT1
7	GND_AMP	8	ZDOUT2
9	GND_AMP	10	ZDOUT3
11	GND_AMP	12	ZDOUT4
13	GND_AMP	14	ZDOUT5
15	GND_AMP	16	ZDOUT6
17	GND_AMP	18	ZDOUT7
19	GND_AMP	20	ZDOUT8
21	GND_AMP	22	ZDOUT9
23	GND_AMP	24	ZDOUT10
25	GND_AMP	26	ZDOUT11
27	GND_AMP	28	ZDOUT12
29	GND_AMP	30	ZDOUT13
31	GND_AMP	32	ZDOUT14
33	GND_AMP	34	ZDOUT15
35	GND_AMP	36	STROBE
37	GND_AMP	38	
39	+5V_AMP	40	+5V_AMP

Connector X8: Digital control signals to amplifier module *4.5*

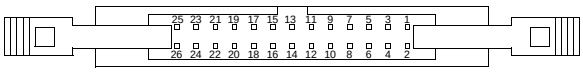


Table 4.5. Pinout Connector X8

Pin	Signal	Pin	Signal
1	+5V_AMP	2	+5V_AMP
3	GND_AMP	4	SDATA
5	GND_AMP	6	SCLK
7	GND_AMP	8	/INT
9	GND_AMP	10	/WRMUX
11	GND_AMP	12	/ENABLE_AMP
13	GND_AMP	14	/RESET_AMP
15	GND_AMP	16	PULS(+)
17	GND_AMP	18	PULS(-)
19	GND_AMP	20	
21		22	
23		24	
25	+5V_AMP	26	+5V_AMP

Interface baord Schematics

5

Figure 5.1. GREAT Interface Board Layout

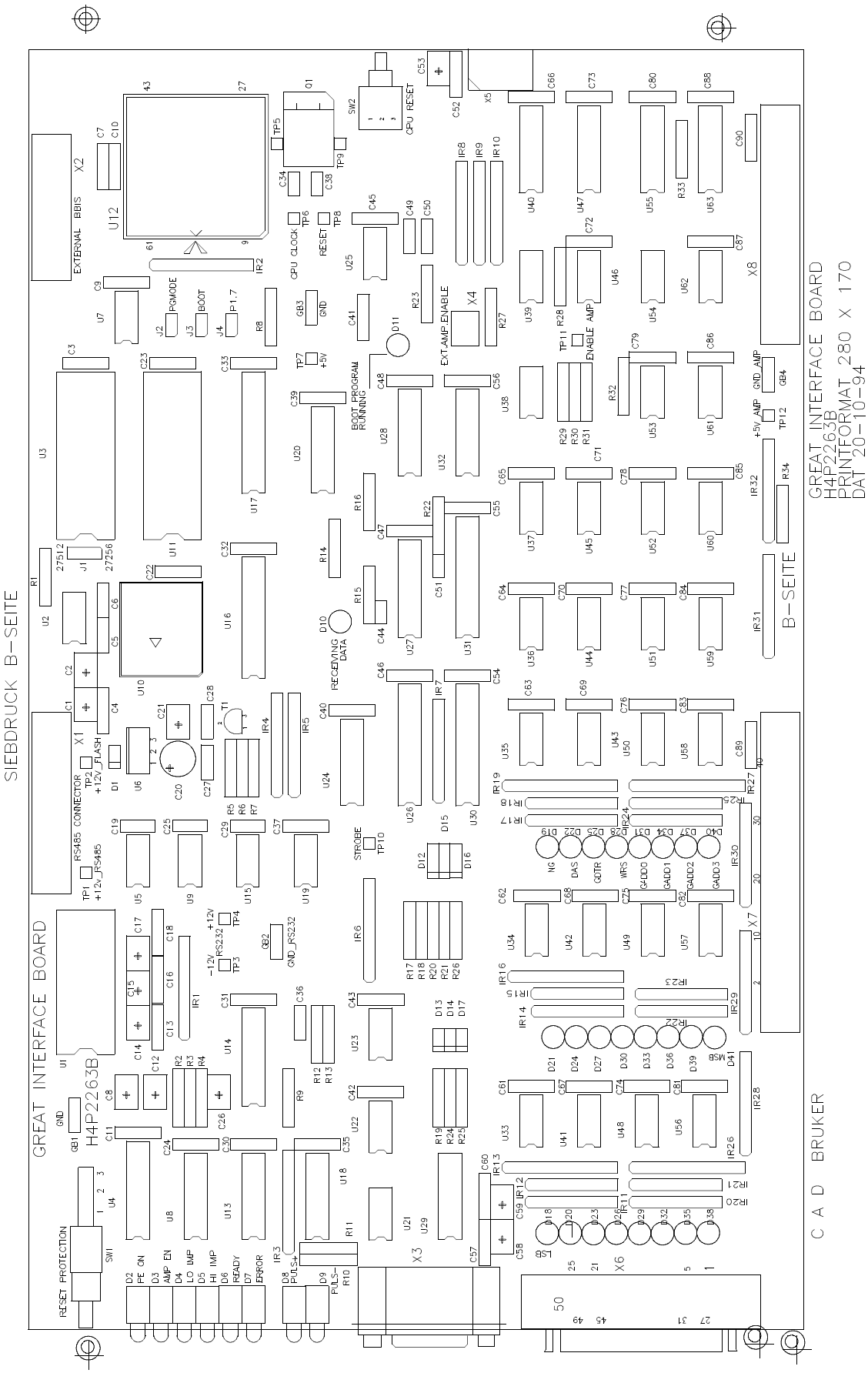
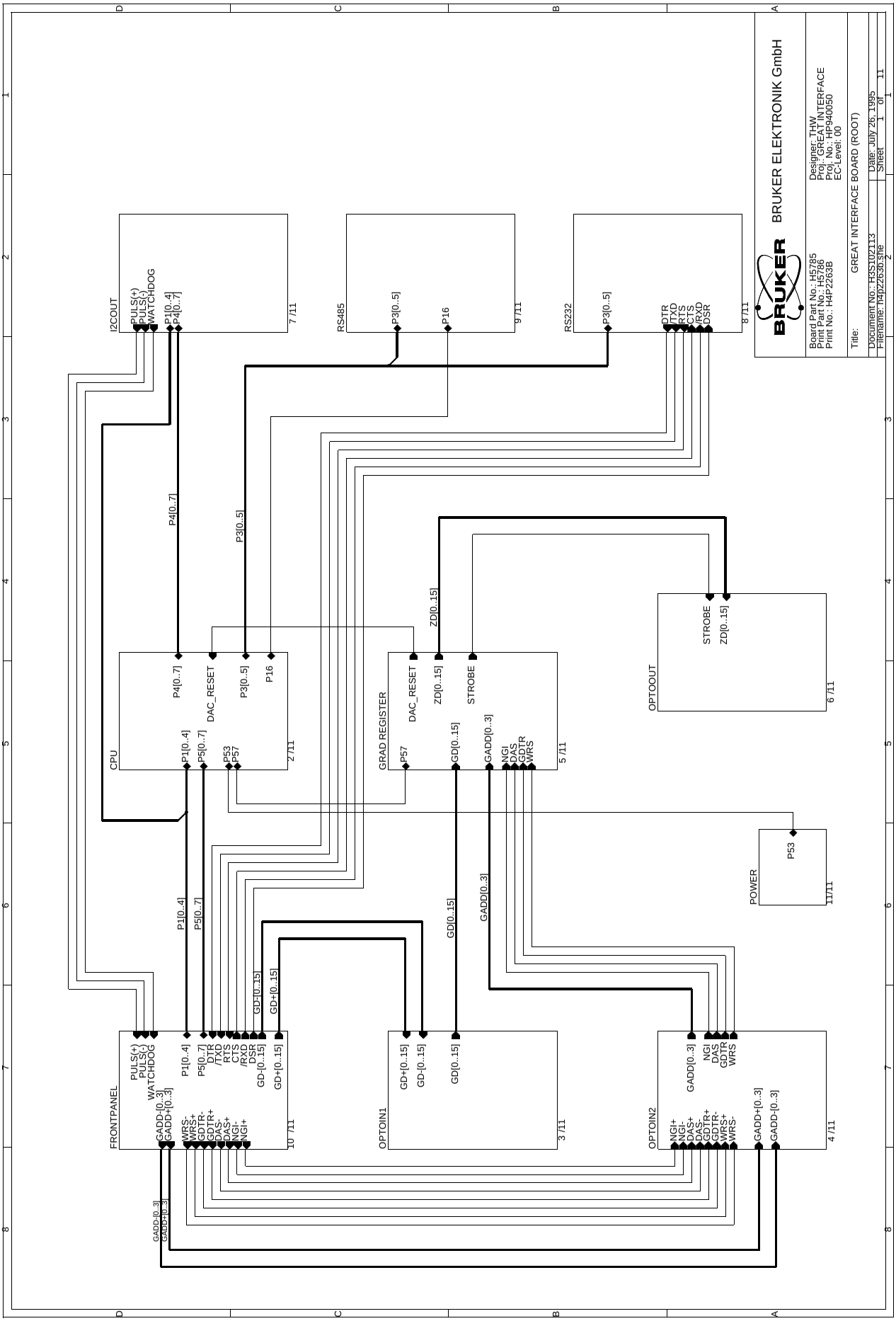


Figure 5.2. GREAT Interface Board Schematic Page 1 of 11



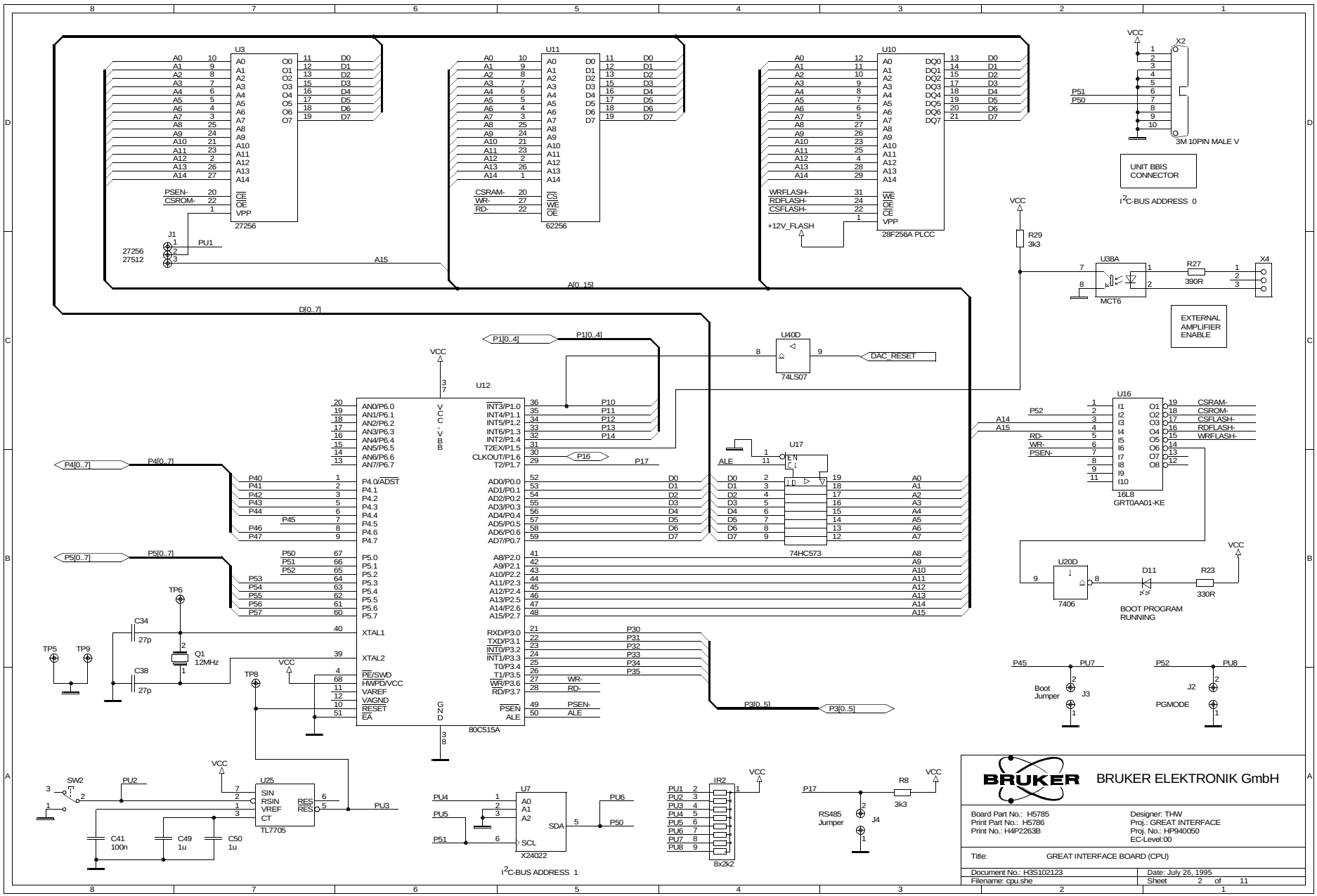


Figure 5.3. GREAT Interface Board Schematic Page 2 of 11

Figure 5.4. GREAT Interface Board Schematic Page 3 of 11

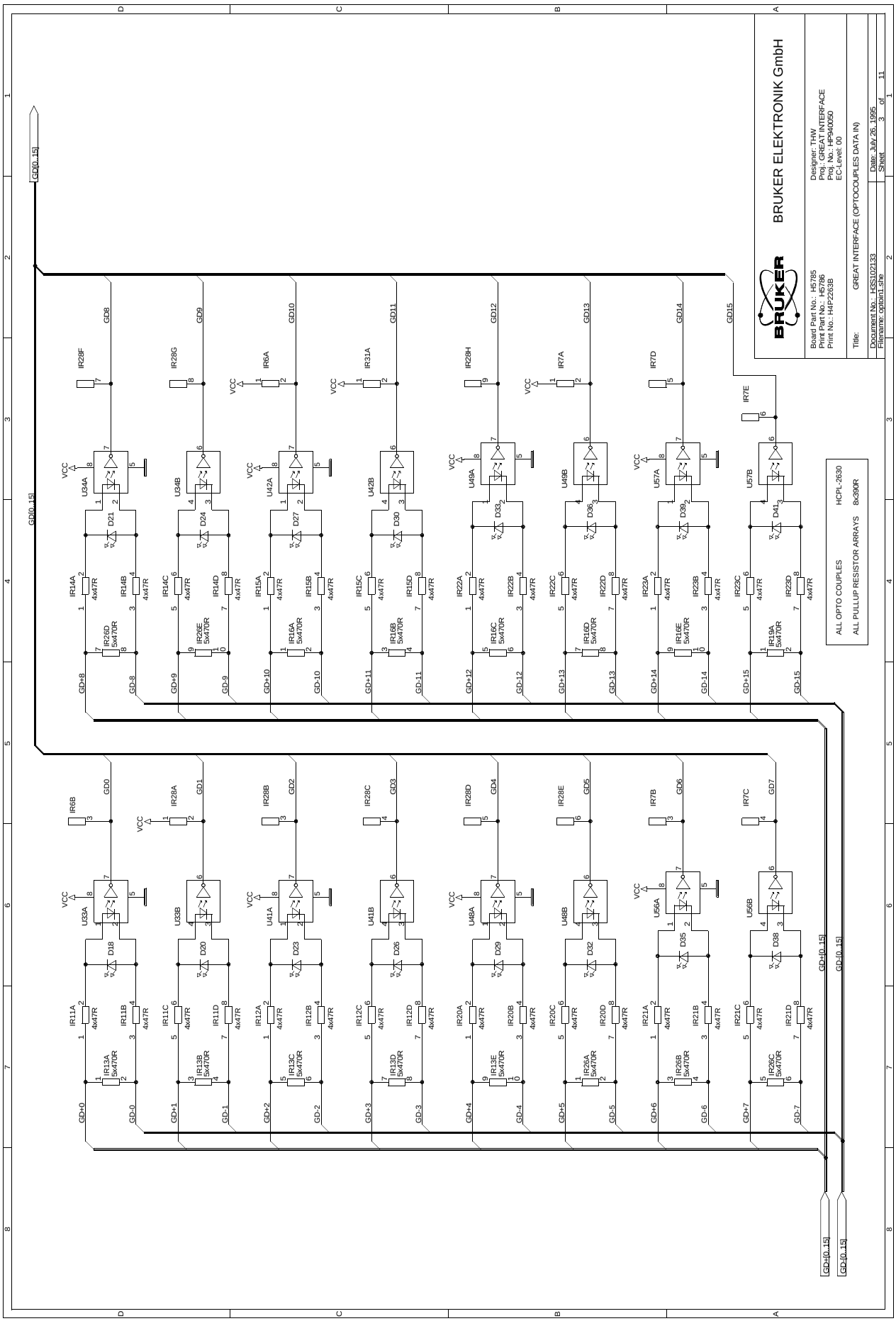


Figure 5.5. GREAT Interface Board Schematic Page 4 of 11

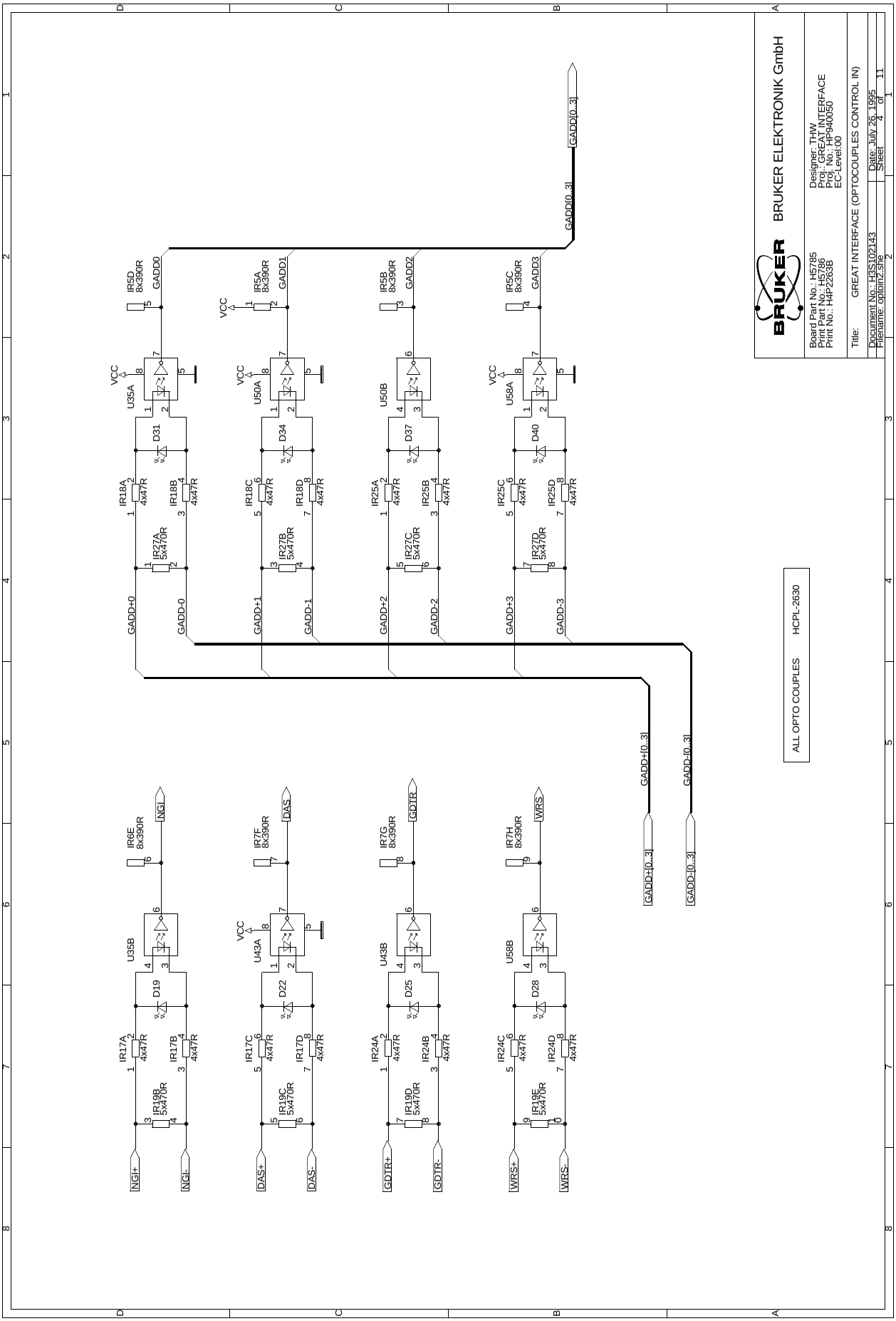


Figure 5.6. GREAT Interface Board Schematic Page 5 of 11

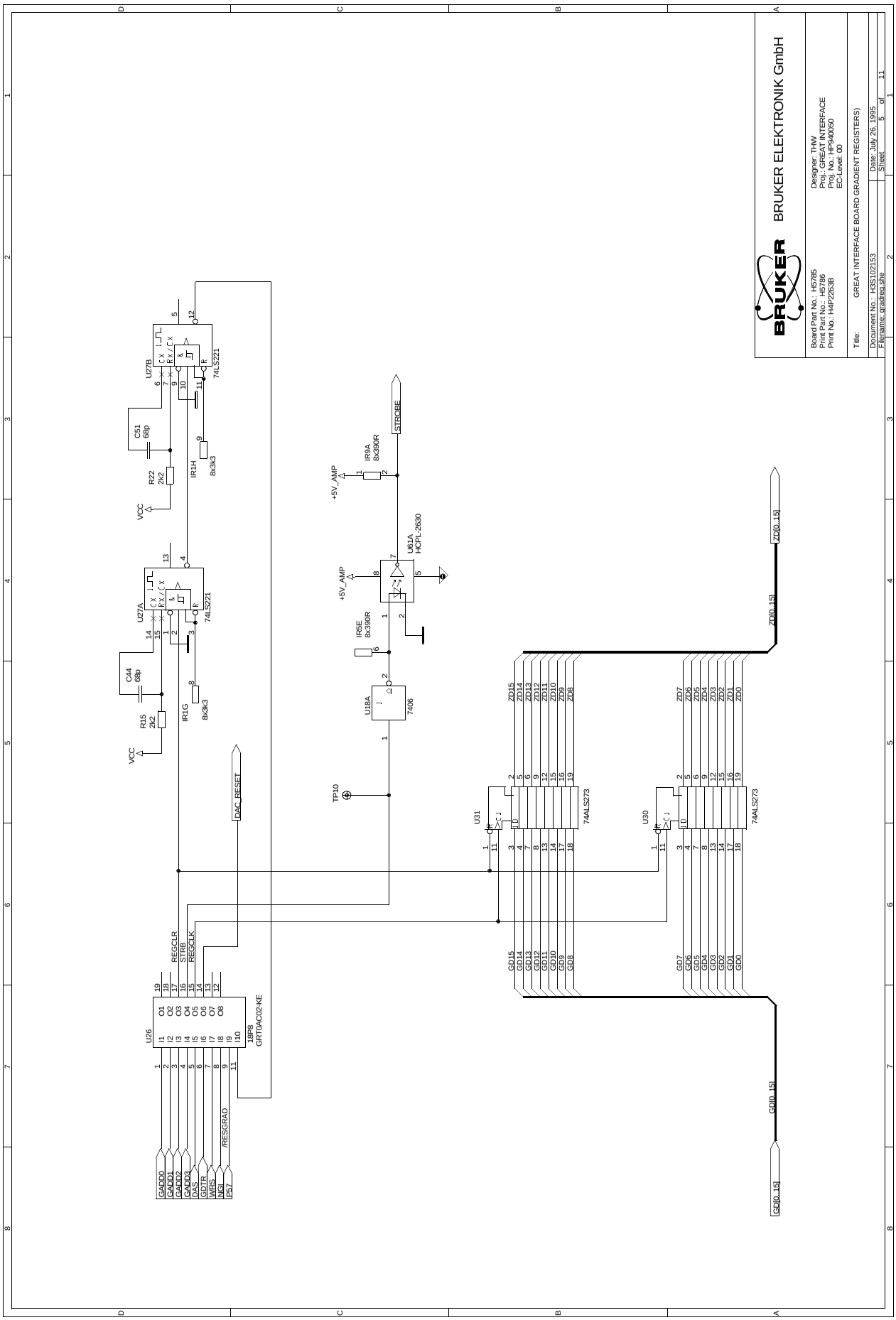


Figure 5.7. GREAT Interface Board Schematic Page 6 of 11

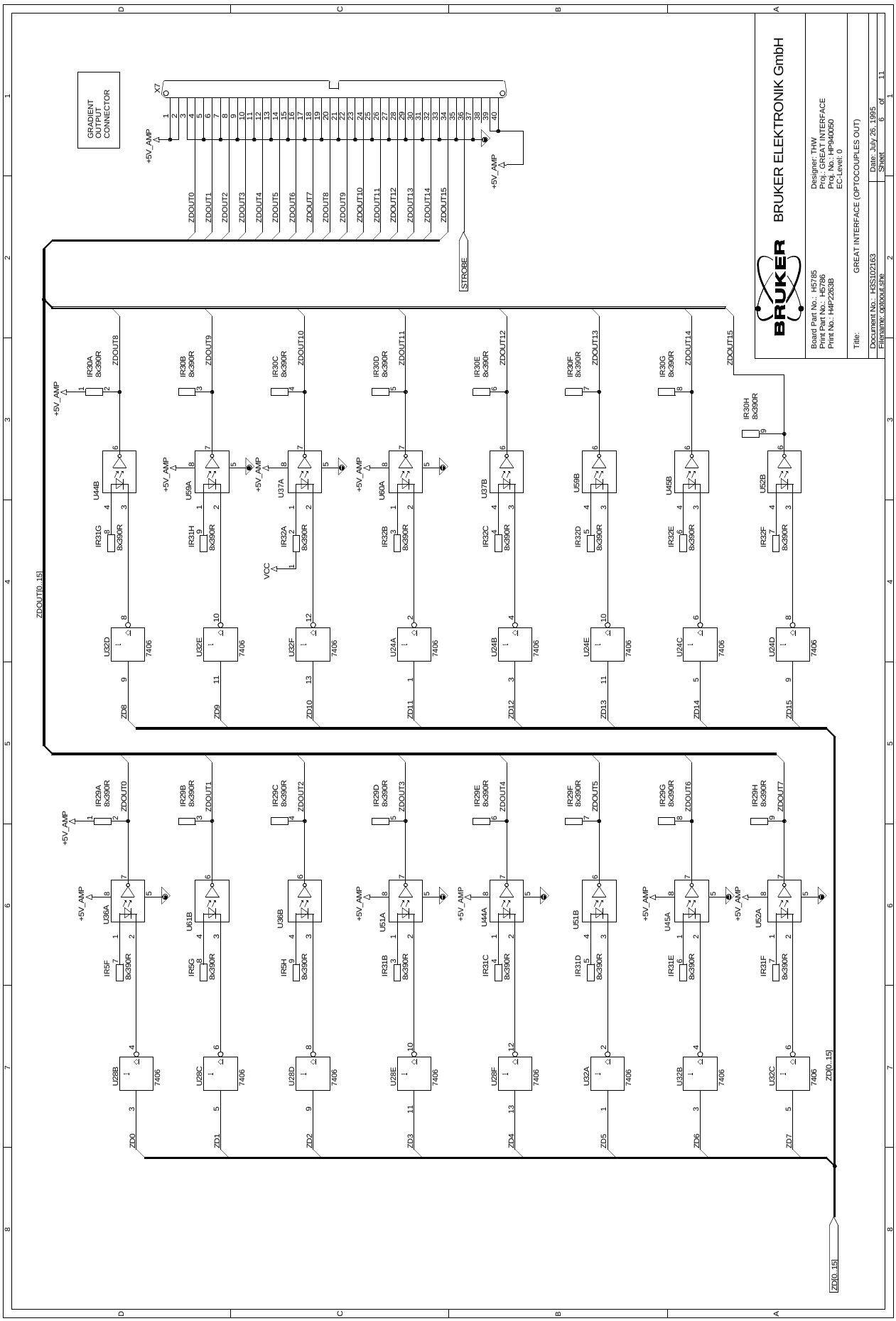


Figure 5.8. GREAT Interface Board Schematic Page 7 of 11

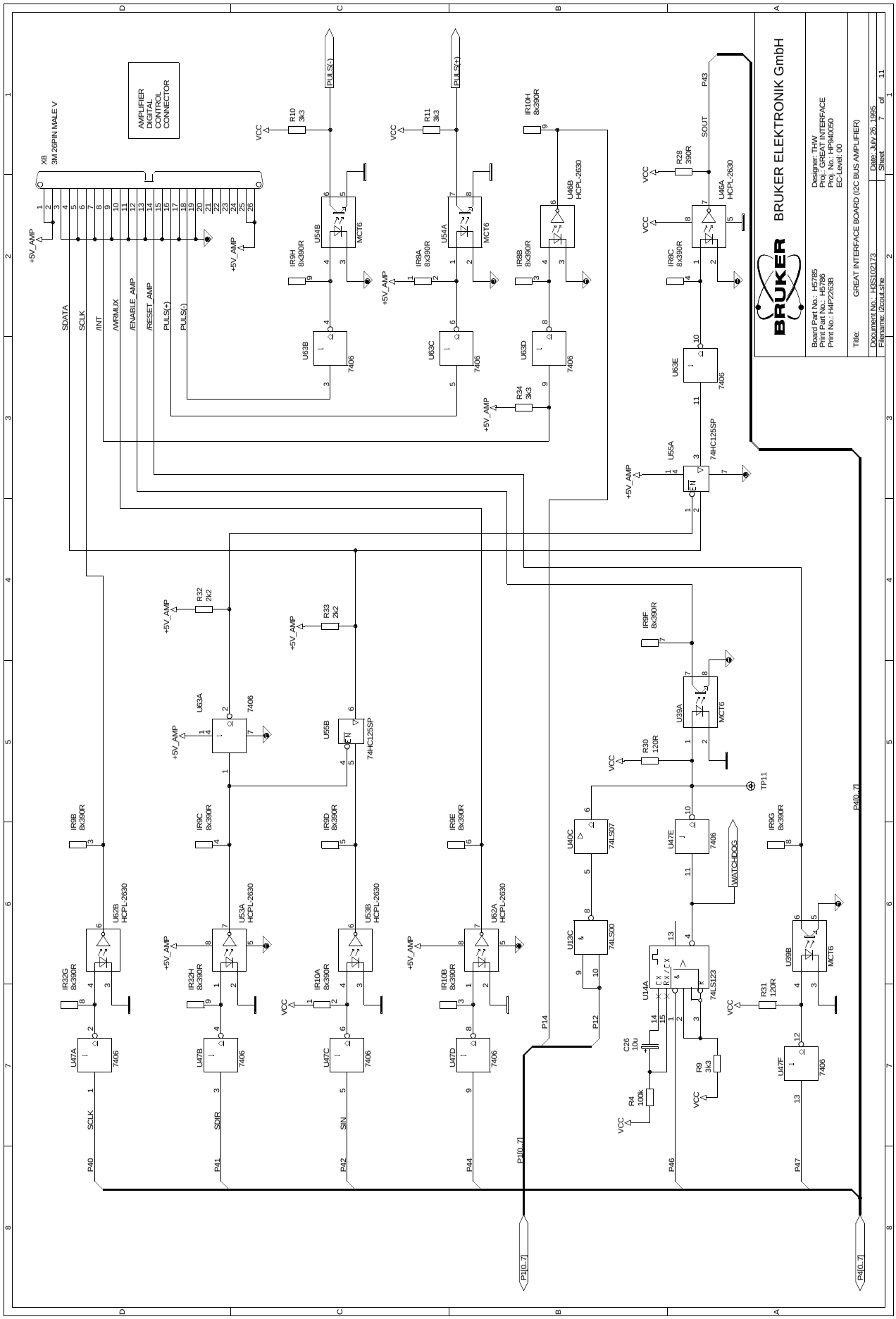


Figure 5.9. GREAT Interface Board Schematic Page 8 of 11

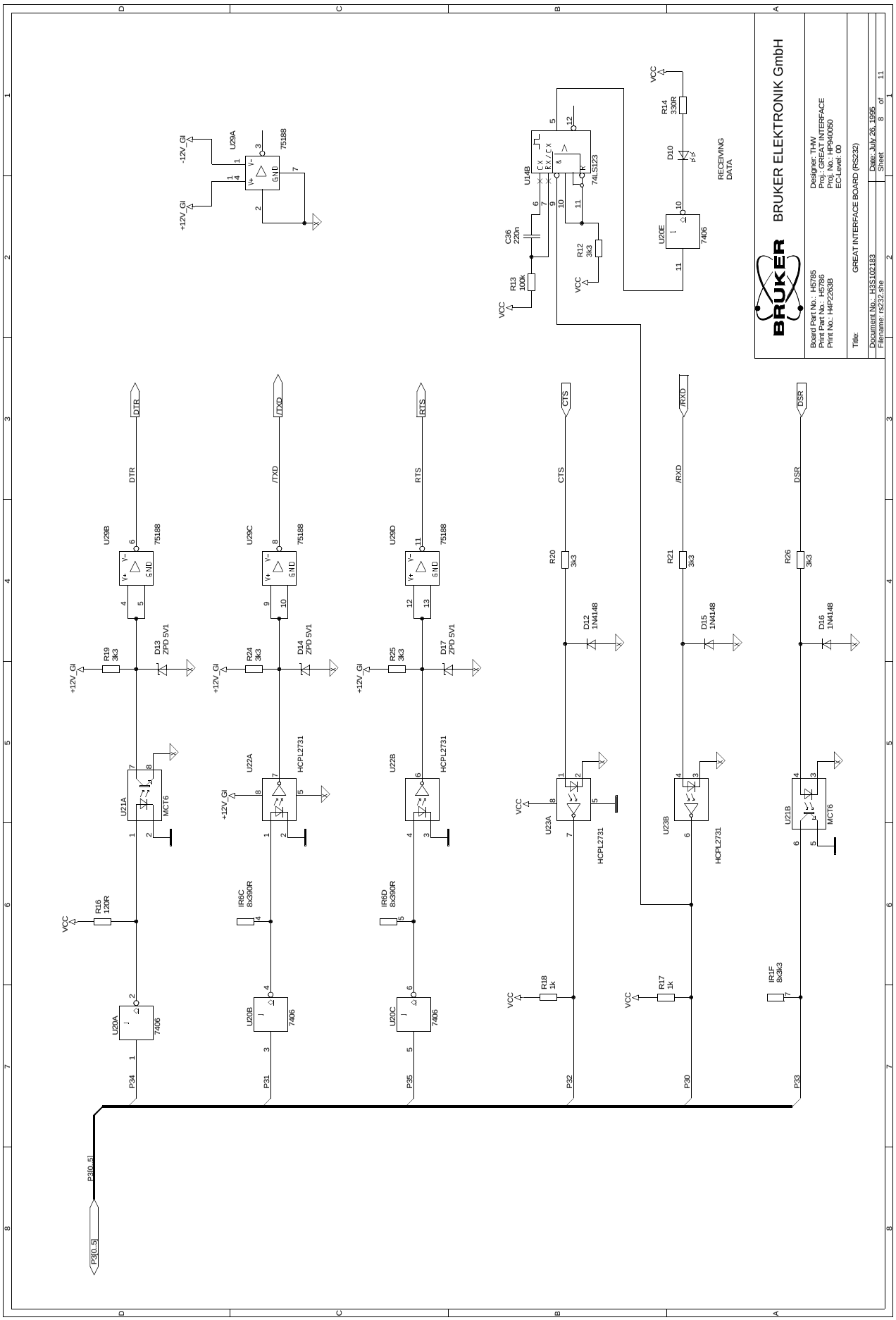
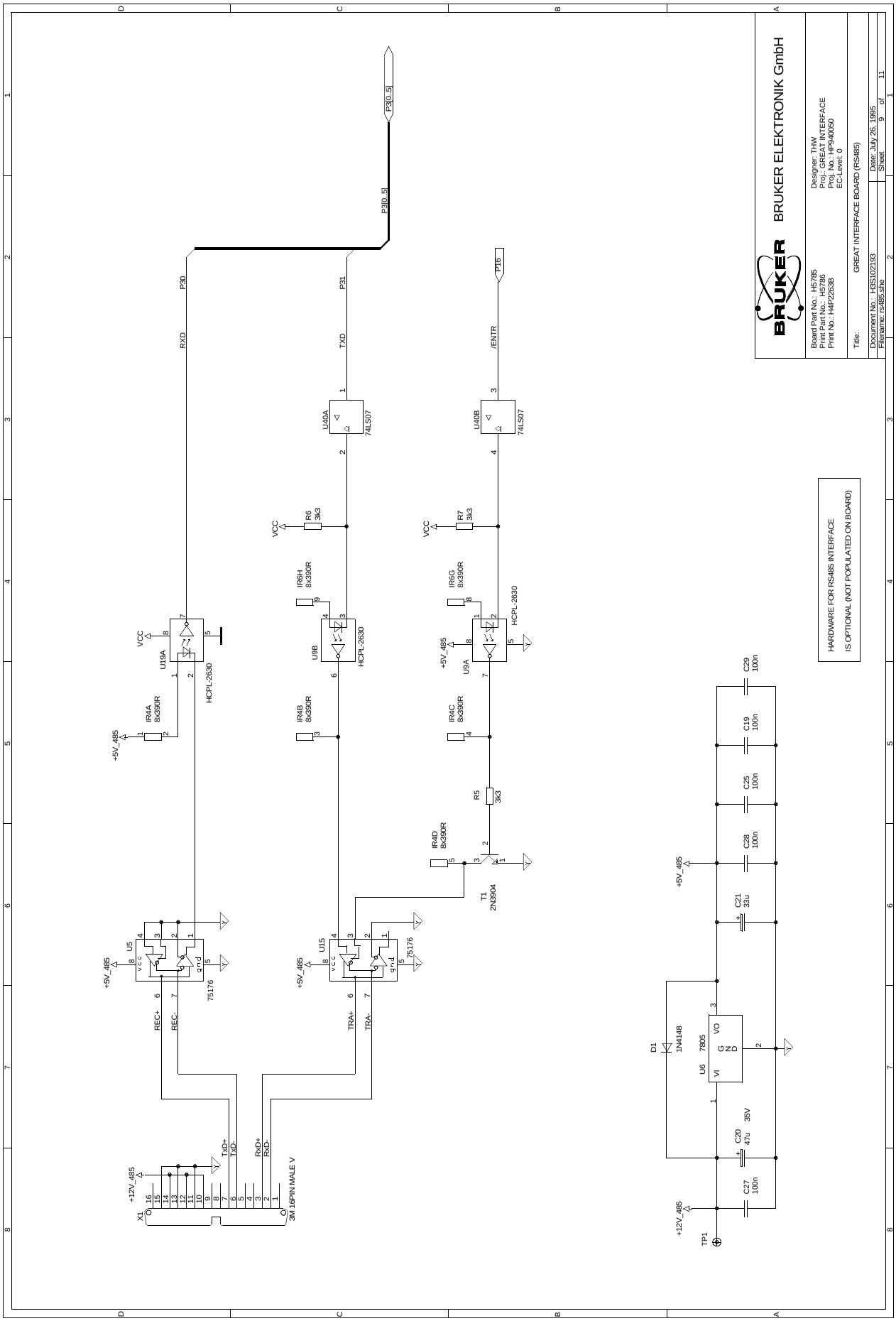


Figure 5.10. GREAT Interface Board Schematic Page 9 of 11



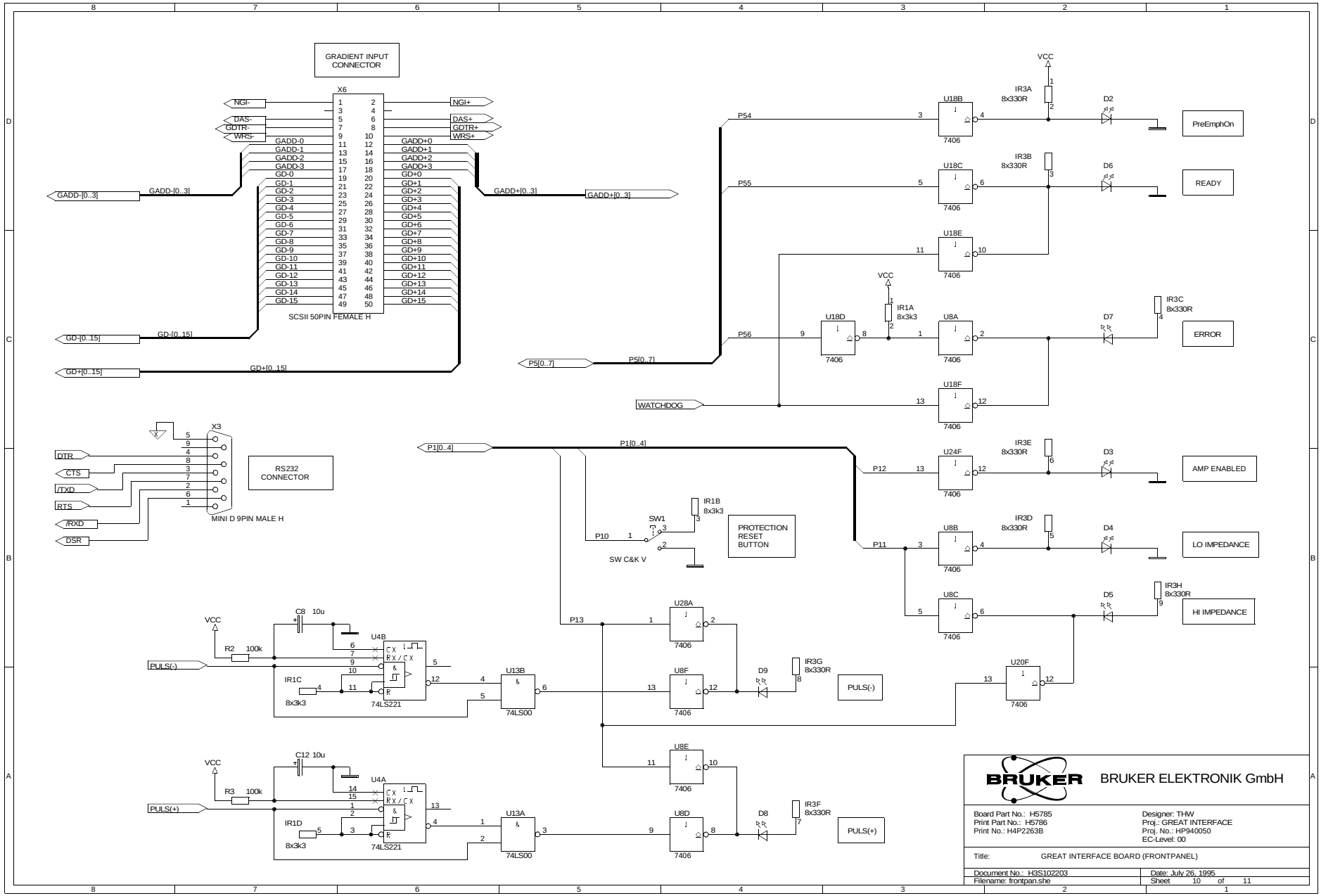
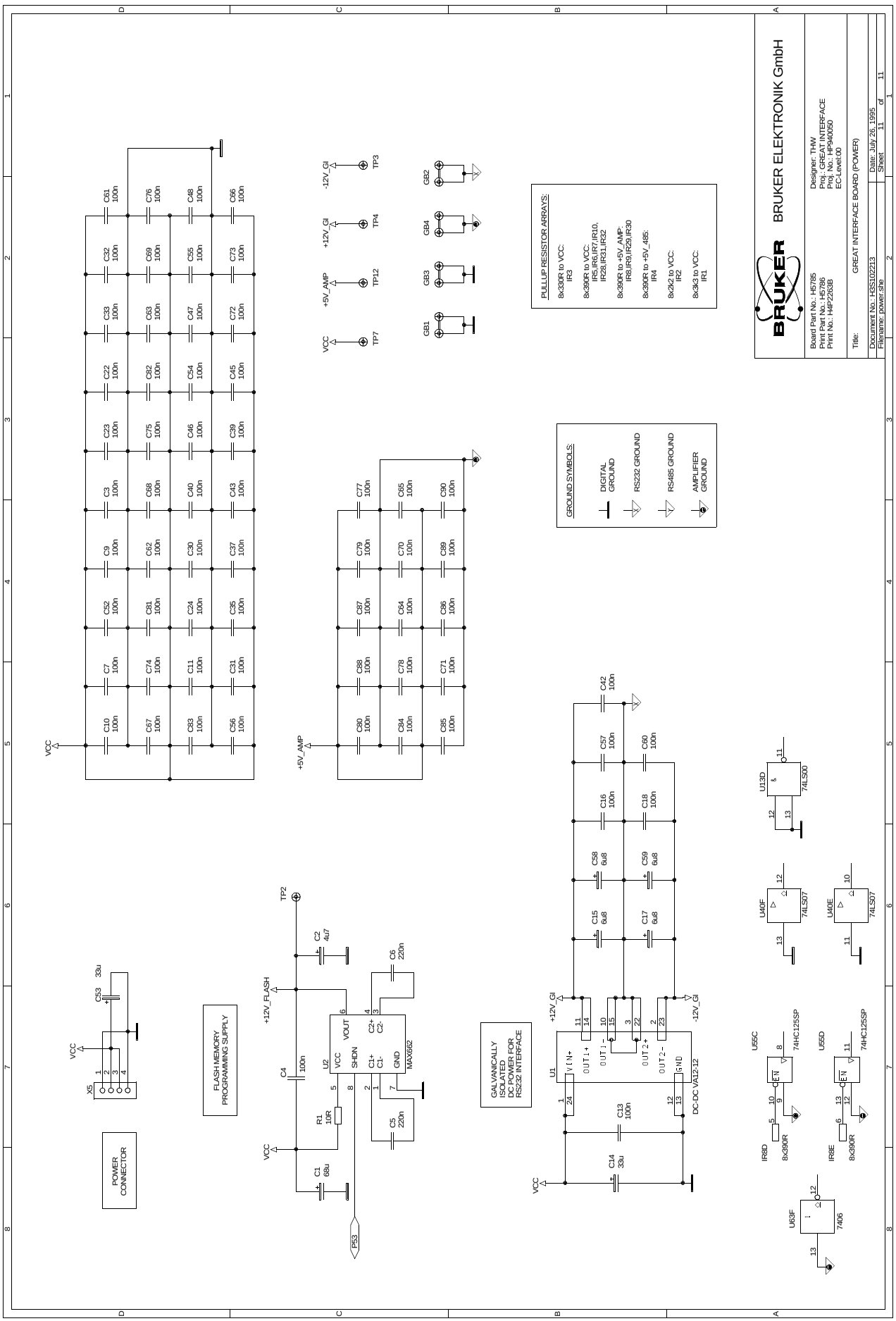


Figure 5.11. GREAT Interface Board Schematic Page 10 of 11

Figure 5.12. GREAT Interface Board Schematic Page 11 of 11



Amplifier board Schematics

6

Figure 6.1. GREAT Amplifier Module Board Layout

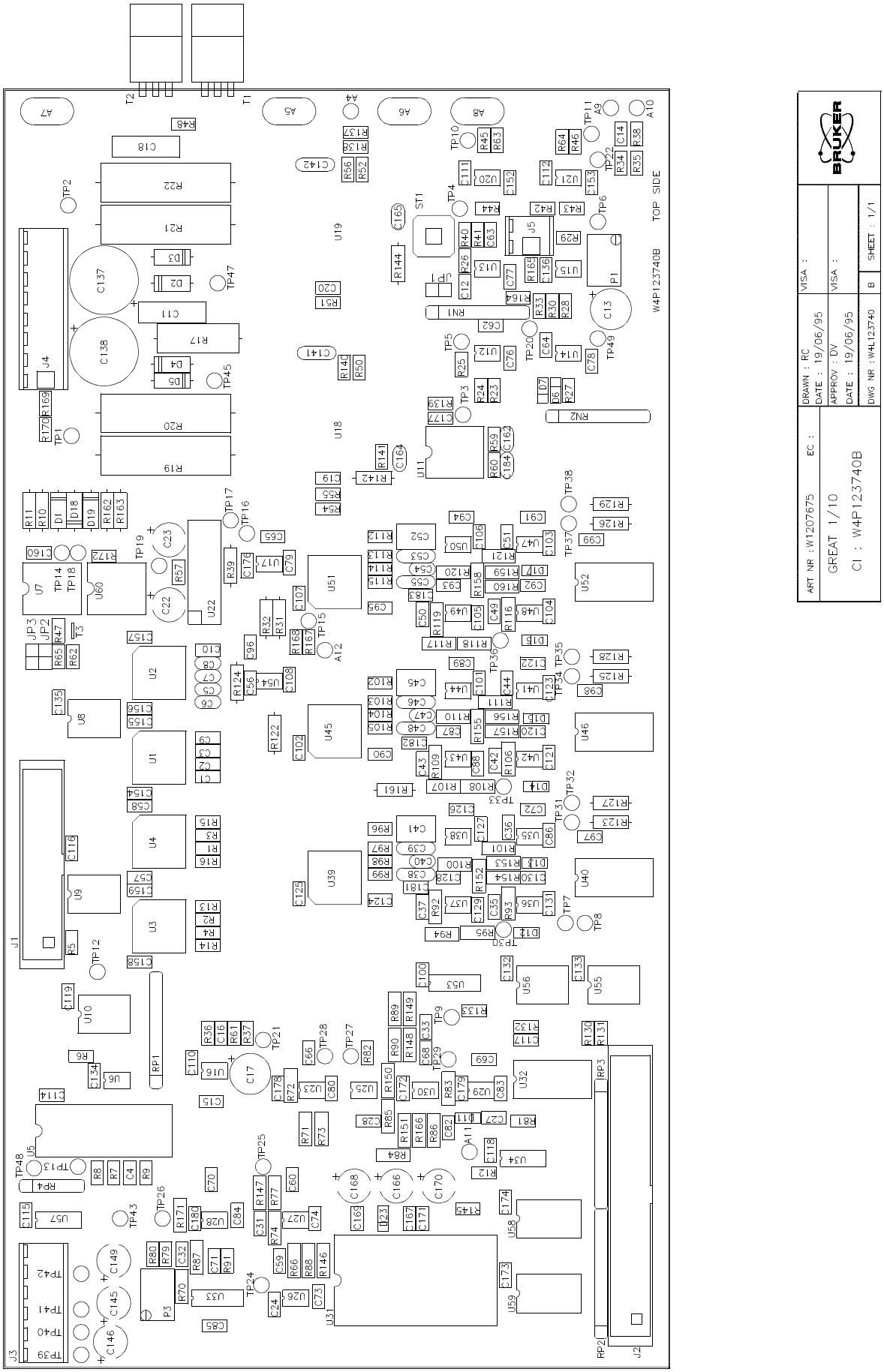


Figure 6.2. GREAT Amplifier Board Schematic page 1 of 8

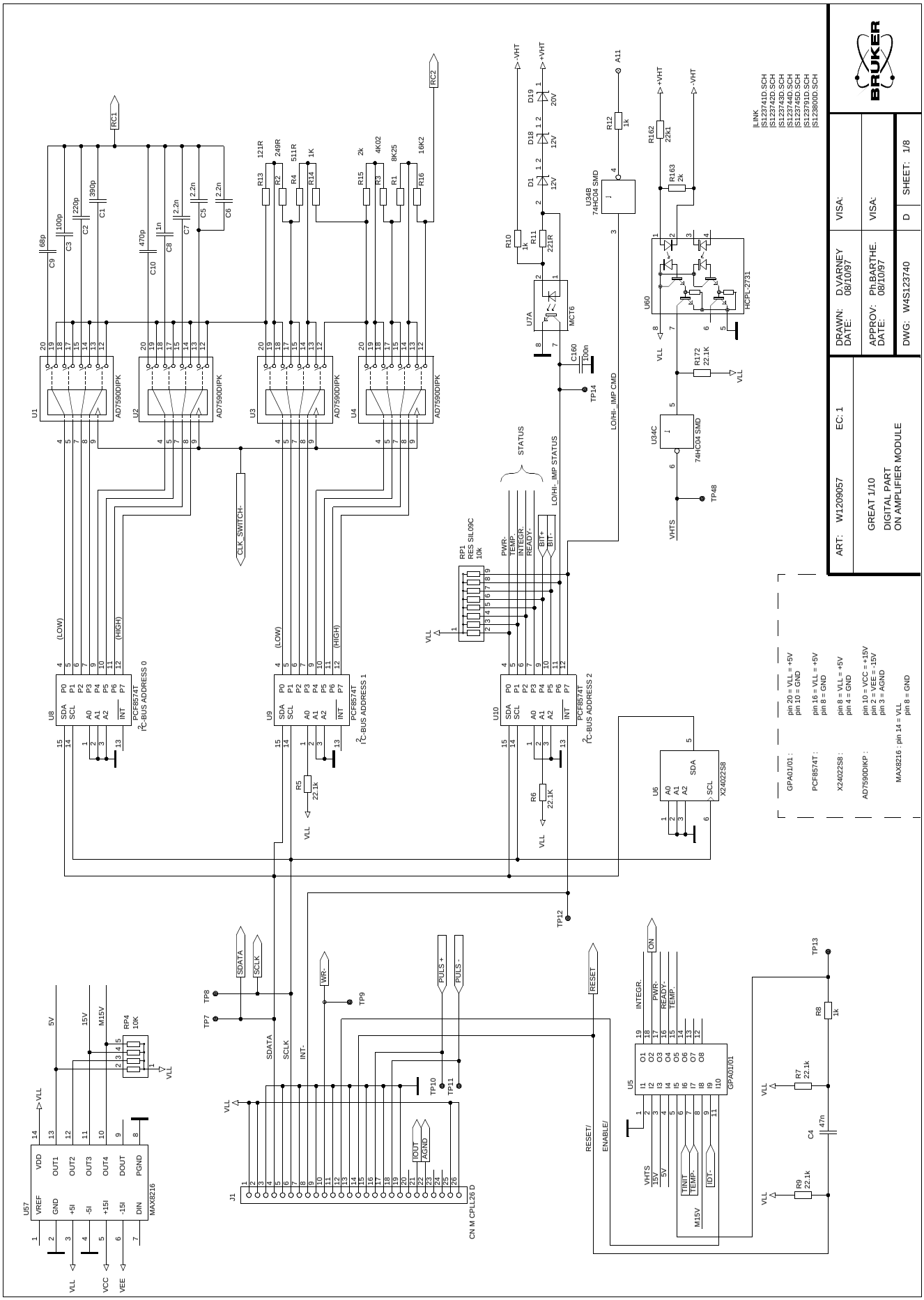


Figure 6.3. GREAT Amplifier Board Schematic page 2 of 8

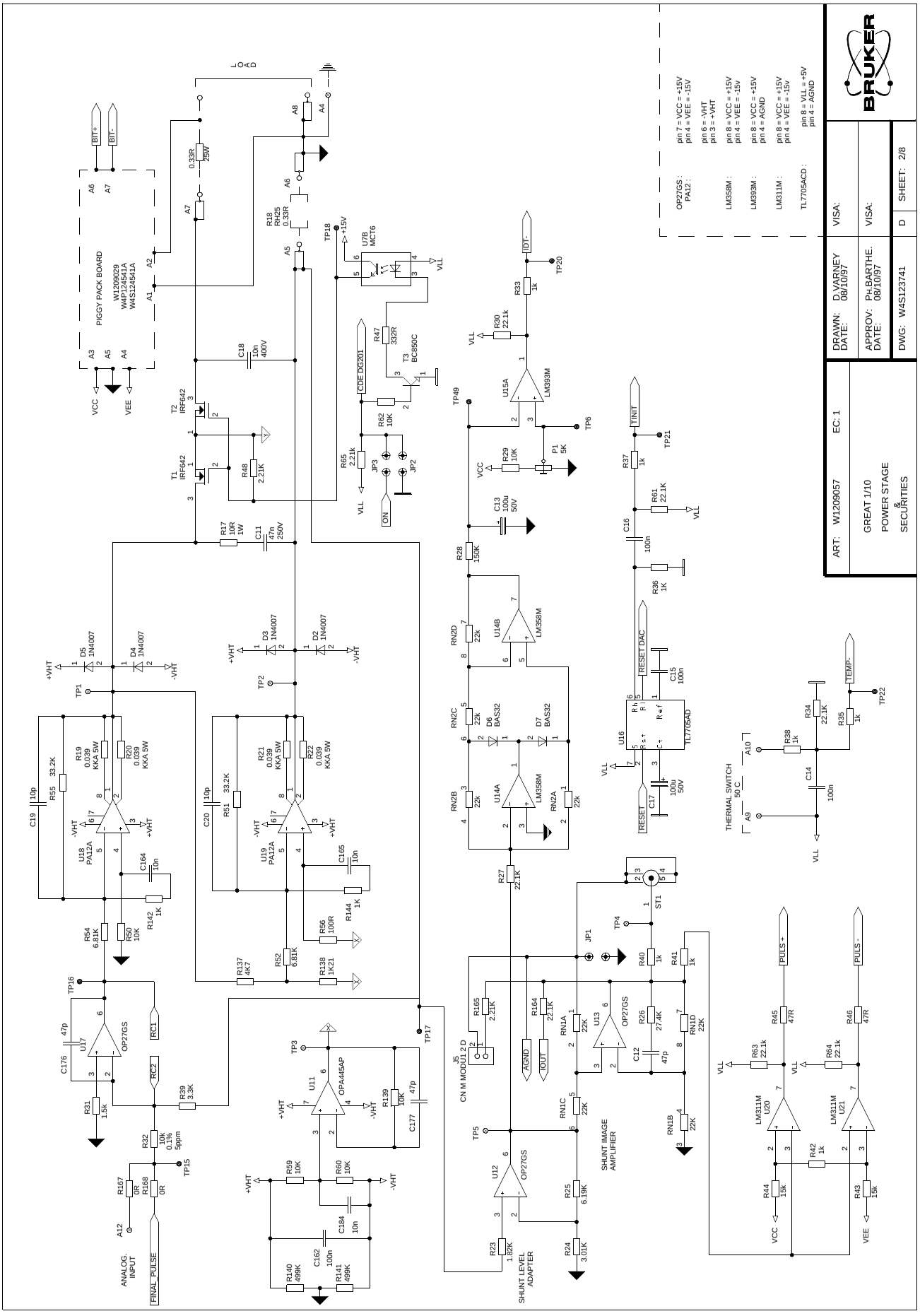
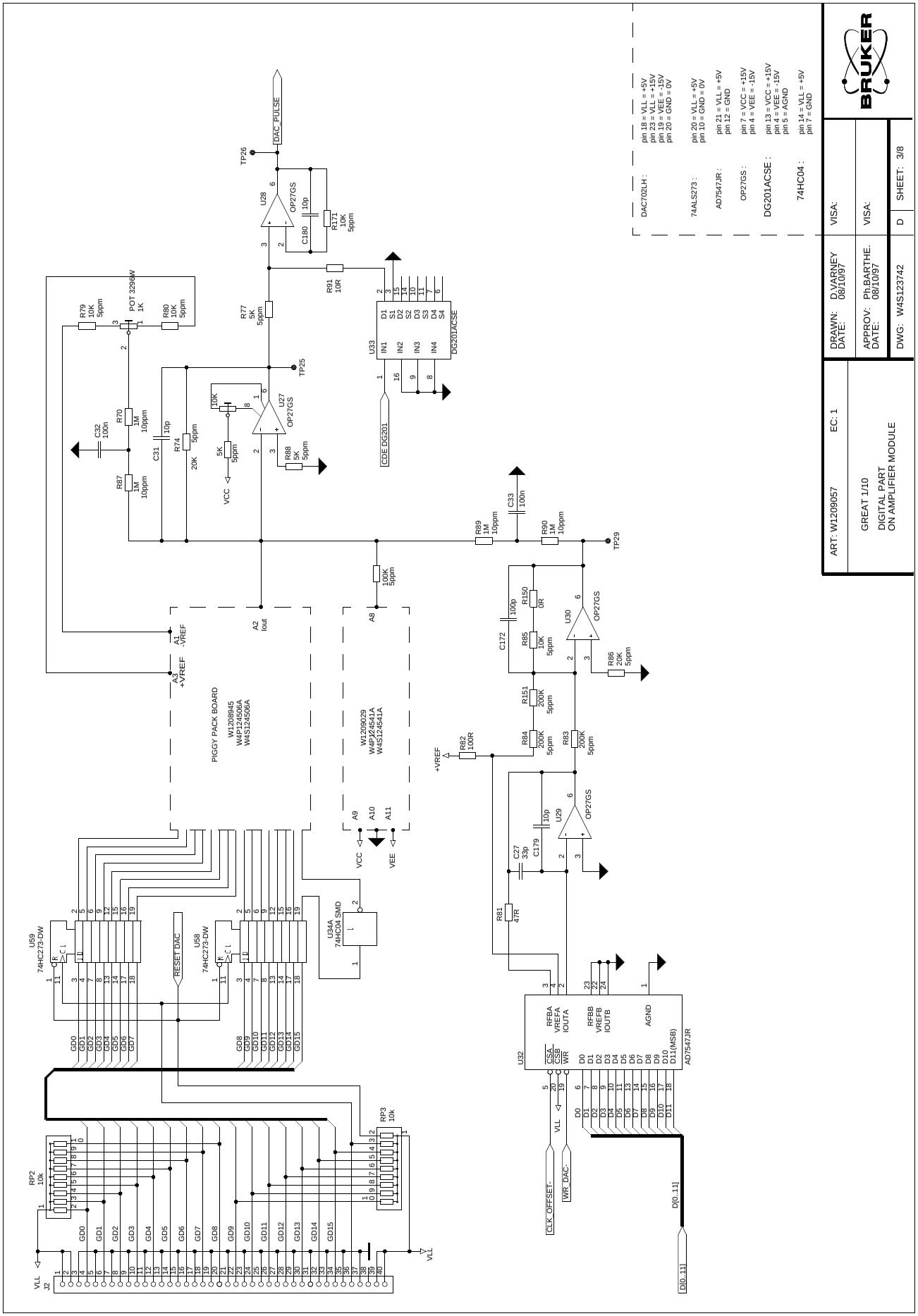


Figure 6.4. GREAT Amplifier Board Schematic page 3 of 8



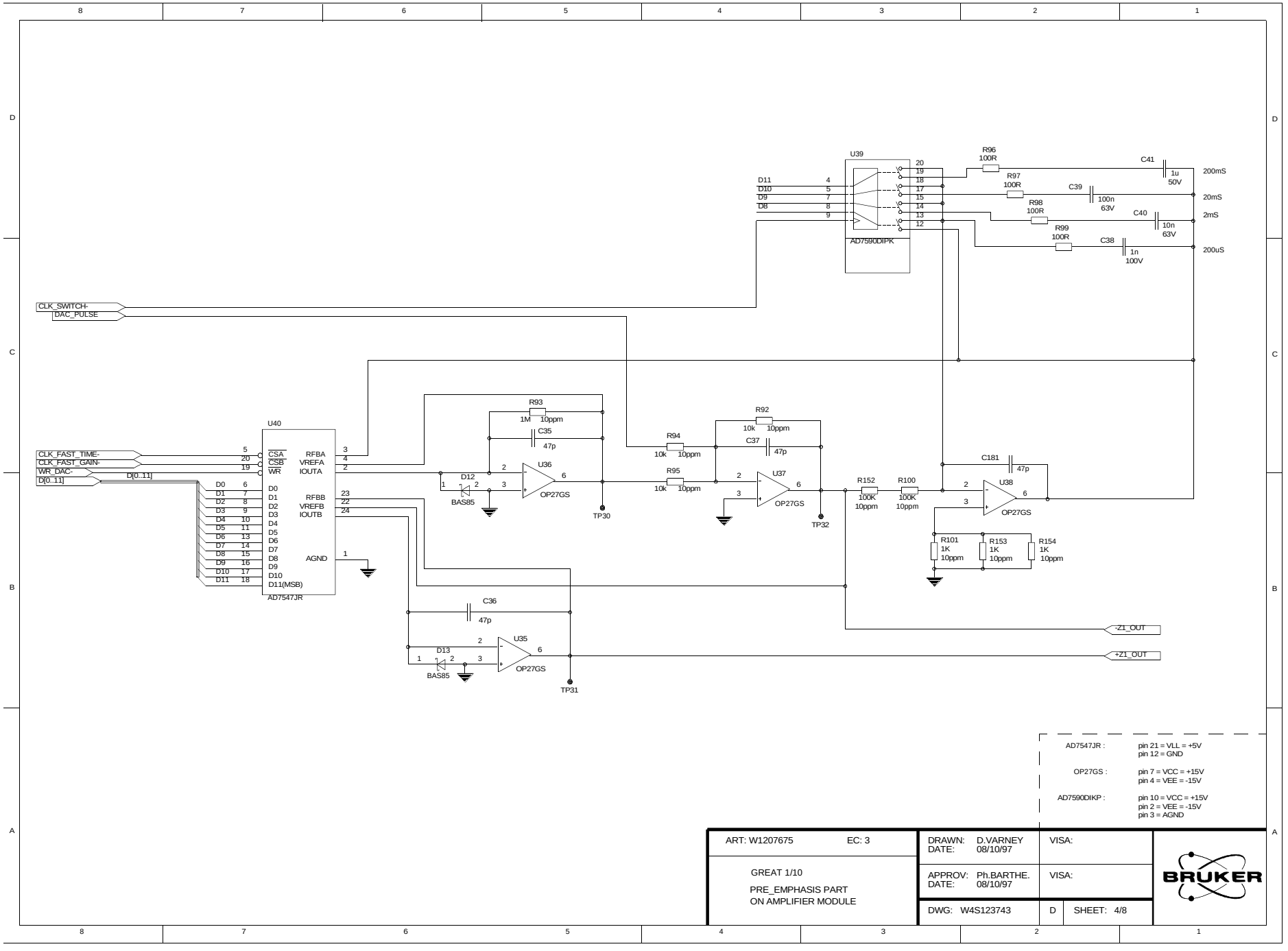


Figure 6.5. GREAT Amplifier Board Schematic page 4 of 8

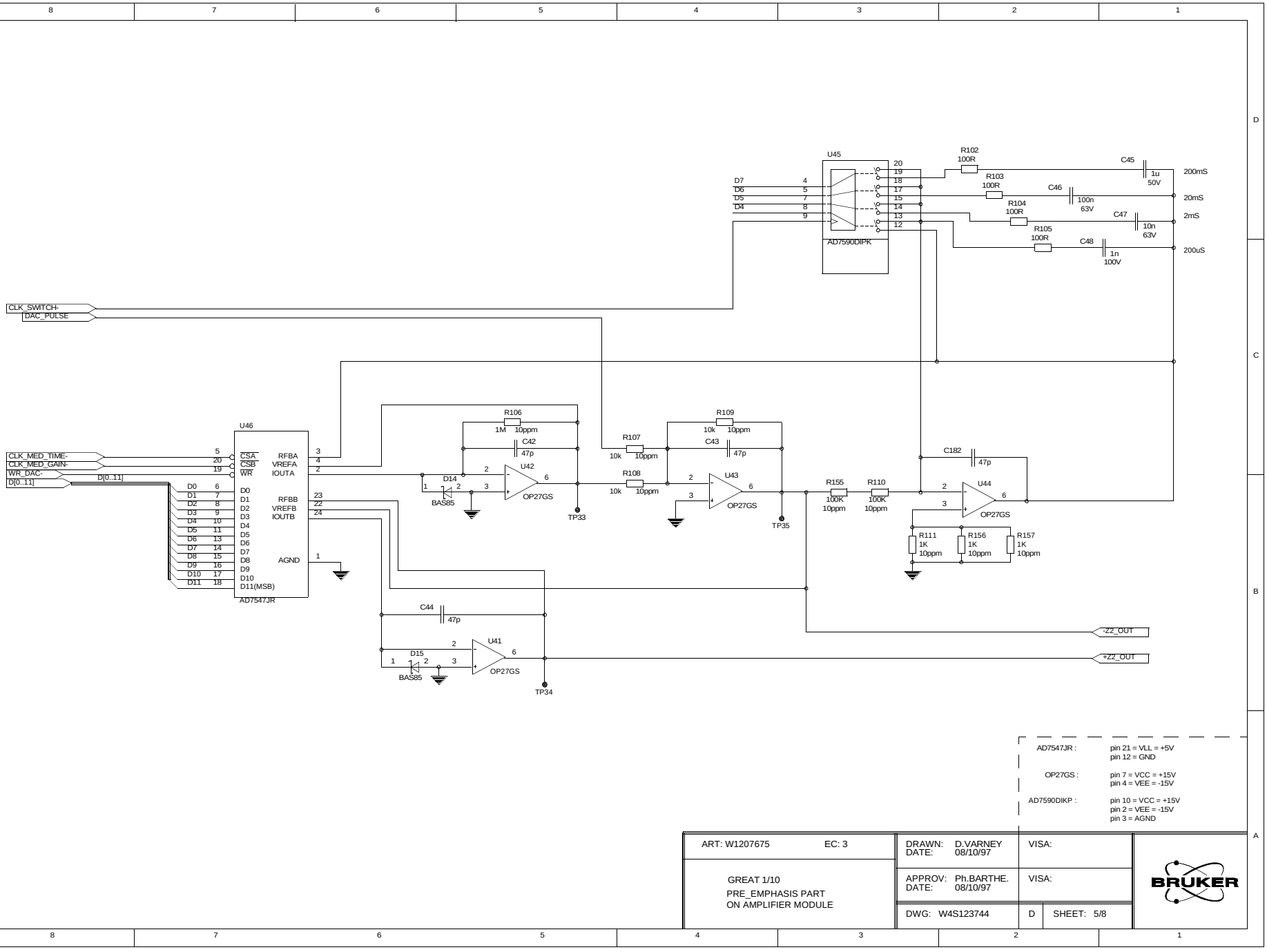


Figure 6.6. GREAT Amplifier Board Schematic page 5 of 8

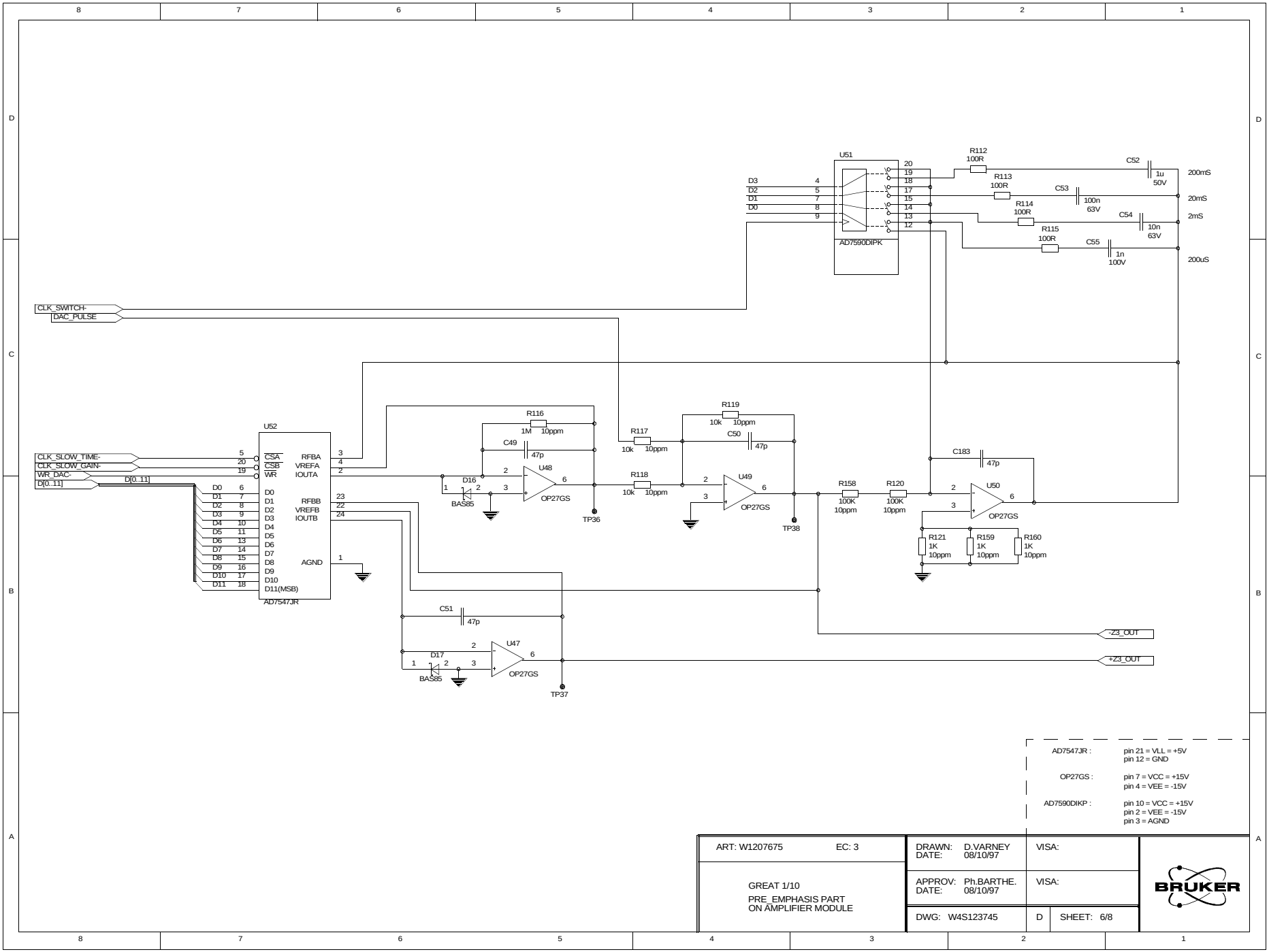


Figure 6.7. GREAT Amplifier Board Schematic page 6 of 8

Figure 6.8. GREAT Amplifier Board Schematic page 7 of 8

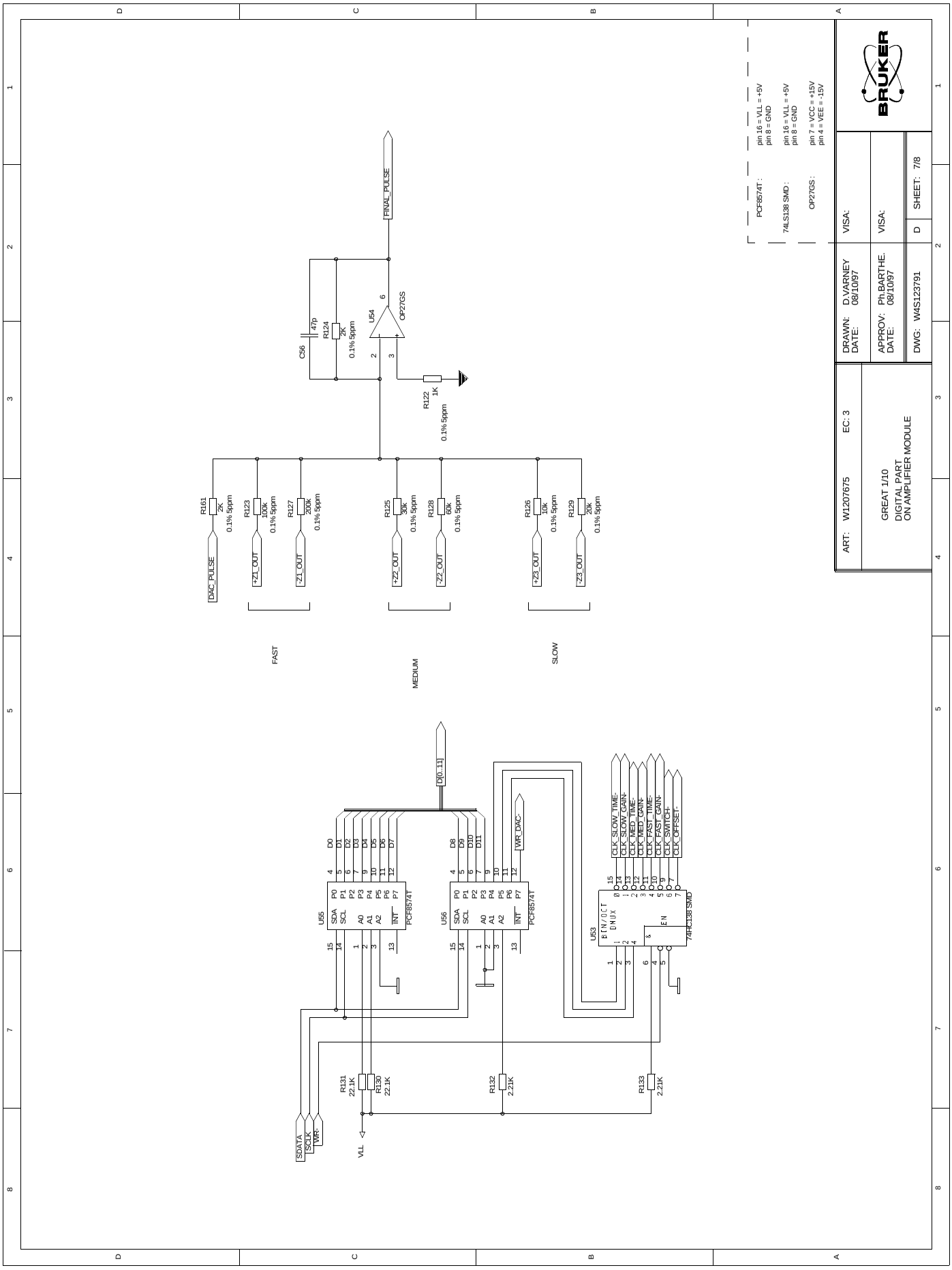
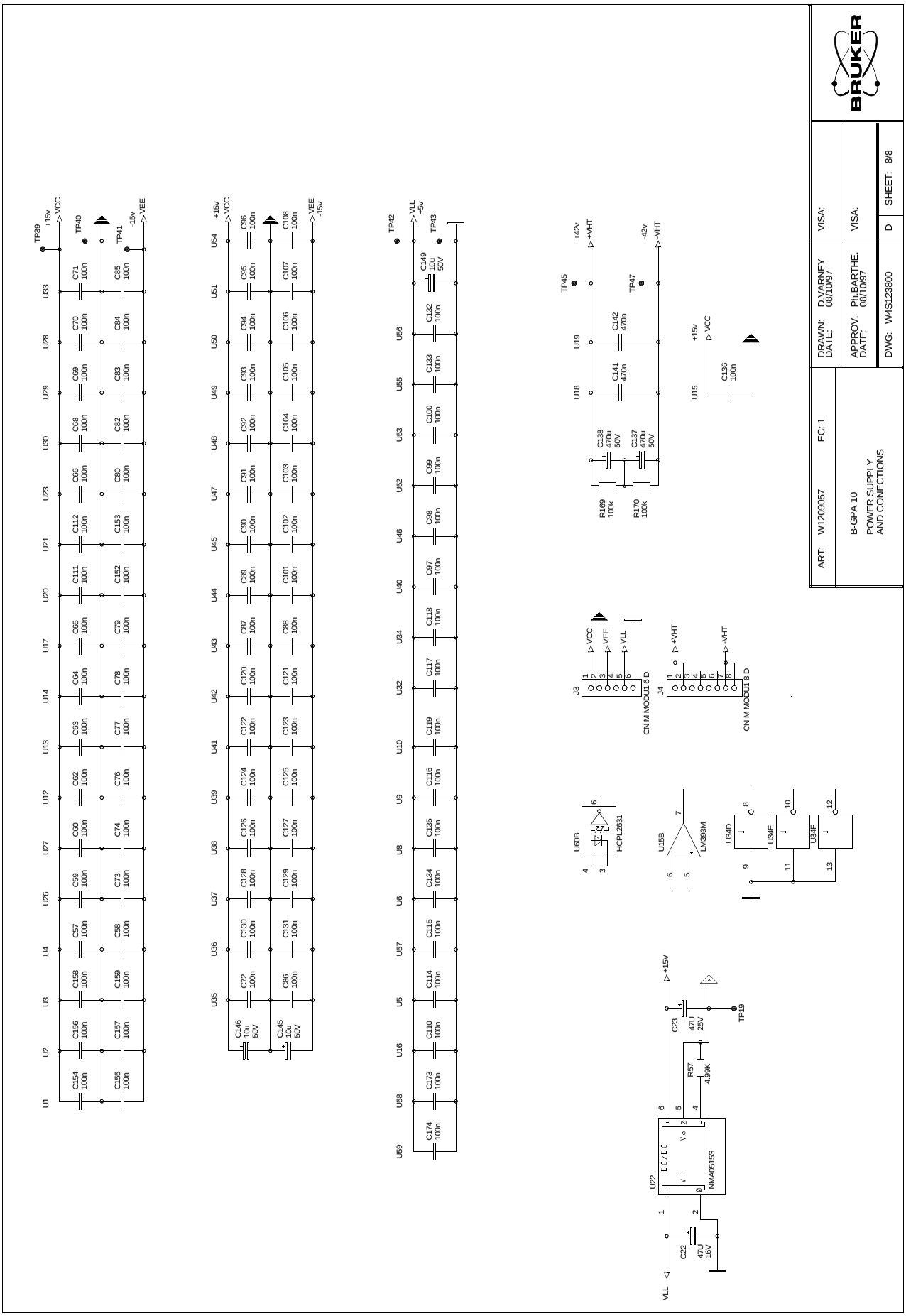


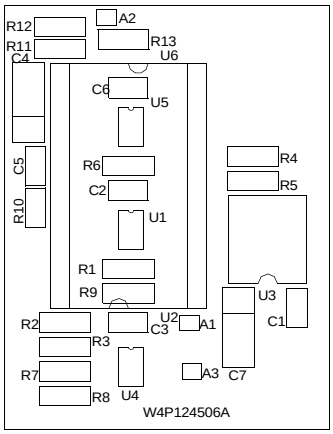
Figure 6.9. GREAT Amplifier Board Schematic page 8 of 8



Piggy Pack board Schematics

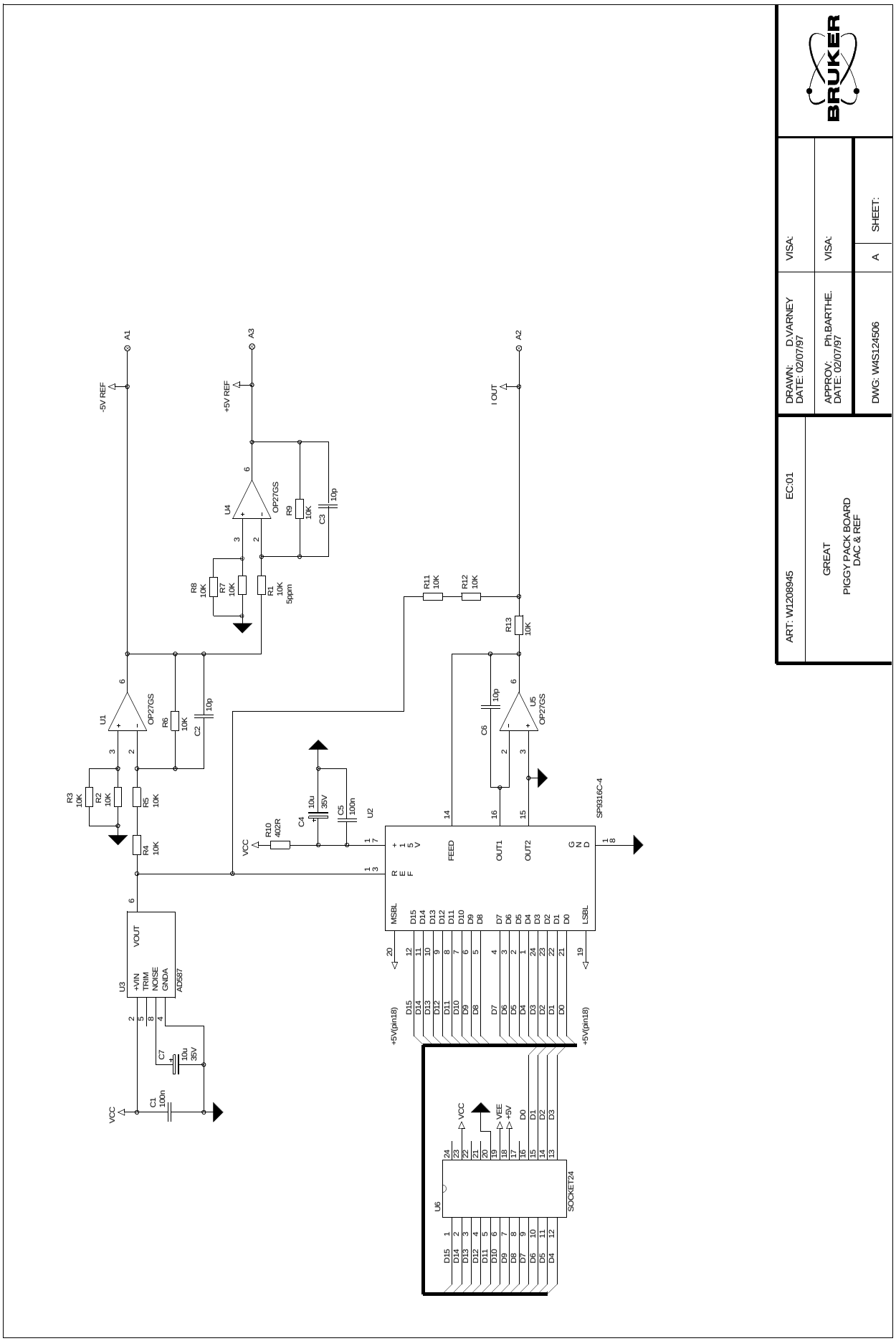
7

Figure 7.1. GREAT Piggy pack board DAC + REF Layout



ART: W1208945 EC:	DRAWN: RC DATE: 23/10/98	VISA:	BRUKER
GREAT 3/10 GREAT DAC 4506 CI : W4P124506A	APPROV: DV DATE: 23/10/96	VISA:	
	DWG: W4L124506	A SHEET: 1/1	

Figure 7.2. GREAT Piggy pack board DAC + REF Schematic

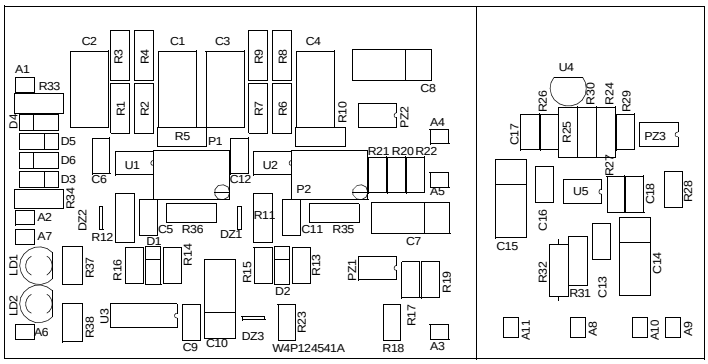


Piggy Pack board Schematics

Auto calibration offset Schematics

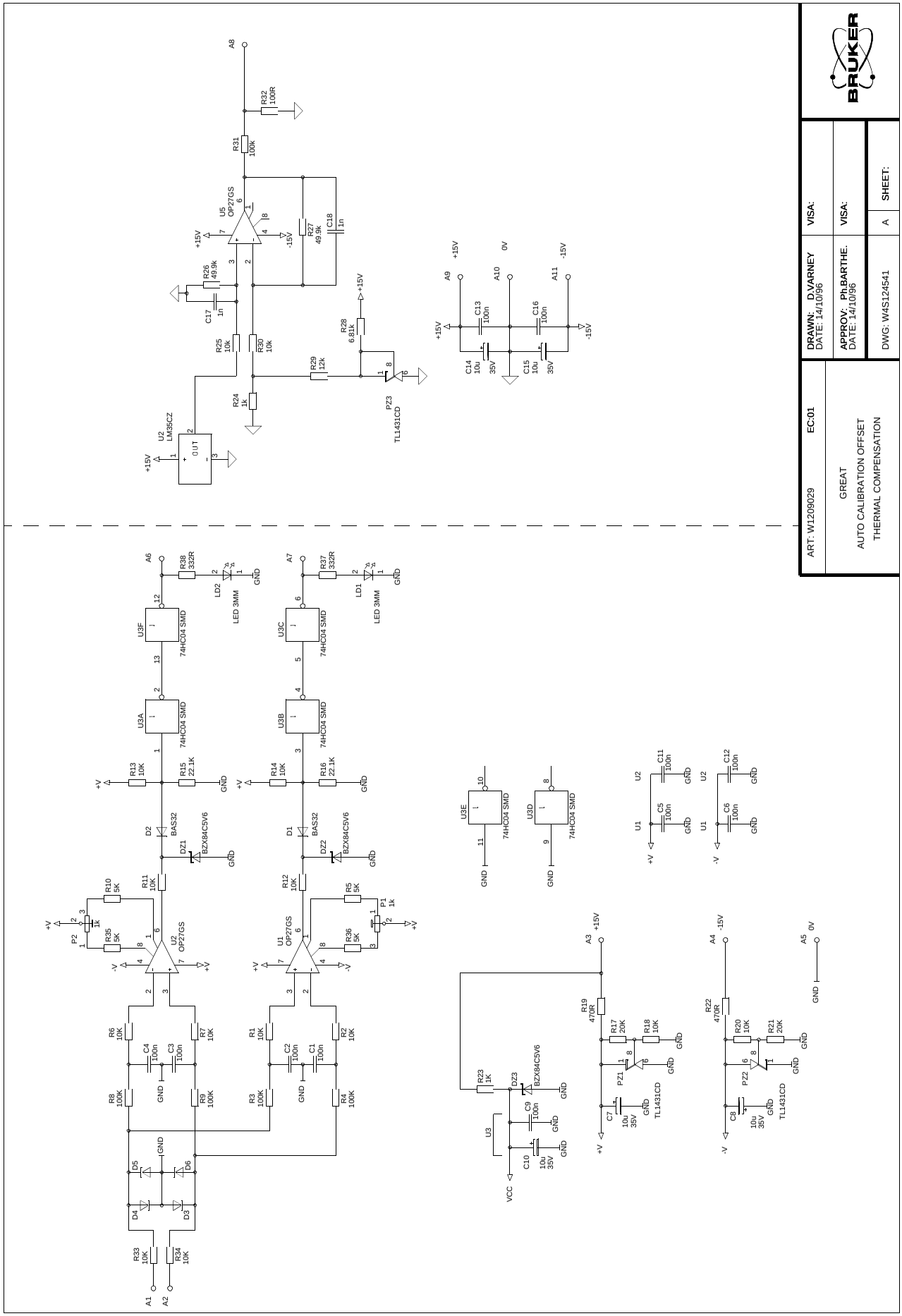
8

Figure 8.1. GREAT Auto calibration offset Layout



ART: W1209029 EC:		DRAWN: RC DATE: 24/10/96	VISA:		
GREAT 3/10 AUTO CALIBRATION OFFSET W4P124541A		APPROV: DV DATE: 24/10/96	VISA:		
		DWG: W4L124541	A	SHEET: 1/1	

Figure 8.2. GREAT Auto calibration offset Schematic



Auto calibration offset Schematics

Figures

Figures

Tables

Tables