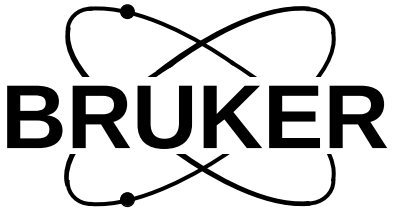

AQR

HADC

Technical Manual

Version 002

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General Description 1

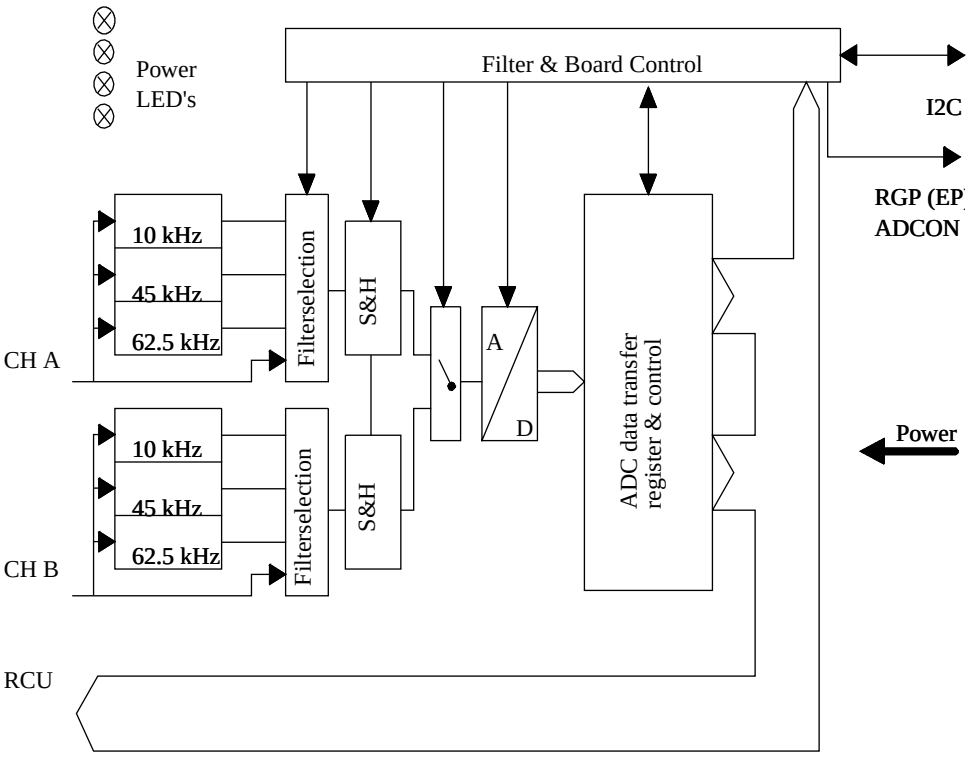
Introduction 1.1

The present analog to digital converter board, called High resolution ADC (HADC), is a 16 Bit system for the whole specified spectral width of 200 kHz. Because of the quadrature detection method in NMR, this system is composed of 2 channels. Each channel has an own anti-aliasing filterbank and Sample & Hold (SHC), but one AD converter, so switching between channel A and B is necessary. The throughput rate for each channel is 200 kSPS (both channels used), resulting in a total of 400 kSPS and allowing oversampling techniques. Therefore only a reduced set of anti-aliasing filters are required. The HADC is very similar to the BRUKER HRD-16.

Functional description 1.2

In the following a short overview of the HADC is given.

Figur 1: Block Diagram HADC



The converter system has two channels (CHA&CHB), which in NMR represent the same FID (Free Induction Decay) signal, one as real (CHA) and one as imaginary (CHB). This is due to the quadrature detection method. Each of these signals pass a four pole Butterworth-filter with cutoff frequencies of 10 kHz, 45 kHz or 62,5 kHz. These filters are used to eliminate noise and to prevent aliasing of signals over the Nyquist frequency. If needed, the possibility exists to bypass the filter in order to install an external filter or to use the filter characteristic of the receiver.

After being filtered, the signal is held by a sample and hold (S&H) circuit, passed through a multiplexer (MUX) and converted by an analog to digital converter (ADC). It converts the analog signal into a digital signal with 16 bits resolution. The full analog signal input range is +/-5V and the throughput rate for each channel is 200 kSPS (in quadrature mode only). The hold command and thereafter the start of the conversion is determined by the rising edge of the Dwell-Clock (DWCLK) from the data acquiring unit (DAU, i.e. RCU Receiver Control Unit). In ‘qsim’ mode the system works in simultaneous quadrature-mode, this means that both channels are holding simultaneously, the ADC is converting channel A first then channel B. In the single-mode or quadrature-off (‘qf’) mode, only channel A converts. The ‘alternating’ mode, also known as ‘sequential’ mode is not possible.

Due to the implementation with one ADC in ‘qsim’ mode the maximal spectral width is 200kHz (total sampling rate is 400kSPS), in ‘qf’ mode the spectral width of 200kHz (sampling rate is 400kSPS) is possible. The digital filters will additionally limit the max. spectral width.

After the conversion stage the data will be latched into a memory (D-flip flop) to remain there until the data can be transferred to the DAU. This transfer overlaps the next conversion started with the next Dwell clock. In fact the data transfer is changed from 32 Bits (2x16 bits) into 4x8 Bits. The first byte is the low byte of channel A, the second byte the high byte of channel A. In quadrature mode the channel B is transferred in the same manner following the channel A data.

For control purposes an I2C bus (Philips) is implemented. Either the DAU or the Receiver (with restriction) can control this bus. Via this bus the HADC can be reseted, the anti-aliasing filter can be selected and the acquisition mode is set. All these settings are coupled to the acquisition software (i.e. in UXNMR FW = filterwidth and AQ_mod = qsim ‘simultaneous acquisition’).

The HADC is located in an rf-cage with access at the front end to the channel A & B inputs, the DAU interface connector and the power led’s. At the rear there is only a connector suitable for the AQR and AQR/P rack (ADC slot). The power is primarly drawn from the AQR rack.

Figur 2: Front view of HADC

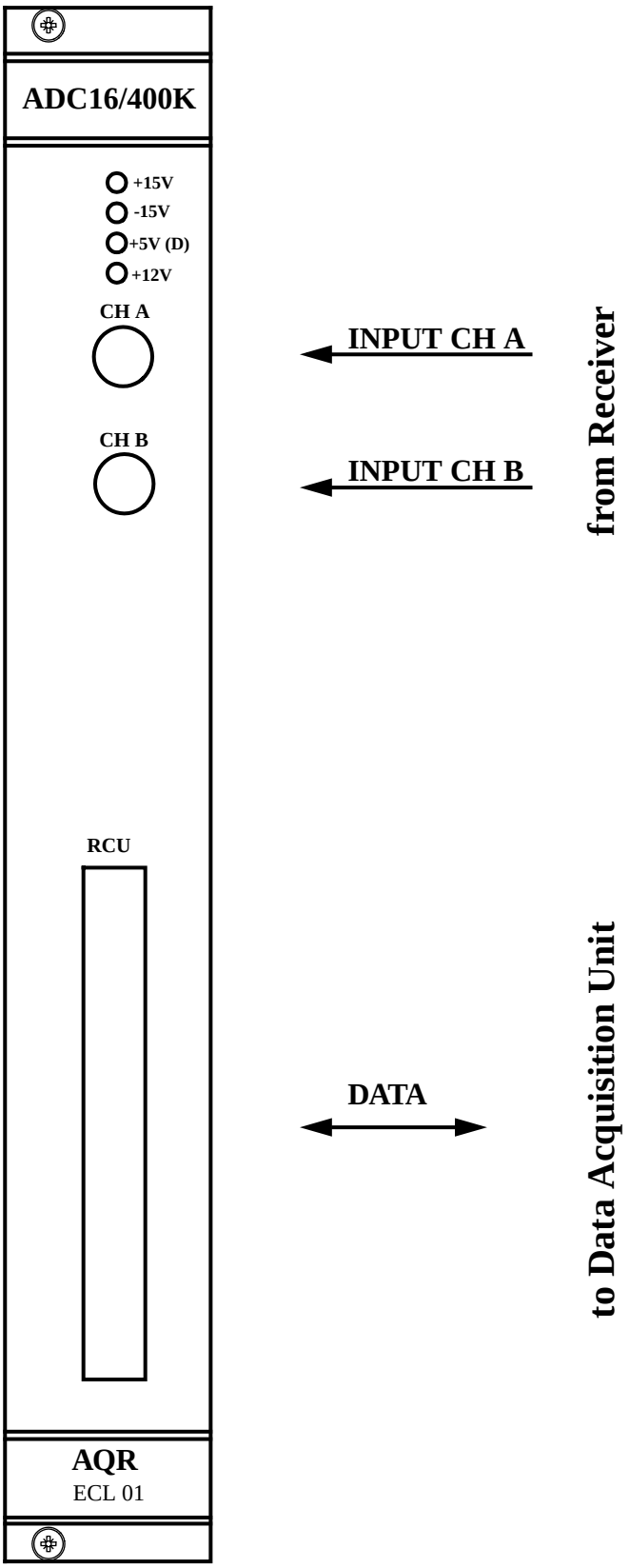


Tabelle 1. DAU-ADC Connector

J1	Signal-Name	J1	Signal-Name	J1	Signal-Name
1	VPWRGND	18	DATA 6~	35	TU0IN
2	VPWRGND	19	DATA 7	36	TU0IN~
3	DATA 0	20	DATA 7~	37	XVDD 12
4	DATA 0~	21	VPWRGND	38	XVDD 12
5	DATA1	22	VPWRGND	39	DWCLKIN
6	DATA 1~	23	DST 1	40	DWCLKIN~
7	DATA 2	24	DST 1~	41	VPWRGND
8	DATA 2~	25	UNIT 0	42	VPWRGND
9	DATA 3	26	UNIT 0~	43	ADC IN
10	DATA 3~	27	SRT 1	44	
11	XVDD 12	28	SRT 1~	45	SDATA IN
12	XVDD 12	29	RES RT	46	SDATA IN~
13	DATA 4	30	RES RT~	47	SERCLK
14	DATA 4~	31	XVDD 12	48	SERCLK~
15	DATA 5	32	XVDD 12	49	SERDIR
16	DATA 5~	33	EP IN	50	SERDIR~
17	DATA 6	34	EP IN~		

Tabelle 2. AQR-ADC Connector

J 6	A	B	C
1			
2			
3			
4			
5			
6	SDA 1		SCL 1
7	SDIR 1		I2C GND
8	ADC ON	ADC ON GND	EP~
9			EPGND
10	RX +9V	RX +9V	RX +9V
11	DGND	DGND	DGND
12			
13			
14	XP 19V	XP 19V	XP 19V
15	PWGND	PWGND	PWGND
16	XM 19V	XM 19V	XM 19V

Power supply 1.4

The power supply is derived from +/- 19V for the analog section and from +/- 9V for the digital section. Analog and digital voltages are generated on-board. The analog voltages are +/- 15V and +/- 5V. The digital voltage is +5V. The digital power supply is divided into two parts, the reason being the galvanic isolation stage between the DAU and the ADC.

In fact the board has six different voltages of which four are shown at the front of the ADC. The +/- 5V which are not shown, are derived from +/- 15V (both analog voltages).

Troubleshooting 2

General 2.1

Before starting to check the system, it should be mentioned, that the board has been thoroughly checked for malfunction or wrong assembly at the factory. For this reason it is prohibited to change or remove components. The board should be sent to the factory for all modifications. The ADC board should only be opened by service personnel.

No LED is lighting 2.2

If no light-emitting diode (LED) is lighting, check if power is present at the AQR and if the DAU connector is connected.

Check all voltages at their respective testpoints:

1. +/-15V analog to AGND1
2. +/-5V analog to AGND1
3. +5V (VCC) digital to DGND
4. +5V (VPWR_P) digital to VPWRGND
   (supplied from the DAU, derived from +12V).

No signal / No conversion 2.3

Check if the cables of CH A and CH B are connected to the receiver.

Start a reset procedure via the acquisition software (i.e. ‘ii’ = initialize interface) or switch power off and on again, in order to start a new power up sequence.

Check for correct jumper settings:

ECL01: JU1,JU4,JU7-JU12

ECL02: JU1,JU4,JU10-JU12

Tabelle 3. DC specification

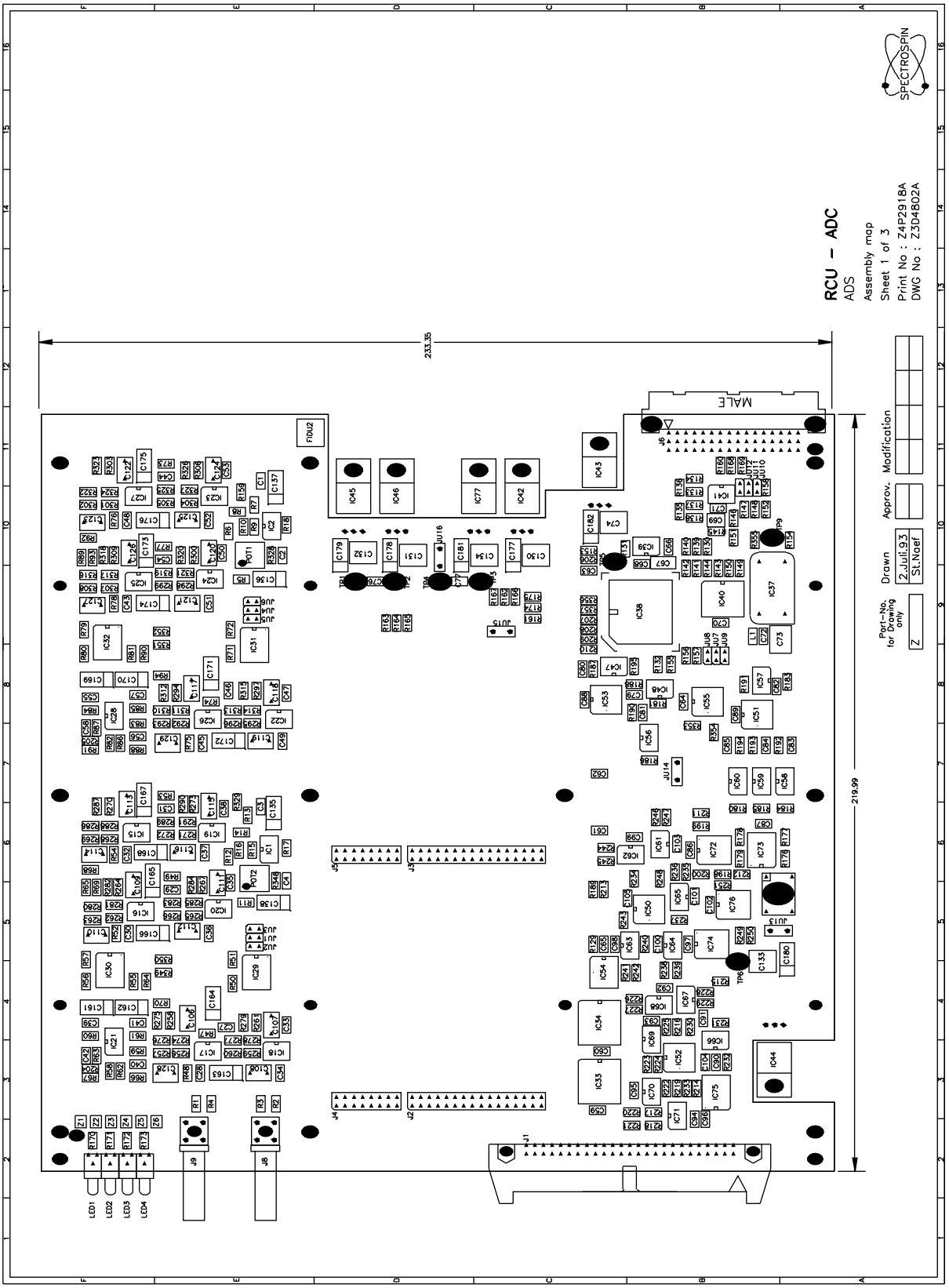
Parameter Conditions	min.	typ	max	Units
Supply current (+19V)		350		mA
Supply current (-19V)		200		mA
Supply current (+9V)		150		mA
Supply current (+12V)		480		mA

Tabelle 4. System specification

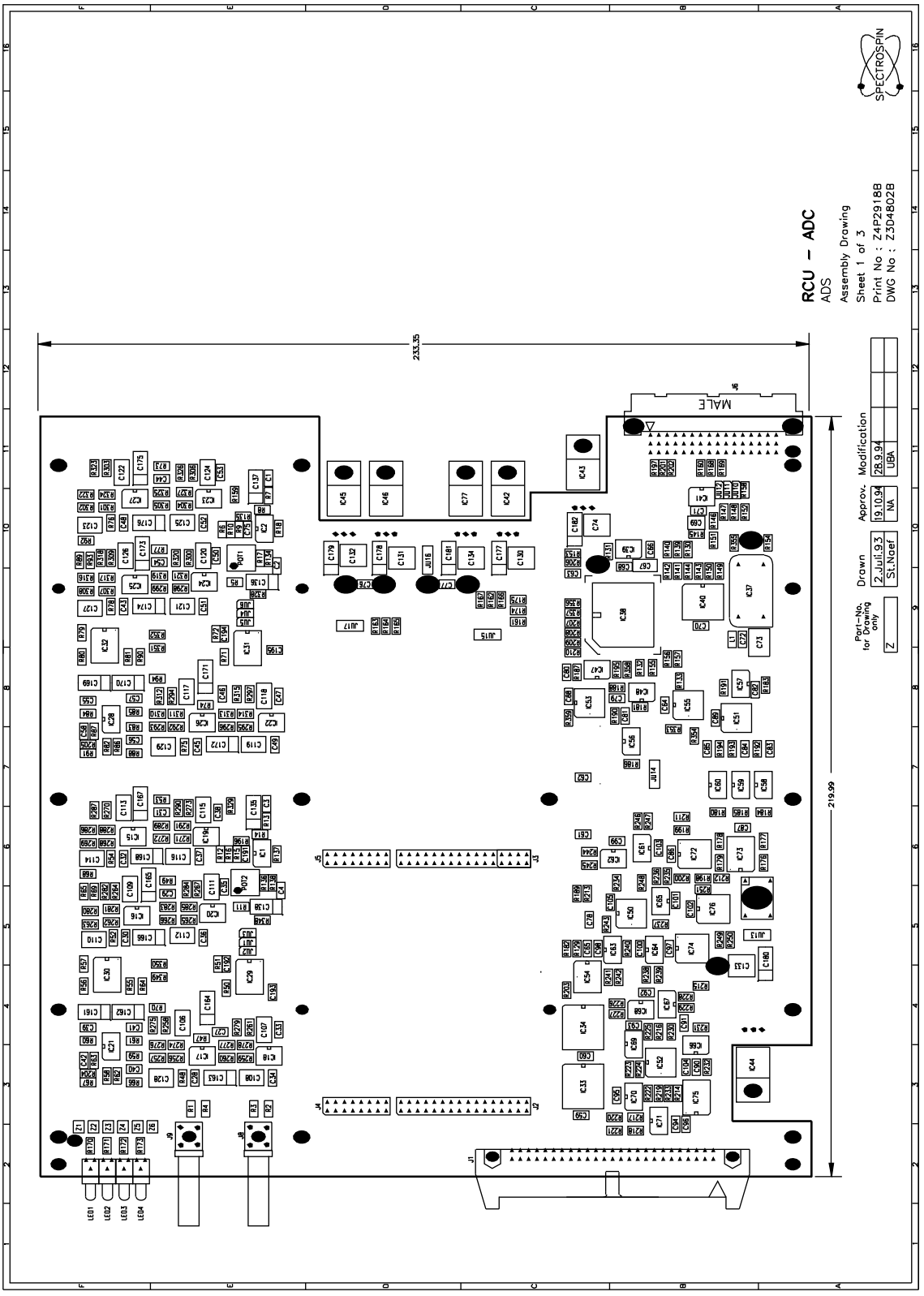
Parameter Conditions	min.	typ	max	Units
Resolution			16	Bits
No Missing Codes			16	Bits
Integral Nonlinearity ADC		+/-0.0012	+/- 0.003	% FSR
Noise		120		µV rms
Spectral Noise (Size 8k / sampling rate 400kSPS)		-120		dB
Signal to (Noise + Distortion) Ratio (10Vpp / 1 kHz)	92			dB
Total Harmonic Distortion (10Vpp / 1 kHz)		-98	-92	dB
Peak Harmonic or Spurious Noise (10Vpp / 1 kHz)		-96	-92	dB
Conversion Time per channel			1,5	µs
Acquisition Time per channel		200		ns
Throughput Rate for each channel (overlap between conversion and acquisition)			200	kSPS
Analog Input Voltage Range			+/- 5	V
Crosstalk CH A: 10 Vpp @ f < 50kHz CH B input shorted		100		dB

Assembly map HADC 3.1

Figur 3: Assembly map HADC ECL01 basic board

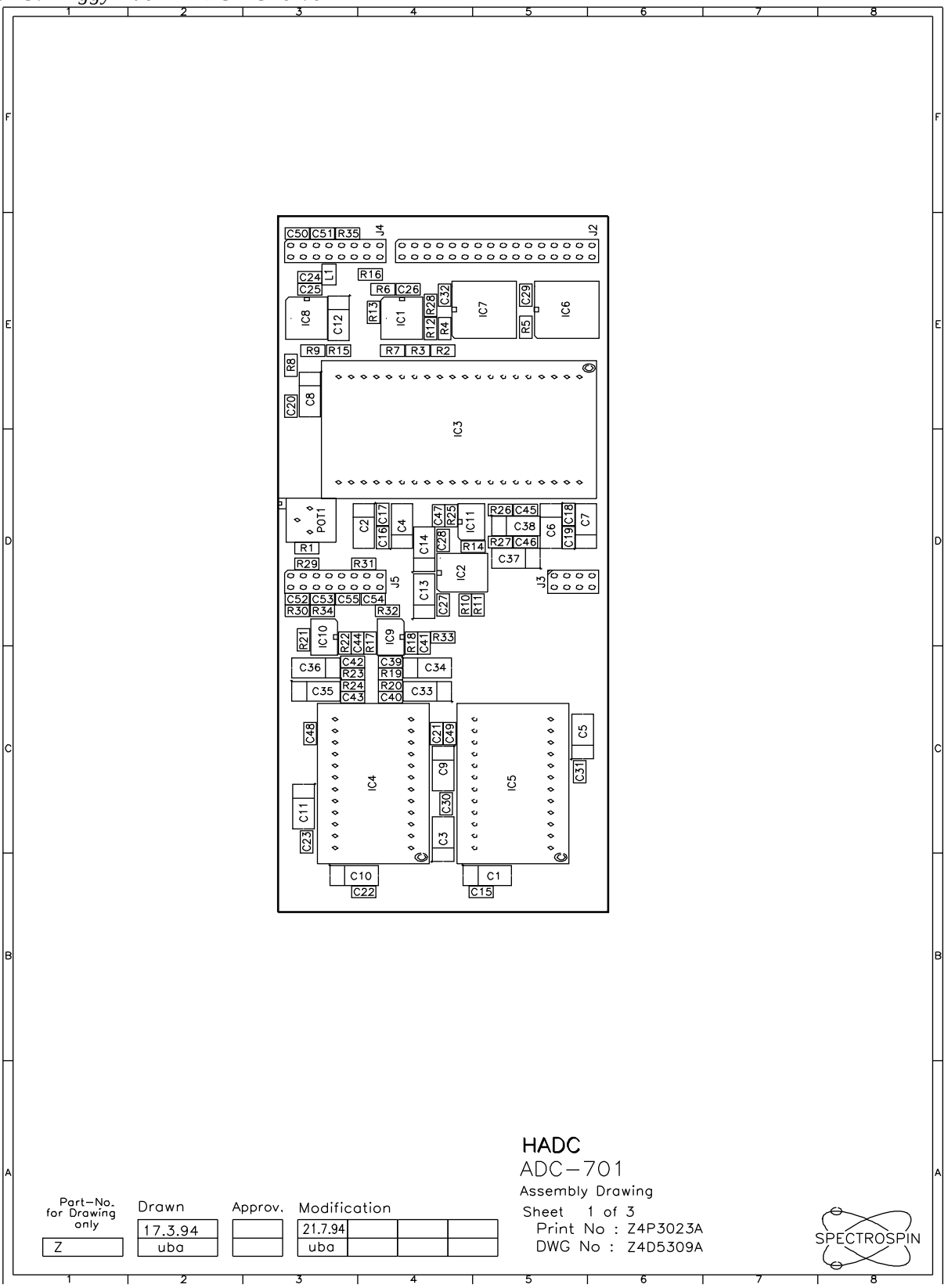


Figur 4: Assembly map HADC ECL02 basic board



Attention: The assembly map may not be consistent with the implementation, because of second source component evaluation and varied use of the board (see HADC).

Figur 5: Piggy Back HADC ECL01/02



Attention: The assembly map may not be consistent with the implementation, because of second source component evaluation and varied use of the board (see SADC).

A

ADC 4
ADC slot 4
analog voltages 7
AQR 4

B

Butterworth 3

C

cutoff frequencies 3

D

Data Acquiring Unit 4
DAU 4
digital voltage 7

E

external filter 3

F

FID 3
FID (Free Induction Decay) 3

H

HRD-16 3

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I2C bus 4

M

multiplexer 4

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sample and hold 4
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