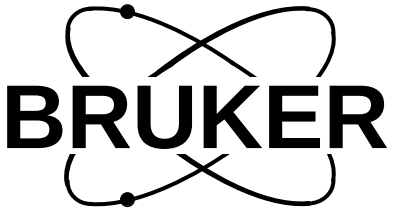

Frequency System

SE451-3CH

Technical Manual

Version 004

BRUKER

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Updated for BASH 2.0 by U. Roos - December 1996

P/N: Z31243
DWG-Nr.: 914 004

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SE451 3-CHANNEL

Features 1.1

- Wideband transmit-receive unit
- SE451 high frequency housing with 5 slots
- 3 broadband transmitter RF-channels
- 3 channel observe capability
- 3 channel 4 Phase Modulator (optional)

General Description 1.2

The 3 channel SE451 consists of three transmitter boards (TF1, TF2 and TF3, or TFX, TFH and TFY), a local oscillator unit (generating signals for frequency synthesis in the transmitter boards) and a receiver. These five boards are plugged onto a motherboard which provides power supply lines and distributes logic signals from the front pannel connectors via a PAL to the individual units. On the motherboard a SP3T-RF-switch selects the local oscillator signal of the observed channel.

Block Diagram 1.3

The following block diagram gives overall information about the 3 channel SE451 unit and its frequency generation principle.

Figure 1: SE451-3CH frequency generation and block diagram

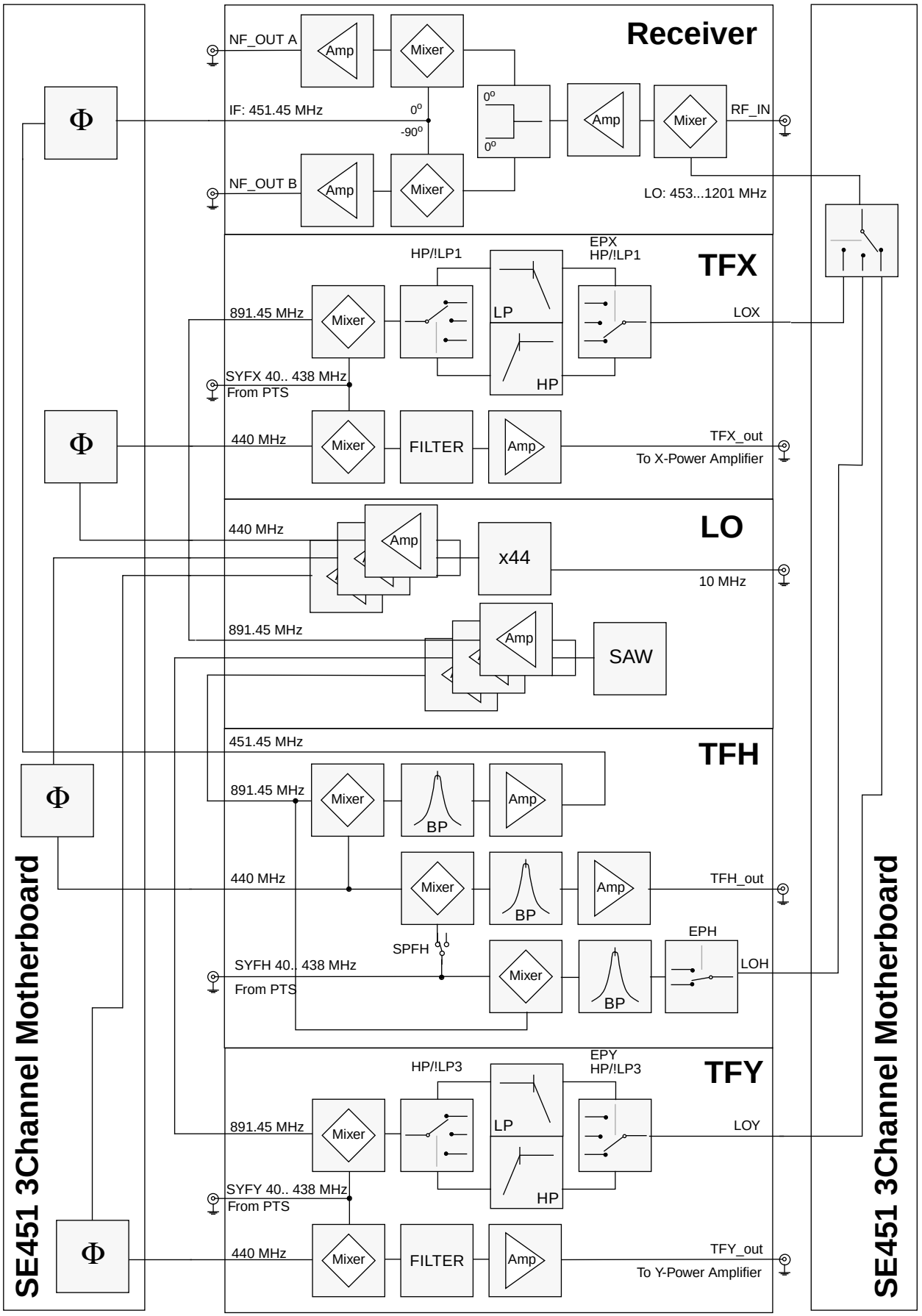
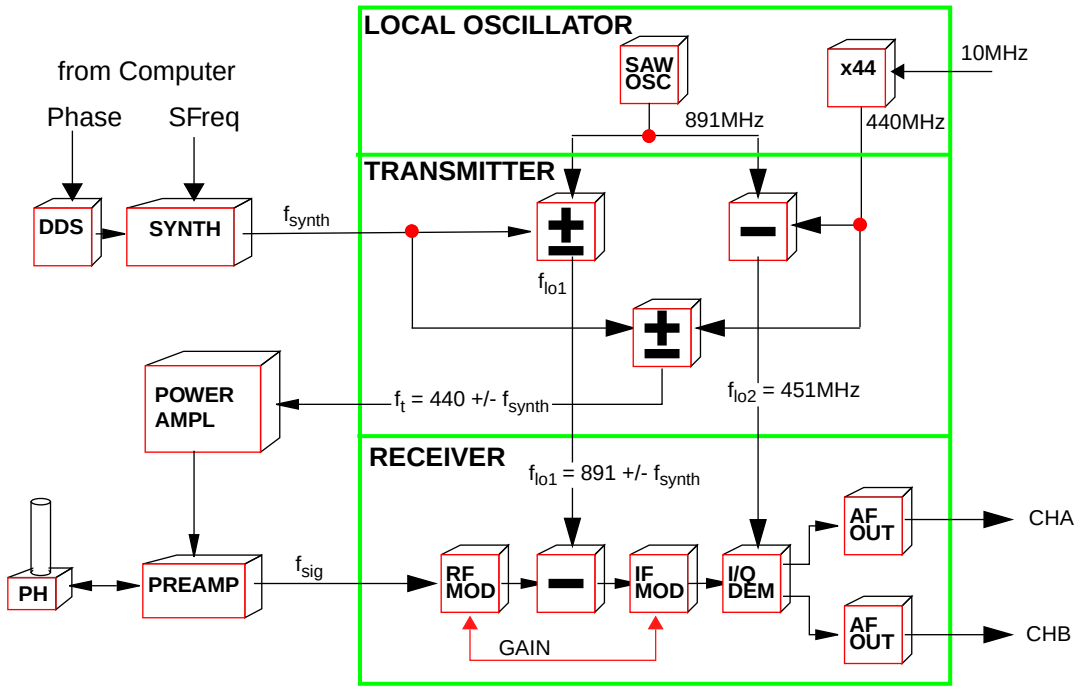


Figure 2: Function diagram SE451



Receiver Gain 1.4

The most used parameter which is set by the operator is the receiver gain. The following description gives information about the receiver gain.

Receiver Gain calculation 1.4.1

The receiver gain (voltage gain) can be set within a range of 12dB to 102dB. The operator is used to set a linear gain via the UXNMR. The following equation describes the relationship of the 'UXNMR-Gain' and the logarithmic voltage gain (between input RF_IN and the audio outputs CHA and CHB) of the SE451 receiver.

$$Gain_{UXNMR} = 10^{\left(\frac{Gain_{RFT} - 12}{20}\right)}$$

$$Gain_{RFT}[dB] = 20\log(Gain_{UXNMR}) + 12dB$$

Receiver Gain Table 1.4.2

In the SE451 receiver the gain can be set in steps of 6dB. The following table lists the different gains and the according control signals

Tabelle 1. Gain Table for 6dB Steps SE451-3CH

RG	RG UXNMR	RG [dB]	DRG0 (RG6)	DRG1 (IF0)	DRG2 (AGC_A)	DRG3 (AGC_B)	DRG4 (RF_A)	DRG5 (RF_B)
1	1	12	0	1	0	0	0	0
2	2	18	1	1	0	0	0	0
4	4	24	0	1	0	0	1	0
8	8	30	1	1	0	0	1	0
16	16	36	0	1	0	0	0	1
32	32	42	1	1	0	0	0	1
64	64	48	0	1	0	0	1	1
128	128	54	1	1	0	0	1	1
256	256	60	0	0	0	0	1	1
512	512	66	1	0	0	0	1	1
1k	1024	72	0	0	1	0	1	1
2k	2048	78	1	0	1	0	1	1
4k	4096	84	0	0	0	1	1	1
8k	8192	90	1	0	0	1	1	1
16k	16384	96	0	0	1	1	1	1
32k	32768	102	1	0	1	1	1	1

General 2.1

This chapter describes the Burndy connectors, theRF-SMA and RF-BNC connectors and the Sub-D connector on the front panel of the SE451-3CH.

Burndy1 connector (SE451 Control) 2.2

Burndy1 is used as general purpose connector (SE451 Control), where all control- , pulse - and power supply- signal are wired. Pins B, C, F, H, L, M, R, S, V, W, Z, AA, DD, JJ, NN are coaxial RF-wires with female connectors whereas pins A, D, E, J, K, N, P, T, U, X, Y, BB, CC, FF, HH, LL and MM are DC-wires with male connectors.

Figure 3: Burndy1: SE451-3CH control connector

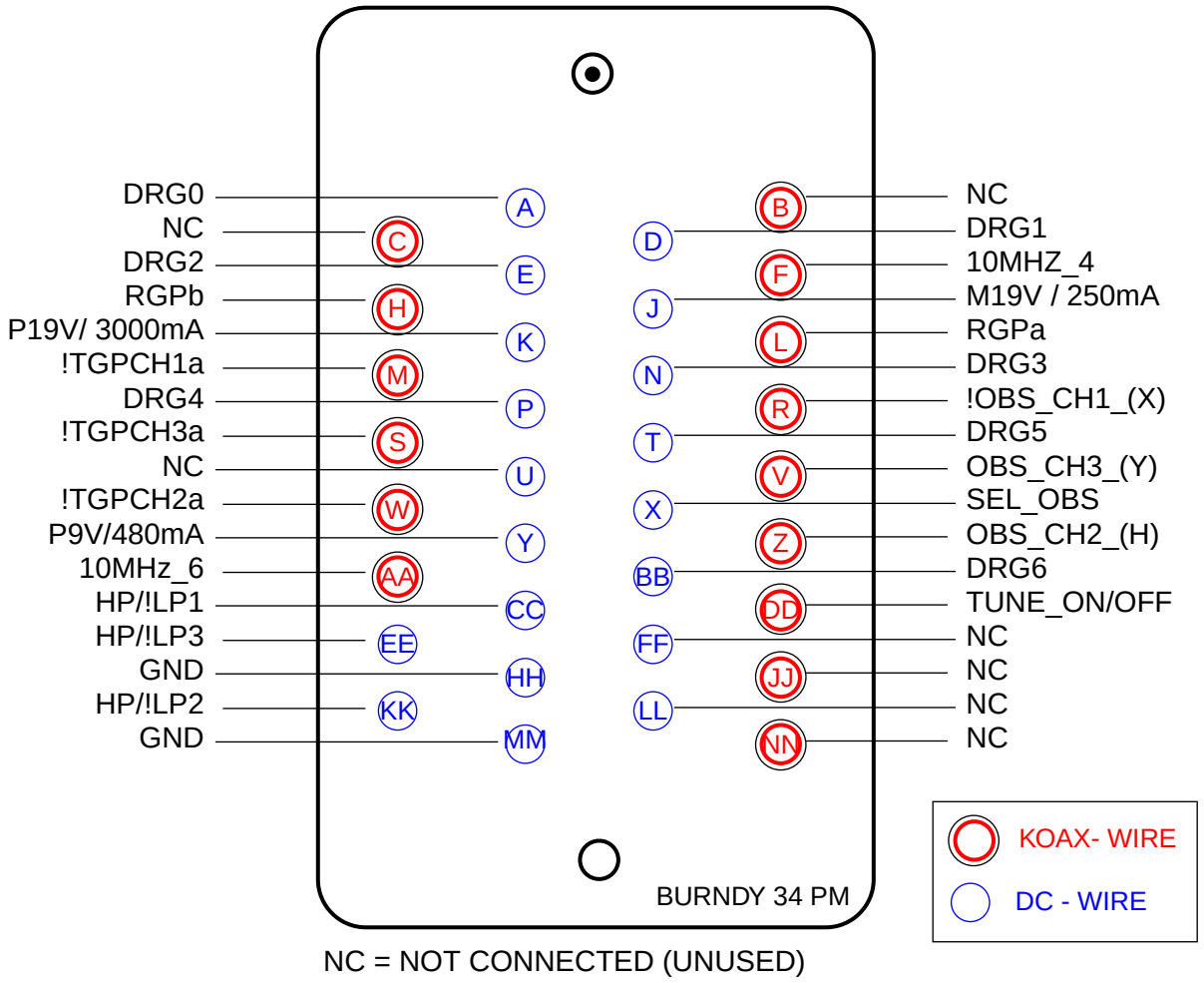


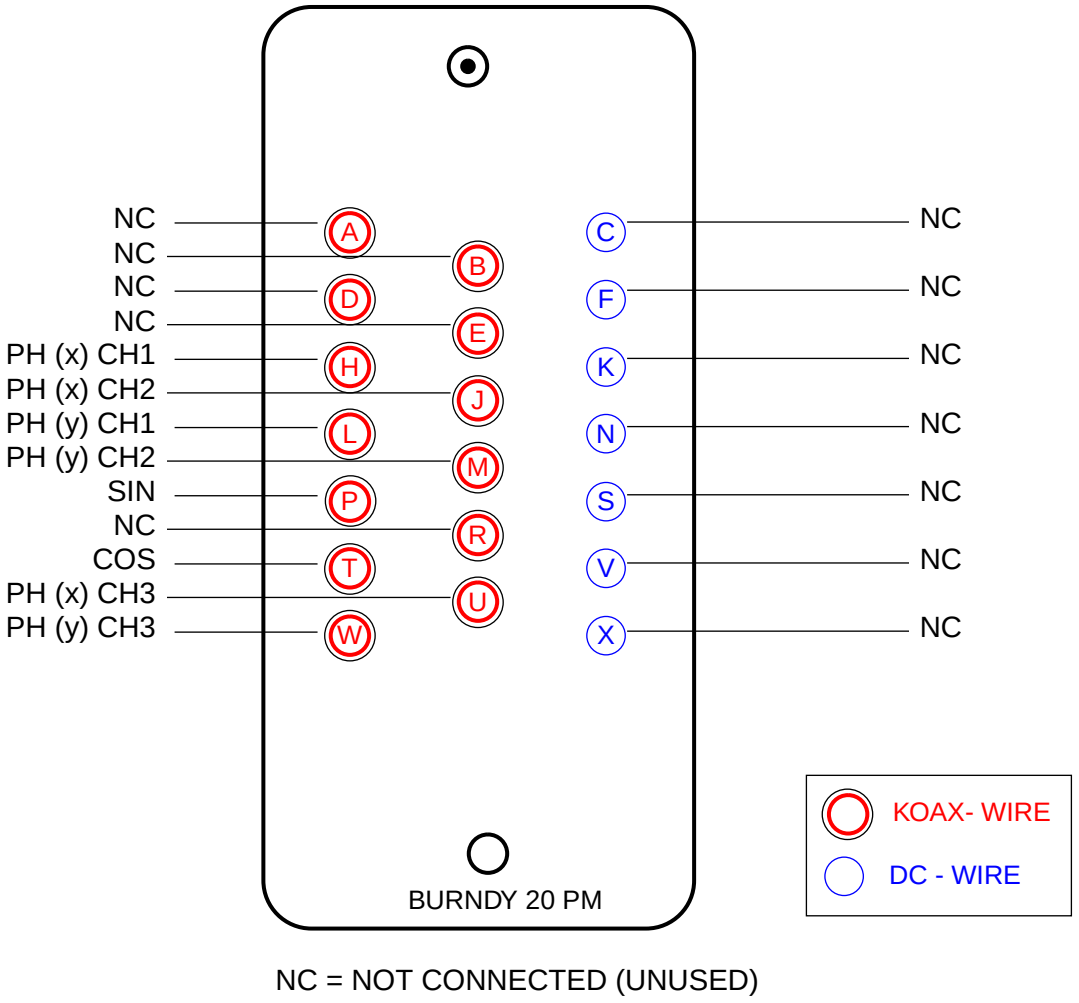
Tabelle 2. Burndy1 signal description

Signal name	signal description
DRG0 - DRG6 (RG6, IF0, AGC_A, AGC_B, RF_A, RF_B, RES(TP9))	Signals controlling the receiver gain, in brackets signal names of earlier SE451 2channel units.
RGPa, RGPb	Receiver gating pulse A (RGPA) and B (RGPB)
!TGPCH1a, !TGPCH2a, !TGPCH3a	Transmitter gating pulse signals of channel 1, 2 and 3, low activ
HP/!LP1, HP/!LP2, HP/!LP3	Highpass/Lowpass control lines for transmitter channels 1, 2 and 3.
!OBS_CH1_(X), !OBS_CH2_(H), !OBS_CH3_(Y)	These signals determine the observe channel and select the appropriate local oscillator reference signal.
10MHz_4, 10MHz_7	10 MHz OUTPUTs from the LO-Board.
SEL_OBS	Select observe signal (also called reverse signal), used only for compatibility to earlier SE451 2 channel units when using the Y-cable as interface and setting the PAL-jumpers on the motherboard accordingly. SEL_OBS is connected to OBSERVE_H~ on the SE451 3channel motherboard. SEL_OBS high selects the X-channel, SEL_OBS low the H-channel as observe-channel.

Burndy2 connector (4Phase Modulator Control) 2.3

Burndy2 wires all control signals for the 4Phase-Modulator which is located on the SE451-3Channel motherboard. All connected pins are RF-coaxial wires with male connectors.

Figure 4: Burndy2: 4 Phase Modulator Control Connector

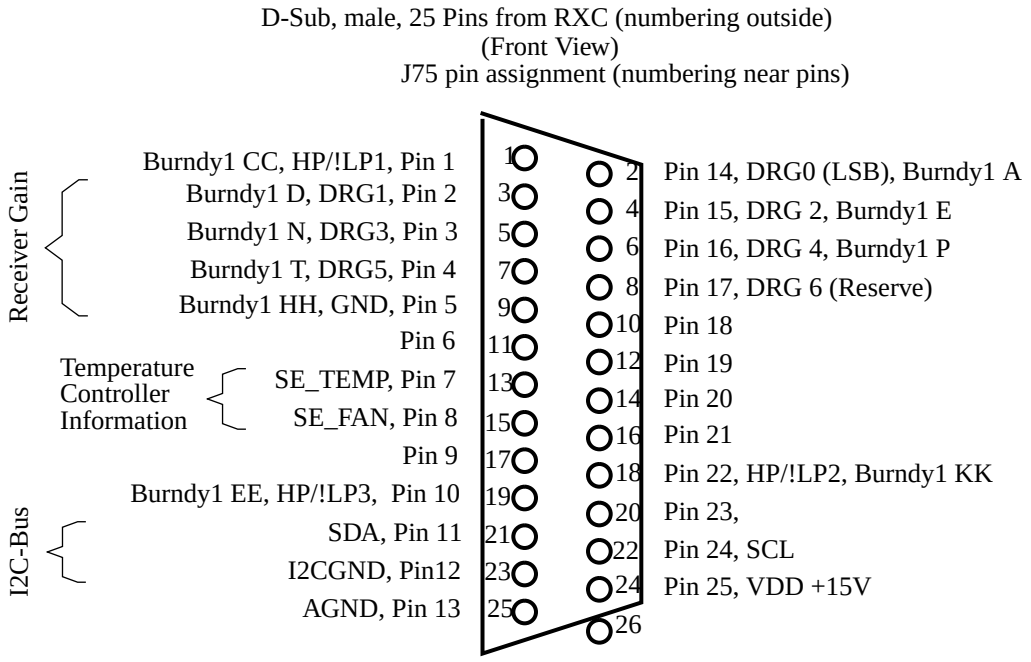


NC = NOT CONNECTED (UNUSED)

25 Sub-D Connector (male, RXC-Control) 2.4

The following diagram shows the pin assignment of the 25 Sub-D RXC-Control connector on the SE451-3CH front pannel. The pin numbers at the outside correspond to the Sub-D numbering scheme, the numbers near the pins are according to the pin assignment of connector J75 (surface mounted 26 pin connector) on the SE451-3CH motherboard. Note that pin 26 of connector J75 is not wired to the RXC-Control Sub-D front pannel connector. The signals for gain-setting (DRG0 to DRG6) and the filter selection signals (HP/!LPx) are wired on Burndy1 connector as well. The according pin assignment is also given in the table below.

Figure 5: RXC Control 25 Sub-D Connector Pin Assignment



SMA and BNC connectors 2.5

On the front pannel the following signals have SMA or BNC connectors:

Tabelle 3. SMA connectors on the front pannel of the SE451-3CH

signal name	signal description
Synth_F1	(PTS-) synthesizer input for channel X (channel 1)
F1_out	X- (1-) transmitter output (to power amplifier)
Synth_F2	(PTS-) synthesizer input for channel H (channel 2)
F2_out	H- (2-) transmitter output (to power amplifier)
Synth_F3	(PTS-) synthesizer input for channel Y (channel 3)
F3_out	Y- (3-) transmitter output (to power amplifier)
10MHz_In	10MHz Input
CHA	NF output, channel A
CHB	NF output, channel B
CHA_BB	Broadband, 50Ohm NF-Output, Channel A
CHB_BB	Boradband, 50Ohm NF-Output, Channel B

Tabelle 4. BNC connectors on the front pannel of the SE451-3CH

signal name	signal description
RF_IN	RF Input from preamplifier
Tune_Out	Tuning output for wobbling

Alternativ signal names 2.6

For compatibility reasons to older SE451-versions and for test purposes on the motherboard of the SE451-3CH alternativ signal names (corresponding to older units) have been used on the screen printing. These names are given in the following table:

Tabelle 5. Alternativ signal names used on the screen printing of the SE451-3CH motherboard

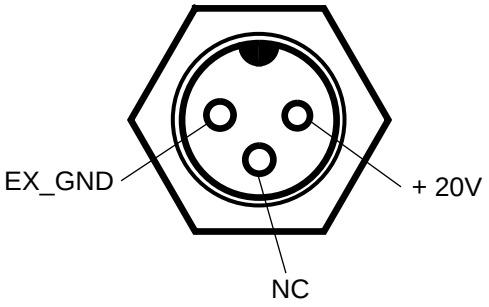
signal name	2nd name	Burndy1 Pin	25 Sub-D Pin	Module Connector Pin	J75 Pin Assignment
DRG0	RG6	A	14	J1 2A	2
DRG1	IF0	D	2	J1 3C	3
DRG2	AGC_A	E	15	J1 4D	4
DRG3	AGC_B	N	3	J1 5E	5
DRG4	RF_A	P	16	J1 6F	6
DRG5	RF_B	T	4	J1 7H	7
DRG6	RES (TP9)	BB	17	-	8
HP/!LP1	FILTER_X	CC	1	J2 2B	1
HP/!LP2	FILTER_H	KK	22	J4 2B	18
HP/!LP3	FILTER_Y	EE	10	J5 2B	19
SEL_OBS	REVERSE	X	-	-	-

ext. Fan Supply connector 2.7

The built in fan with and its temperature controller board are supllied by an external source. The ext. supply connector is located at the back of the SE451 housing.

The pin assignement is as follows:

Figure 6: ext. supply connector pin assignment



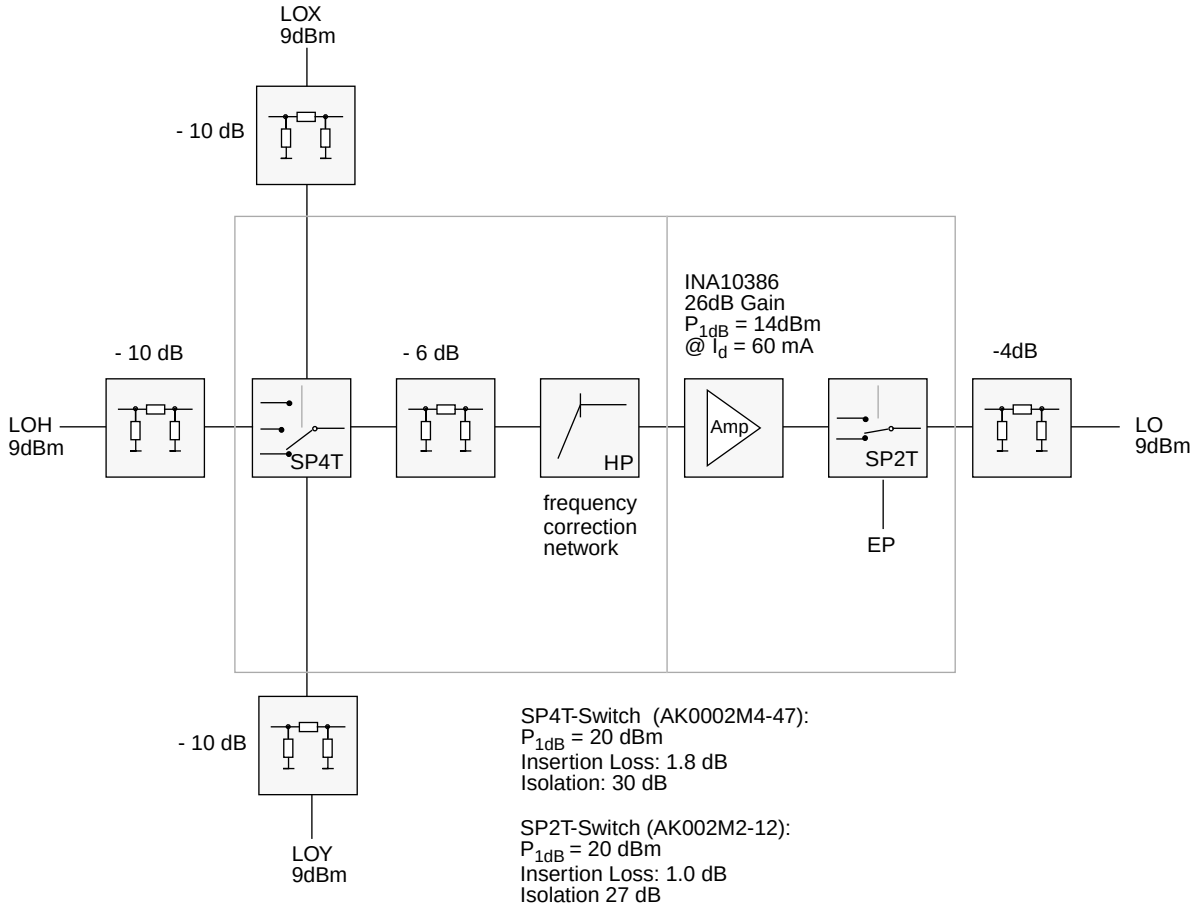
General 3.1

On the motherboard all the signals of the different modules and the front pannel connectors are routed. A PAL provides the possibility to adjust gating pulses to different console wirings via jumpers (see the chapter about the PAL in this manual). As well on the motherboard a SP3T RF-switch routes the three local oscillator signals which determine the observed channel. A block diagram of this small RF circuit can be found in the next paragraph. For units with 4Phase Modulator the phase shifters are implemented on the motherboard as well

Block diagram LO-switch 3.2

To provide good isolation between the three local oscillator signals and the output (as well as good cross isolation between the three LO-signals themselves) and for a good matching attenuators have been placed at the inputs and the output of the SP3T switch. A frequency correction network provides a flat insertion loss/gain characteristic over the range of 400MHz to 1200MHz.

Figure 7: Block diagram of the LO-Switch on the SE451-3CH motherboard Z4P2997



PAL Equations

4

General 4.1

This chapter describes the equations used in the PAL (IC7, EP910PLCC) on the SE451-3CH motherboard. The following mnemotechnics were used:

NOBL: New Observe Logic

NEPL: New EP (Empfangspuls=Receiver Pulse) Logic

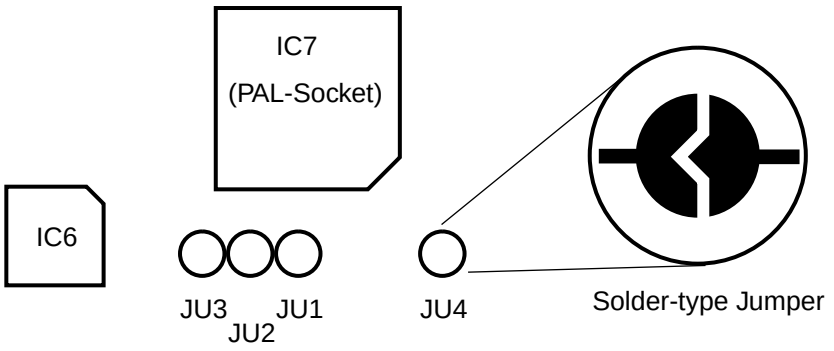
INVEP: Inverted EP

INVTGP: Inverted TGP (Transmitter Gating Pulse)

Jumpers 4.2

The 3-Channel SE451 can be configurated for high activ control signals (old mode) or low active control signals (new mode). There are 4 solder-type jumpers (JU1 ... JU4) located just below the PAL-socket on the motherboard.

Figure 8: Location of the jumpers JU1 ... JU4



Factory configuration 4.2.1

All 3-CH SE451 are factory configurated for low active control signals (unless specific ordered).

Tabelle 6. Jumper settings (factory configuration):

Jumper	Setting	Description
JU1	open	Low active transmitter gating pulses (!TGPCH1a, !TGPCH2a and !TGPCH3a)
JU2	open	Low active receiver gating pulses (RGPa and RGPb)
JU3	open	Transmitter and receiver switched by one pulse only (RGPa)
JU4	open	Observe channel selected by three separat signals !OBS_CH1_(X), !OBS_CH2_(H) and !OBS_CH3_(Y)

Jumper settings for other configurations 4.2.2

If the SE451 3-CH unit is used as a replacement for an older 2-CH unit the jumpers have to be set as follows:

Tabelle 7. Jumper settings for replaced 2-CH units:

Jumper	Setting	Description
JU1	closed	High active transmitter gating pulses (!TGPCH1a, !TGPCH2a and !TGPCH3a)
JU2	closed	High active receiver gating pulses (RGPa and RGPb)
JU3	closed	Transmitter and receiver switched by two different pulses: RGPa => EP, RGPb => EPX, EPH
JU4	closed	Observe channel selected by one signal only: SEL_OBS high = H, SEL_OBS low = X

Modification for OBS-SEL logic:

The SEL_OBS signal used in this configuration is wired in the y-cable attachment to the old console wiring, but not in the SE451 3-CH chassis. An additional DC-contact must be inserted as pin X in the connector Burndy 1 and wired to the !OBS_CH2_(H) signal on the motherboard (special pad available).

This modification is normally done prior to delivery at the factory. A field modification is difficult because of limited access and therefore not recommended.

Tabelle 8. Description of the jumpers on the SE-451-3CH motherboard:

Jumper (Signal)	Function	Setting	Description
JU1 (INVTGP)	Selects between high or low active transmitter gating pulses !TGPCH1a, !TGPCH2a and !TGPCH3a	open closed	Low active transmitter gating pulses. High active transmitter gating pulses.
JU2 (INVEP)	Selects between high or low active receiver gating pulses RGPa and RGPb.	open closed	Low active receiver gating pulses. High active receiver gating pulses.
JU3 (NEPL)	Selects between one or two receiver gating pulse RGPa only or RGPa and RGPb.	open closed	Transmitter and receiver EP's switched by one pulse only (RGPa). Receiver (EP) switched by RGPa, transmitters (EPX, EPH and EPY) switched by RGPb.
JU4 (NOBL)	Selects between one or three observe select signals OBS_SEL or !OBS_CH1_(X), !OBS_CH2_(H) and !OBS_CH3_(Y).	open closed	Three observe select signals !OBS_CH1_(X), !OBS_CH2_(H) and !OBS_CH3_(Y), one for each channel. One observe select signal OBS_SEL (OBS_SEL high = H-channel, low = X-channel).

Tabelle 9. Input signals of the PAL, IC7

Input signal	Pin-Nr. PLCC
RGPa	Pin 19
RGPb	Pin 20
!TGPCH1a	Pin 21
!TGPCH2a	Pin 25
!TGPCH3a	Pin 26
!OBS_CH1_(X)	Pin 27
!OBS_CH2_(H)	Pin 3
!OBS_CH3_(Y)	Pin 4
NOBL (Jumper JU4)	Pin 5
NEPL (Jumper JU3)	Pin 41
INVEP (Jumper JU2)	Pin 42
INVTGP (Jumper JU1)	Pin 43

Tabelle 10. Output signals of the PAL, IC7

Output signal	Pin-Nr. PLCC
EP	Pin 32
EPX	Pin 35
EPH	Pin 34
EPY	Pin 33
SPFX	Pin 31
SPFH	Pin 30
SPFY	Pin 29
LO1	Pin 6
LO2	Pin 7
LO3	Pin 8
LO_ON	Pin 9

In the PAL equations the following abbreviations were used

&: logical AND-relation

#: logical OR relation

$: logical EXOR-relation

!: inversion

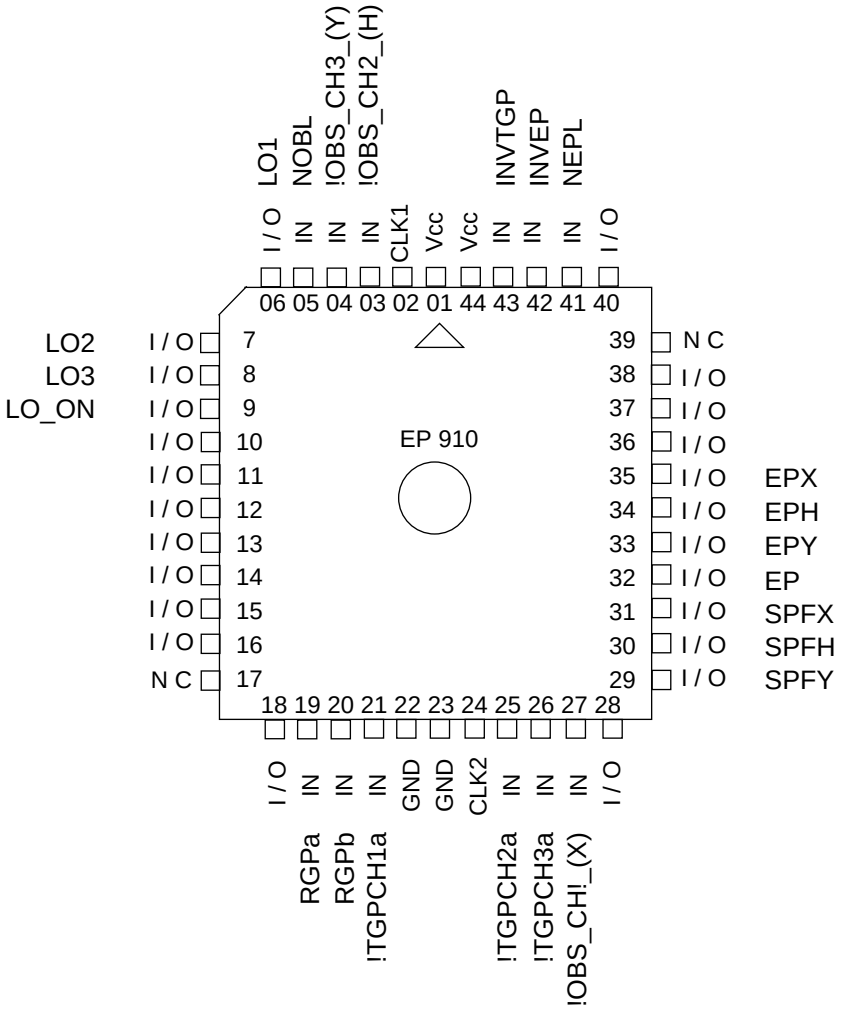
Tabelle 11. PAL equations of IC7, EP910PLCC

Signal	Equation
EPinta	RGPa $ INVEP
EPintb	RGPb $ INVEP
obsX	!(!OBS_CH1_(X))
obsH	!(!OBS_CH2_(H))
obsY	!(!OBS_CH3_(Y))
EP	EPinta (Standard pulse for the receiver)
SPFX	!TGPCH1a $ INVTGP
SPFH	!TGPCH2a $ INVTGP
SPFY	!TGPCH3a $ INVTGP
EPX	obsX & !obsH & !obsY & EPinta & NEPL & NOBL #(obsX & !obsH & !obsY & EPintb & !NEPL & NOBL) #(!obsH & EPinta & NEPL & !NOBL) #(!obsH & EPintb & !NEPL & !NOBL)
EPH	!obsX & obsH & !obsY & EPinta & NEPL & NOBL #(!obsX & obsH & !obsY & EPintb & !NEPL & NOBL) #(obsH & EPinta & NEPL & !NOBL) #(obsH & EPintb & !NEPL & !NOBL)
EPY	!obsX & !obsH & obsY & EPinta & NEPL & NOBL #(!obsX & !obsH & obsY & EPintb & !NEPL & NOBL)
!LO1	EPX (LO-SP4T-switch is LOW-active)
!LO2	EPH (LO-SP4T-switch is LOW-active)
!LO3	EPY (LO-SP4T-switch is LOW-active)
LO_ON	EPX # EPH # EPY (LO-SP2T-switch is HIGH-active)

PAL: PLCC Pin Connections 4.5

In the following figure you find the pin connections of the pal on the motherboard of the SE451-3CH. The signal names correspond to the names in the above tables.

Figure 9: Pin Connections of the PAL on the motherboard of the SE451-3CH



4Phase Modulator 5

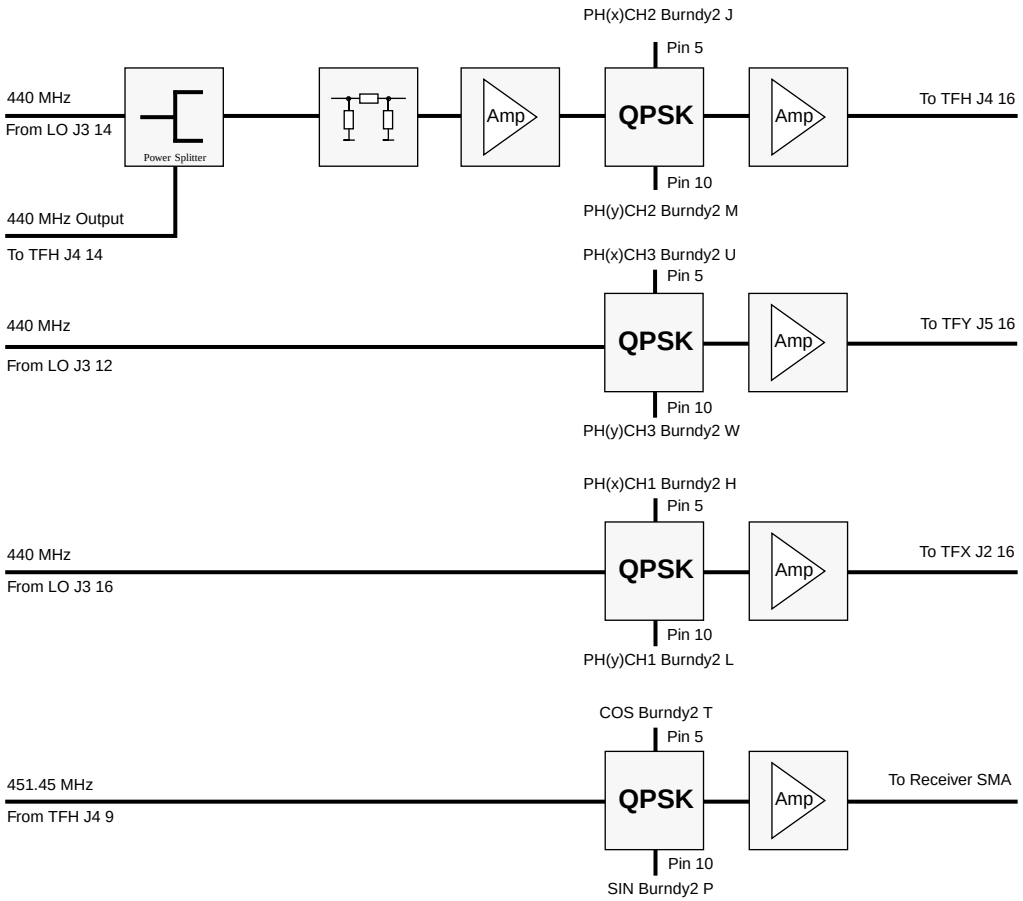
General 5.1

The SE451-3CH can be equipped with a 4Phase Modulator located on the mother-board. The 4Phase Modulator is controlled via Burndy2 connector by the 4Phase Modulator control board in the acquisition rack (AQR). This system provides fast phase switching of the three transmitter outputs and the receiver phase.

Block Diagram of 4Phase Modulator RF Board (RF part only) 5.2

The embedding of the 4Phase Modulator in the SE451-3CH environment can be seen in the overall . The 4Phase Modulator controls the phase of the 440 MHz local oscillator signals for the transmitters and the 451.45 MHz signal. This is done by QPSK phase shifters (FPQ-475 by MiniCircuits). In the chosen operation mode the QPSK modulators have an insertion loss of about 12 dB which is compensated by an amplifier. The overall gain of any of the four phase shift paths is 0 dB. The 3dB loss due to the power splitter in the TFH signal path is compensated by an additional amplifier/attenuator combination.

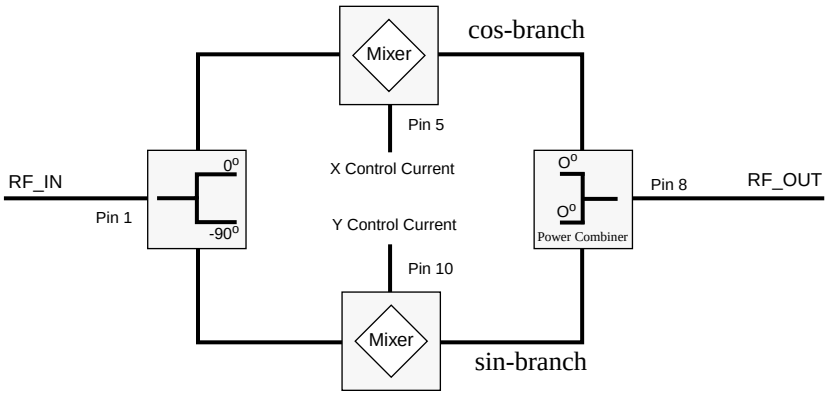
Figure 10: Block Diagram of the 4Phase Modulator RF Board



Block diagram and function description of a QPSK-modulator 5.3

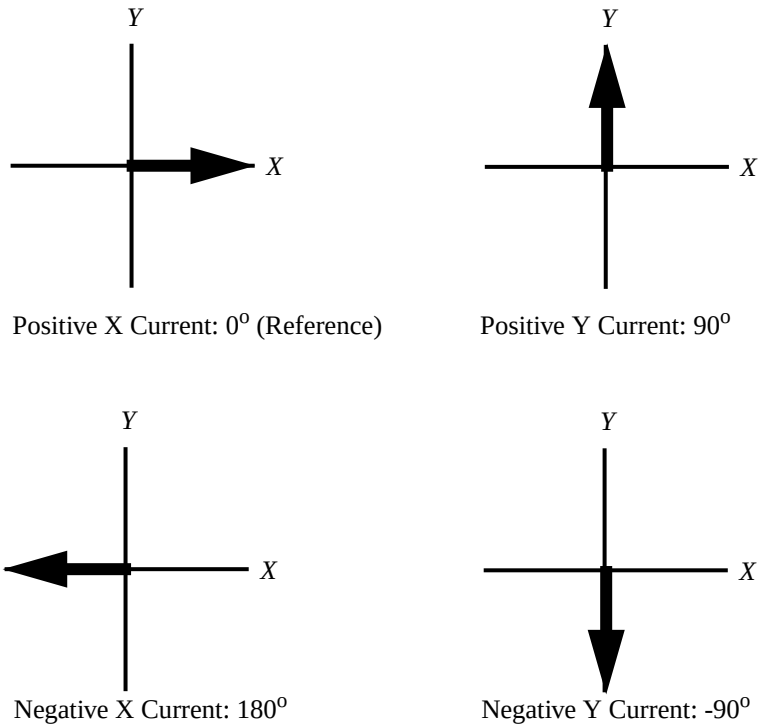
The QPSK-Blocks can be represented by the following block diagram:

Figure 11: Block Diagram of QPSK-Modulator



The mixers in the cosine and sine branches in the block diagram of the QPSK-modulator are diode ring mixers and operate as switches for the RF signal. By applying positive current (normally in the order of 20 mA) to the control port of the mixer, the RF signal is transferred without phase shift. With a negative current, the RF signal is inverted. No control current results in isolation of the according branch. The four possible control currents result in four different phase states as shown in the following figure:

Figure 12: Phase states in normal operation mode of a QPSK-modulator



The definition of the 90^o and -90^o phase shift is of course somewhat arbitrary, as the sign of the phase shift of the 90^o power splitter at the input of the QPSK-block is not known and was chosen to be -90^o in the above example.

Function description of the 4Phase Modulator 5.4

As an extension of the normal operation of a QPSK-modulator the mixers can be used as electronic attenuators, the attenuation being set by the diode control current at the LO-port of the mixer. In addition the two branches (sine and cosine) can be selected at the same time. If the RF signal is again represented by a vector in the XY-plane the vector can now reach any point in the coordinate system. With some trigonometry the principle is easily understood:

Suppose the RF input signal is

$$A \cdot \cos(\omega t)$$

A being any amplitude of no importance. After the mixer the signal in the cosine branch is

$$A_X \cdot \cos(\omega t)$$

A_X being controlled by the X control current. Again after the mixer, the signal in the sine branch is

$$A_Y \cdot \sin(\omega t)$$

A_Y is controlled by the Y control current. After the power combiner at the output, the RF signal is

$$A_X \cdot \cos(\omega t) + A_Y \cdot \sin(\omega t)$$

which is equal to

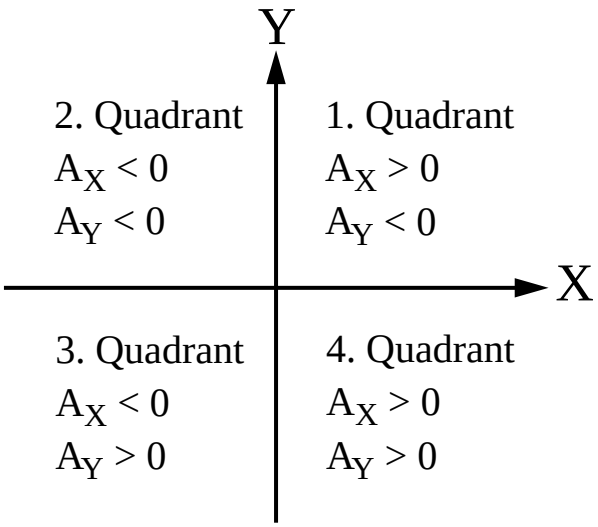
$$A \cdot \cos(\omega t + \varphi)$$

with

$$A = \sqrt{A_X{}^2 + A_Y{}^2} \qquad \varphi = \operatorname{atan}\left(\frac{-A_Y}{A_X}\right)$$

The next figure shows again the XY-plane and the conditions on A_Y and A_X for the RF signal vector to be in one of the four quadrants.

Figure 13: Control currents for 4 quadrant phase shift



Temperature Controller 6

General 6.1

The SE451-3CH is equipped with a temperature controller. This device regulates the temperature to a constant operating point to ensure maximum stability. Even if the regulator is switched off the system is very stable due to the ingenious air guide and the long time constant for temperature changes (in the order of 15 minutes).

For stable operation the spectrometer should be in an air-conditioned room. The temperature controller is able to compensate the remaining temperature changes of an air-conditioning system (about +/-4 degrees). The regulator does not eliminate the need for air-conditioning as it has not been designed to compensate large temperature differences (e.g. 10 degrees or more).

There are basically two different versions of the temp. contrl. board installed in the SE451-3CH. They are referred to in this chapter as print index Z4P3032 and as index Z4P3032A or higher (Z4P3032A and B). The main difference is the operating point adjustment procedure. The easiest way to find out which controller version is installed in your unit is by counting the LED's at the front panel. Index Z4P3032 has two (one green and one red), index Z4P3032A or higher has three (one green and two red).

Function description 6.2

A temperature sensor (AD592) measures the temperature in the QD-module of the receiver of the SE451-3CH unit. This sensor signal is fed into a P-regulator which controls the input voltage of the variofan cooling the unit (regulation of the air flow by varying the speed of rotation (revolutions per minute) of the fan).

Operation 6.3

The temperature controller tries to keep the temperature inside the unit constant. However it can only do so for ambient temperatures within a certain range around a preset regulator operating point. The higher the ambient temperature the smaller the temperature range which the controller is able to compensate. At an ambient temperature of 20^{o} Celsius (293K) this range is +/-5 degrees around the operating point. At 30^{o} Celsius (303K) this range reduces to +/-3 degrees.

If the ambient temperature leaves the range which the controller can compensate, an error is indicated by the error LED on the front panel. The controller operating point must then be adjusted to the new ambient temperature. The following paragraph describes how to adjust the operating point of the regulator.

Operating point adjustment index Z4P3032 6.3.1

To adjust the operating point you must first switch the controller off with the front panel switch (position REGULATOR OFF). This mode disables the regulator and connects the fan to a constant voltage (9V). The system must then be stabilized at the new ambient temperature for at least one hour.

After this time the regulator operating point can be adjusted on the front panel potentiometer („Operating Point Adjust“). The aim of the adjustment is to reach a regulator output voltage of 9V (the same as the constant fan voltage when the regulator is off). The regulator output voltage can be measured with a voltmeter at pin 8 of the 25 Sub-D connector RXC on the front panel of the SE451-3CH. If you measure this voltage you must turn the adjustment-potentiometer until the voltmeter shows a reading of 1.8Volts.

If the adjustment has been performed the regulator can be switched on (REGULATOR ON) with the front panel switch.

Operating point adjustment index A and higher 6.3.2

The adjustment of the controller operating point has been improved for boards with index A and higher (Z4P3032A or B). An additional LED has been implemented (named „Not Adjusted“ on the front panel) to indicate the proper setting of the regulator operating point. The procedure of the regulator adjustment is as follows:

Switch the controller off with the front panel switch (position REGULATOR OFF). This mode disables the regulator and connects the fan to a constant voltage (9V). The system must then be stabilized at the new ambient temperature for at least two hours. After this time the regulator operating point can be adjusted on the front panel potentiometer („Operating Point Adjust“). The red LED („Not Adjusted“) is on as long as the regulator operating point is not adjusted. The LED turns off if the regulator is adjusted. Turn the potentiometer until the „Not Adjusted“-LED does no longer shine. Be aware that the „off window“ of the LED is quite small and therefore easy to miss if the adjustment is done to fast. You can then switch on the regulator with the front panel switch (REGULATOR ON).

LED descriptions 6.4

LED green: +19V 6.4.1

The green LED (+19V) indicates that the +19V supply of the fan is OK. In both modes (REGULATOR ON and OFF) the green LED must be on. Otherwise the device is out of order and must be repaired.

LED red: ERROR 6.4.2

If the regulator is on (REGULATOR ON switch position) the red LED (ERROR) indicates that the operating point should be adjusted. It does not mean however that NMR-experiments should not be performed. Just switch the regulator off (The ERROR LED does no longer shine) and go on with your measurements. The system is very stable even in the constant fan operating mode (REGULATOR OFF). For maximum stability adjust the operating point of the controller. To do this follow the procedure described above („Adjustment of the operating point“). During normal operation of the regulator the red LED should not shine.

If the regulator is off (REGULATOR OFF switch position) the red LED should never be on. If the LED shines in the „regulator off“-mode the device is out of order and must be repaired.

LED red: Not Adjusted (Z4P3032A and higher only) 6.4.3

For temperature controllers with index A and higher an additional red LED has been implemented to simplify the adjustment procedure of the regulator.

If the regulator is on (REGULATOR ON switch position) this red LED should never be on.

If the regulator is off (REGULATOR OFF switch position) this LED is on as long as the operating point of the controller is not properly set. Turn the „operating point adjust“ potentiometer until the LED turns off. If the operating point is adjusted the LED does not shine and the regulator can be switched on.

External fan supply 6.5

SE451-3CH units with temperature controller boards index Z4P3032A or higher are equipped with an external fan supply. This is either a modified PSD1 board in the AQR-Rack or an extra plug-in power pack. The ext. fan supply connector is located at the back of the SE451-3CH unit.

External fan supply monitor 6.6

The ext. supply voltage is monitored to ensure save operation of the SE451-3CH unit. If by any cause the ext. supply voltage fails, an alarm will sound. In this case check for proper connection and function of the ext. fan supply.

BBIS for SE451-3CH 7

General 7.1

The SE451-3CH unit has a built in BBIS (Bruker Board Information System) chip. It is an I2C-EEPROM controlled via the RXC receiver controller board in the AQR rack. The BBIS circuit is galvanic isolated from the SE451 motherboard and supplied from the RXC board.

The BBIS information is structured into four blocks or pages in the following order:

1. Production page
2. Service page
3. Device block
4. Application block

Their contents is read by the UXNMR to configure the proper control signals for the SE451-3CH. They can also be read by the user with the RXC-tool.

Block / page description 7.2

Structure, datatypes and contents of the following blocks and pages are according to document ZDEN0001 BBIS-Manual. More detailed information is available from Spectrospin AG, Fällanden.

BBIS production page 7.2.1

This page contains all production data (serial numbers, production date and place etc.). It is factory configurated and should therefore not be changed.

Tabelle 12. Example for a production page:

Type	Length	Data	Description
V	1	2	dataformat version for the production page
C	1	S	protocol devicename
S	5	SE19	device callname
S	16	Z003020	partnumber [example 300MHz unit]

Type	Length	Data	Description
T	16	0002	serialnumber
S	10	Z4P2997A	printnumber SE451 motherboard
U	1	16	hardware code SE451 motherboard
T	7	940506	produktion date [y m d]
C	1	Z	produktion location [Z = Zurich Fällanden]
U	1	1	produktion department
S	5	SLE	testengineer
I	1	3	test department
I	1	0	ECL (after delivery)
S	13	0	reserve (13 bytes, always 0)

BBIS service page 7.2.2

This page contains all service data (repair date and place etc.). It is factory configurated and should therefore not be changed.

Tabelle 13. Example for a service page:

Type	Length	Data	Description
V	1	2	dataformat version for the service page
T	16	--	repair number
U	1	8	hardware code after repair
T	7	--	repair / modification date
T	5	--	service engineer
C	1	F	repair location
U	1	1	ECL after modification
S	15	0	reserve (15 bytes, always 0)

This block contains all device data (built-in modules and their configuration etc.). It is factory configurated and should therefore not be changed.

Tabelle 14. Example for a device block:

Type	Length	Data	Description
V	1	0	dataformat version for the device block
U	1	1	motherboard type [1 = QUAD]
U	1	0	motherboard type reserve
U	1	250	1st transmitter type [TFX SL]
U	1	0	1st transmitter type reserve
U	1	57	2nd transmitter type [TFH SL 300MHz]
U	1	0	2nd transmitter type reserve
U	1	250	3rd transmitter type [TFX SL]
U	1	0	3rd transmitter type reserve
U	1	0	4th transmitter type [not placed]
U	1	0	4th transmitter type reserve
U	1	249	1st receiver type [SL]
U	1	0	1st receiver type reserve
U	1	0	2nd receiver type [not placed]
U	1	0	2nd receiver type reserve
U	1	0	3rd receiver type [not placed]
U	1	0	3rd receiver type reserve
U	1	0	4th receiver type [not placed]
U	1	0	4th receiver type reserve
U	1	0	LO reserve
U	1	0	LO reserve
S	42	0	reserve (42 bytes, always 0)

BBIS application block 7.2.4

This block contains all application data. Users and service personnel can write in here any data they want, for example some special settings, adjustments etc. This block is not used by the UXNMR and therefore open to everyone.

Tabelle 15. Example for an application block:

Type	Length	Data	Description
V	1	2	dataformat version for the application block
S	16	--	reserve
S	16	--	reserve
S	16	--	reserve
S	14	--	reserve

Technical Data 8

General Specifications 8.1

Number of Channels with observe capability:	3
Frequency Range (FULLBAND):	5 ..... 750MHz
Frequency-Steps:	0.01Hz
TR Pulse (ON/OFF):	100nS
TR switching Time:	< 5uS
Phase Modulation:	0.1uS (0.05deg)(via DDS)
IF-Frequency:	451MHz (..MX,..SX
	22MHz (..RX)
Amplitude Stability:	RX: 0.15dB/K
	TX: -1dB/K
Phase Stability:	RX: 10˚/K
	TX: 10˚/K
Phase Modulation via WAVEFORM-Generator:	0.1uS (0.05deg)(via DDS)
Amplitude Modulation without WAVEFORM-Generator:	
Modulation:	60dB, 0.14dB Resolution
Attenuation:	90dB, 0.07dB Resolution
Gain Range (w/o Preamp):	-80 ..... +10dBm
Noise Figure:	7 dB @ max. Gain
	~50 dB @ min. Gain
Gain Steps:	3dB (..RX)
	6 dB (..MX, ..SX)
Bandwith with BB Option:	400kHz (3dB)
	2.5MHz (1dB)
Quad Image:	1% / 0.2% (QP, NS8)
O1-Spike:	1% / 0.2% (QP, NS8)
50Hz - Sidebands:	typ. 0.2%

Power Supply (including 4Phase Modulator) 8.2

Currents indicated are currents including 4Phase Modulator Option

+19V supply current:	2800	mA
-19V supply current:	300	mA
+9V supply current:	700	mA

Warm-up time constant 8.3

Warm-up time (time from system power-up to stable RF-operation)

Warm-up time	2 h

Pulse Propagation Delay (Motherboard only) 8.4

Pulse propagation delay of PAL (IC7) and Output Buffer (IC , 74AS757) on the SE451-3CH motherboard Z4P2997, according to data sheets (not measured):

Minimum Propagation Delay	33 ns
Maximum Propagation Delay	45 ns

Receiver Gain Table 8.5

Tabelle 16. Gain Table for 6dB Steps SE451-3CH

RG	RG UXNMR	RG [dB]	DRG0 (RG6)	DRG1 (IF0)	DRG2 (AGC_A)	DRG3 (AGC_B)	DRG4 (RF_A)	DRG5 (RF_B)
1	1	12	0	1	0	0	0	0
2	2	18	1	1	0	0	0	0
4	4	24	0	1	0	0	1	0
8	8	30	1	1	0	0	1	0
16	16	36	0	1	0	0	0	1
32	32	42	1	1	0	0	0	1
64	64	48	0	1	0	0	1	1
128	128	54	1	1	0	0	1	1
256	256	60	0	0	0	0	1	1
512	512	66	1	0	0	0	1	1
1k	1024	72	0	0	1	0	1	1
2k	2048	78	1	0	1	0	1	1
4k	4096	84	0	0	0	1	1	1
8k	8192	90	1	0	0	1	1	1
16k	16384	96	0	0	1	1	1	1
32k	32768	102	1	0	1	1	1	1

Table 17: ECL Information for 3-Channel SE451

ECL	Additional Features or Changes	Print Index (Motherboard)	HW-Code	PLD Software
Prototype		Z4P2997A	8	
ECL 00	1. BBIS Piggi-back print Z4P3031 2. Temp. Control Board index Z4P3032 or Z4P3032A 3. Ext. fan supply from AQR PSD1 board or from plug-in Power pack (Temp. Contr. Board index Z4P3032A only)	Z4P2997B	16	SE30AA01-ZE
ECL 01	1. BBIS on motherboard 2. Additional attenuator in each phase-shifter path 3. Temp. Control Board index Z4P3032B 4. Ext. fan supply from plug-in power pack	Z4P2997C	32	SE30AA01-ZE

Y-Cable Z12621 10

General 10.1

The Y-cable provides compatibility to earlier 2 channel SE451 units which have separate Burndy connectors with control and power supply lines for each individual SE451-module (TFX, TFH, LO and Receiver, RFT). In the SE451-3CH all power supply and control lines are contained in connector Burndy1 (See the chapter about Burndy1 connector (SE451 Control) on page 11). The Y-cable is the interface between these two connector systems.

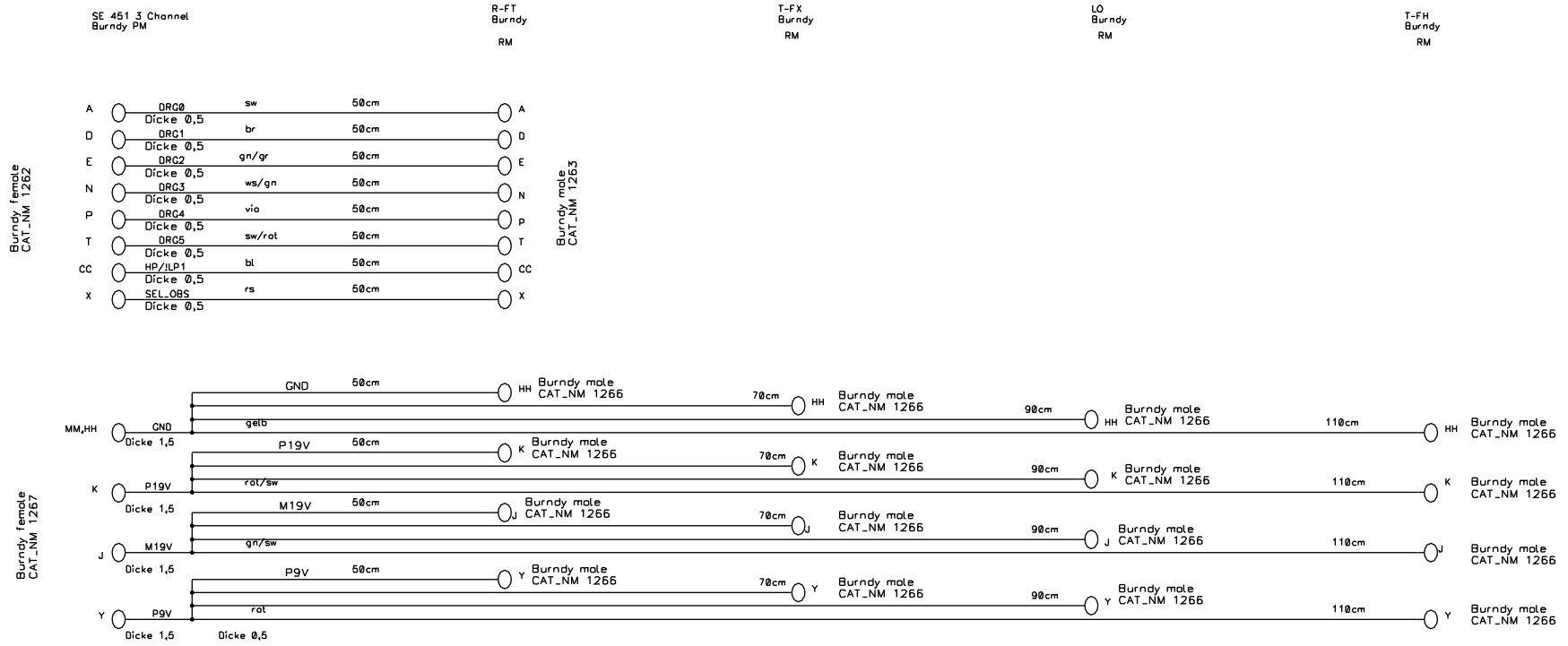
Operation of SE451-3CH with Y-cable 10.2

In order for the SE451-3CH to behave like a 2 channel SE451 the Y-cable must be connected and the jumpers (solder-type) on the SE451-3CH motherboard must be set accordingly. For a description of the jumper settings see the chapter about PAL Equations on page 19, especially the paragraph about Jumpers on page 19. Basically all jumpers must be set when working in the 2 channel mode. For individual experiments or applications transmitter and/or receiver pulses can be inverted by appropirate jumper setting.

Note that the 3rd (Y-) channel of the SE451-3CH is not controlled via the Y-cable and performs no action in the 2 channel operating mode.

Wiring of the Y-cable 10.3

On the following pages you will find the wiring diagrams of the SE451-3CH Y-cable



SE451-3CH

Y-Kabel

DC Wiring
Sheet 1 of 2
Print No:
DWG No:

Part-No. for Drawing only	Drawn	Approv.	Modification				A3
Z12621	SLE 24.05.94						

SPECTROSPIN

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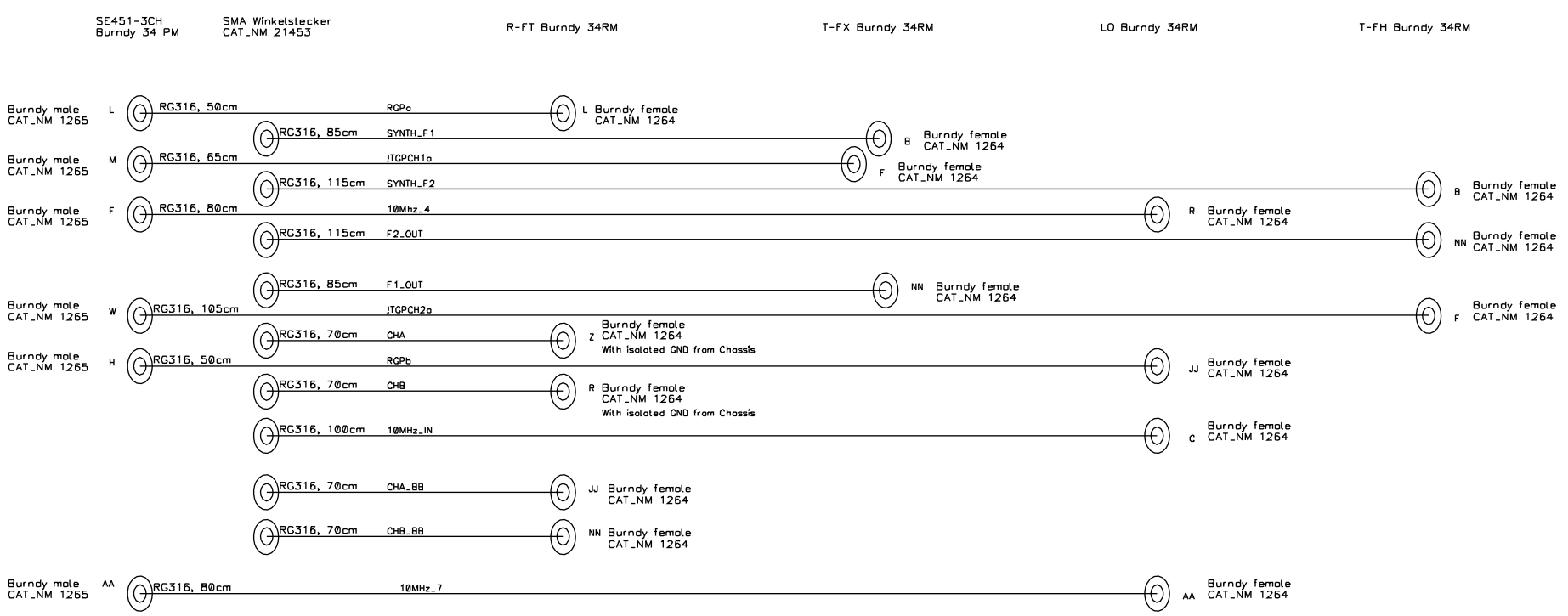


SE451-3CH

Y-Kabel

HF Wiring
Sheet 2 of 2
Print No:
DWG No:

Part-No. for Drawing only	Drawn	Approv.	Modification				A3
Z12621	SLE 24.05.94						

SPECTROSPIN

Schematics Motherboard 11

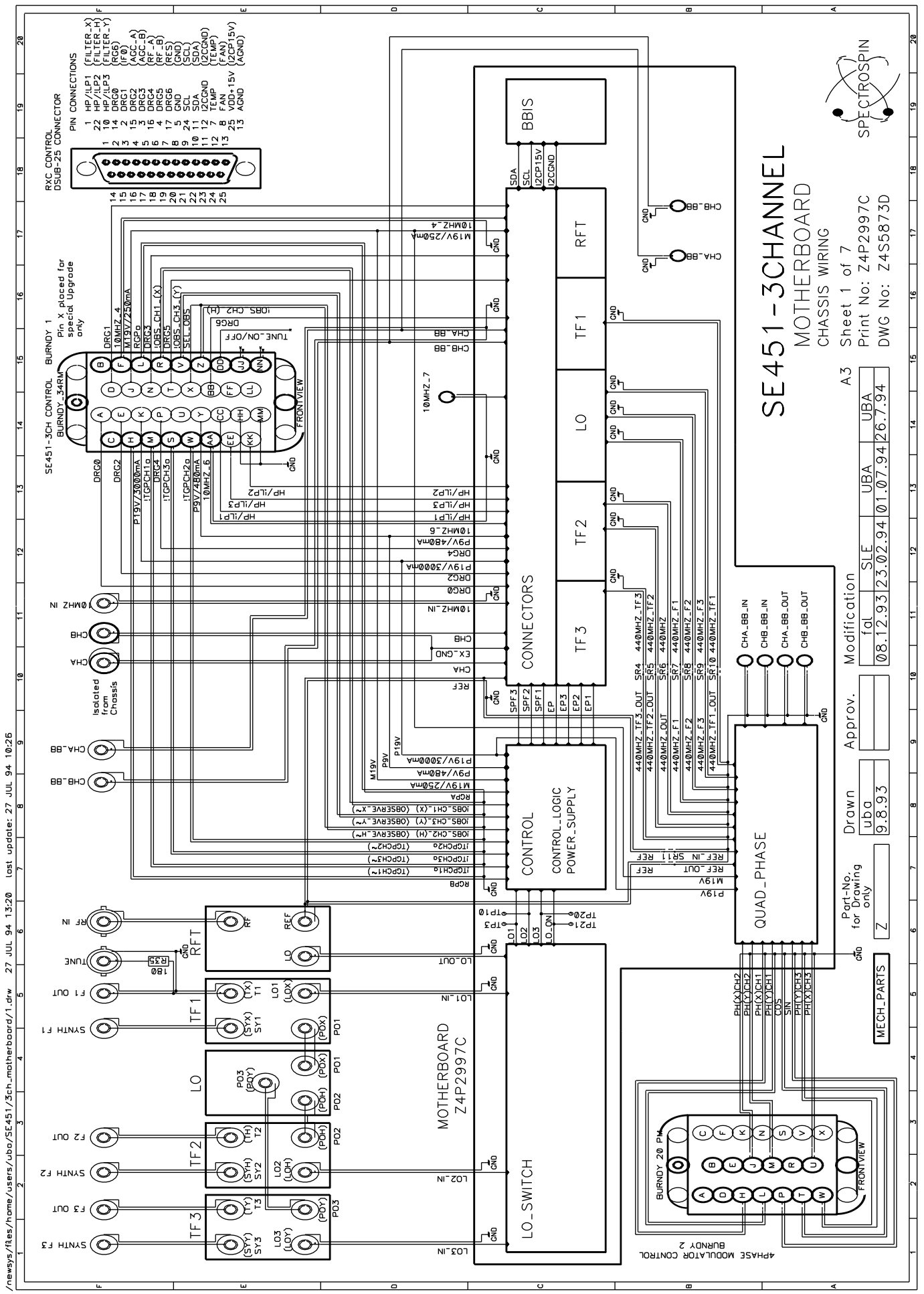
On the following pages you will find the schematics of the SE451-3CH motherboard Z4P2997C..

Motherboard Index B:

The SE451-3CH motherboard index B is almost identical to the index C described in this chapter. The only differences are the location of the BBIS circuit and the connection to the Temp. Contr. board.

The BBIS circuit is new on the motherboard itself, whereas on index B it was on a piggy-back print. For further information please refer to the BBIS schematic chapter.

Schematics and Assembly 11.1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MOTHERBOARD
CHASSIS WIRING
A3 Sheet 1 of 7
Print No: Z4P2997C
DWG No: Z4S5873D
SPECTROSPIN
Modification
fal 08.12.93
SLE 23.02.94
UBA 01.07.94
UBA 26.7.94
Approv.
Drawn uba 9.8.93
Part-No. for Drawing only Z
MOTHERBOARD Z4P2997C
CONNECTORS
CONTROL
CONTROL_LOGIC POWER_SUPPLY
QUAD_PHASE
LO_SWITCH
RFT
TF1
TF2
TF3
LO
BBIS
RXC CONTROL DSUB-25 CONNECTOR
SE451-3CH CONTROL BURNDY_34RM
BURNDY 1
Pin X placed for special Upgrade only
BURNDY 20 PH
4PHASE MODULATOR CONTROL BURNDY 2
MECH_PARTS
Isolated from Chassis
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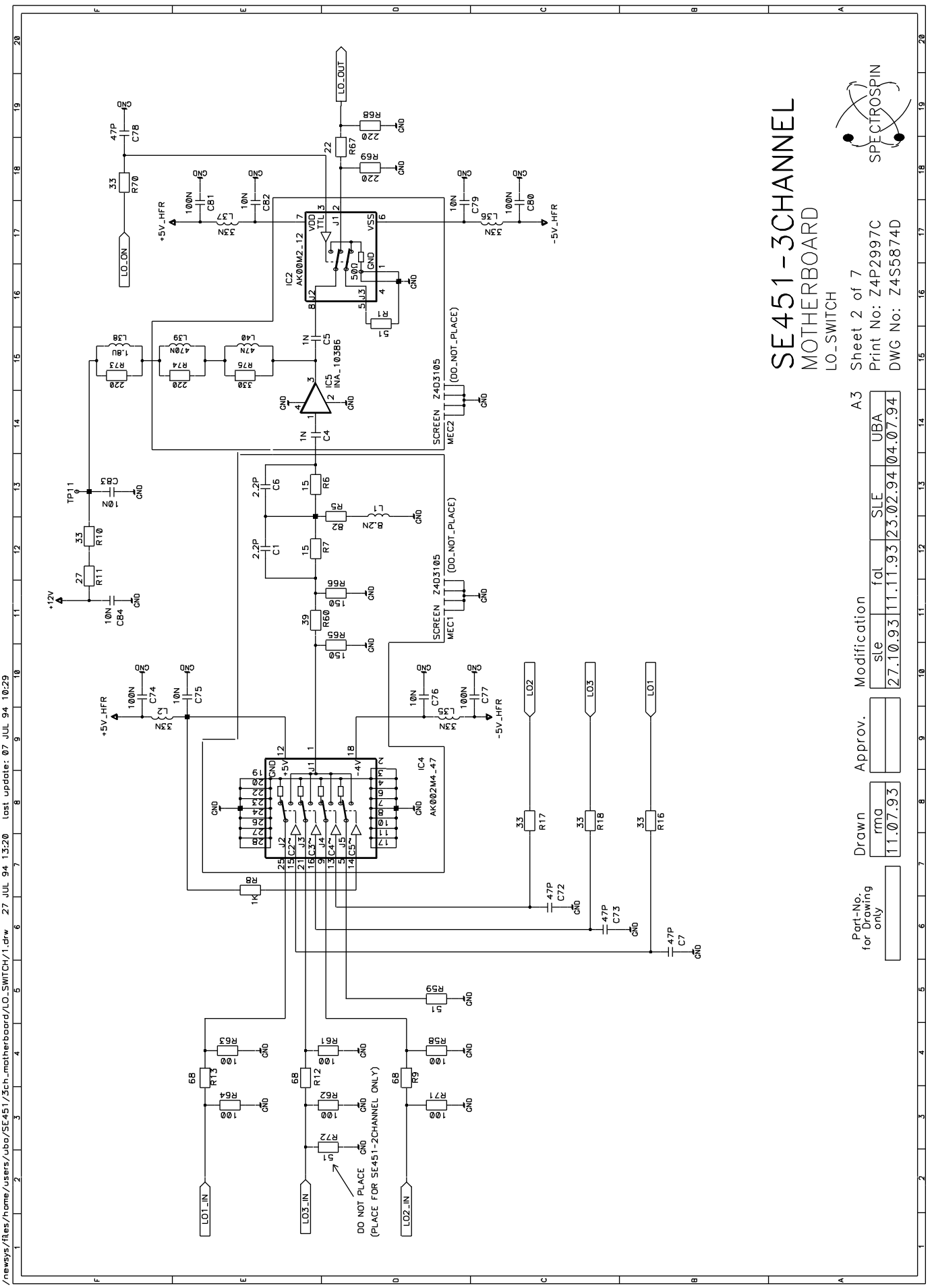
SE451-3CHANNEL
MOTHERBOARD
LO_SWITCH
Sheet 2 of 7
Print No: Z4P2997C
DWG No: Z4S5874D
SPECTROSPIN
A3
Modification
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fal 11.11.93
SLE 23.02.94
UBA 04.07.94
Drawn rma 11.07.93
Approv.
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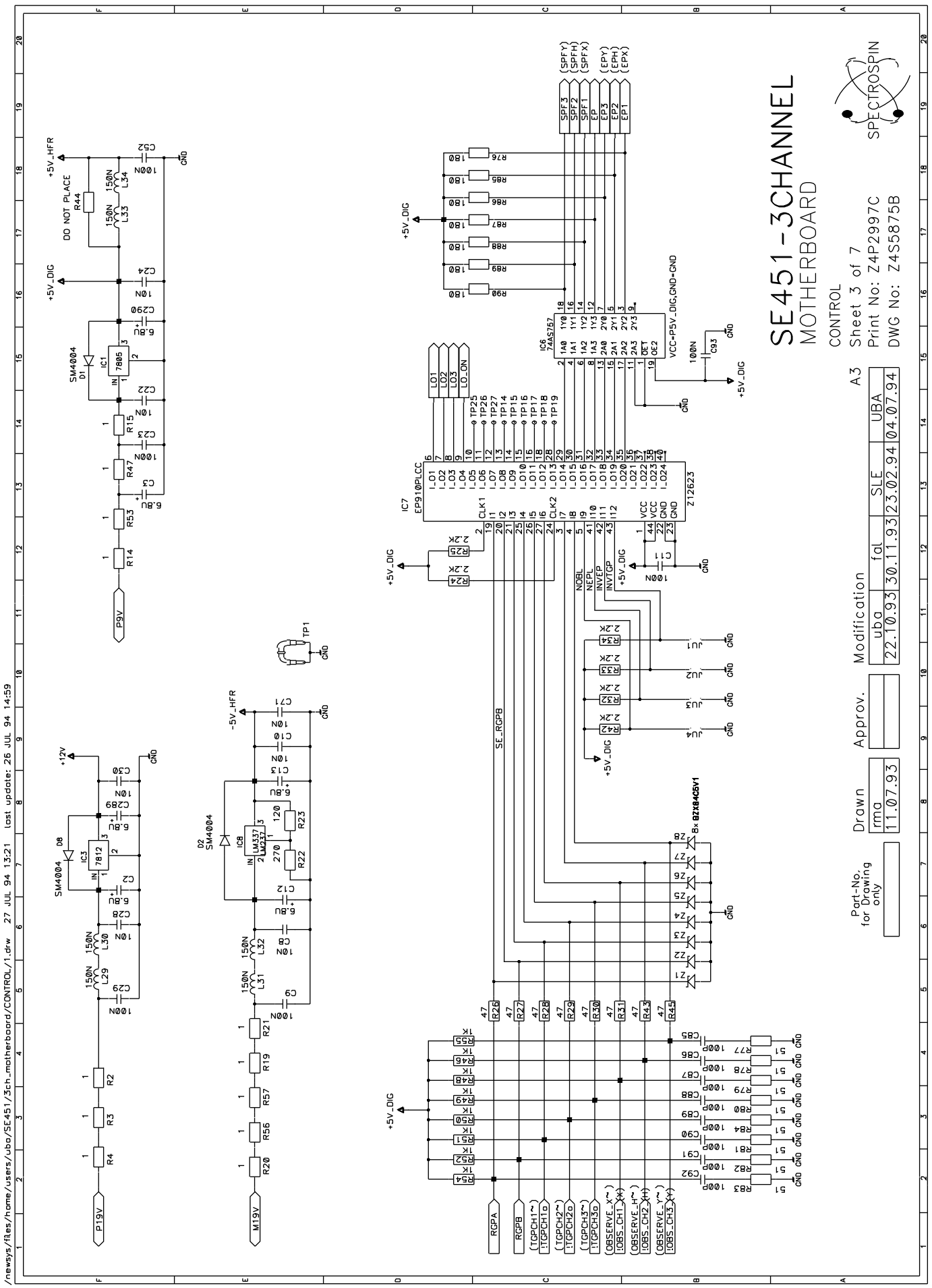
LO_OUT
LO_ON
IC2 AK00M2_12
IC5 INA_10386
IC4 AK002M4_47
SCREEN Z4D3105 (DO_NOT_PLACE) MEC2
SCREEN Z4D3105 (DO_NOT_PLACE) MEC1
+5V_HFR
-5V_HFR
+12V
LO1
LO2
LO3
LO1_IN
LO2_IN
LO3_IN
DO NOT PLACE (PLACE FOR SE451-2CHANNEL ONLY)


SE451-3CHANNEL
MOTHERBOARD
CONTROL
Sheet 3 of 7
Print No: Z4P2997C
DWG No: Z4S5875B
A3
SPECTROSPIN
Modification
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fal 30.11.93
SLE 23.02.94
UBA 04.07.94
Drawn rma 11.07.93
Approv.
Part-No. for Drawing only
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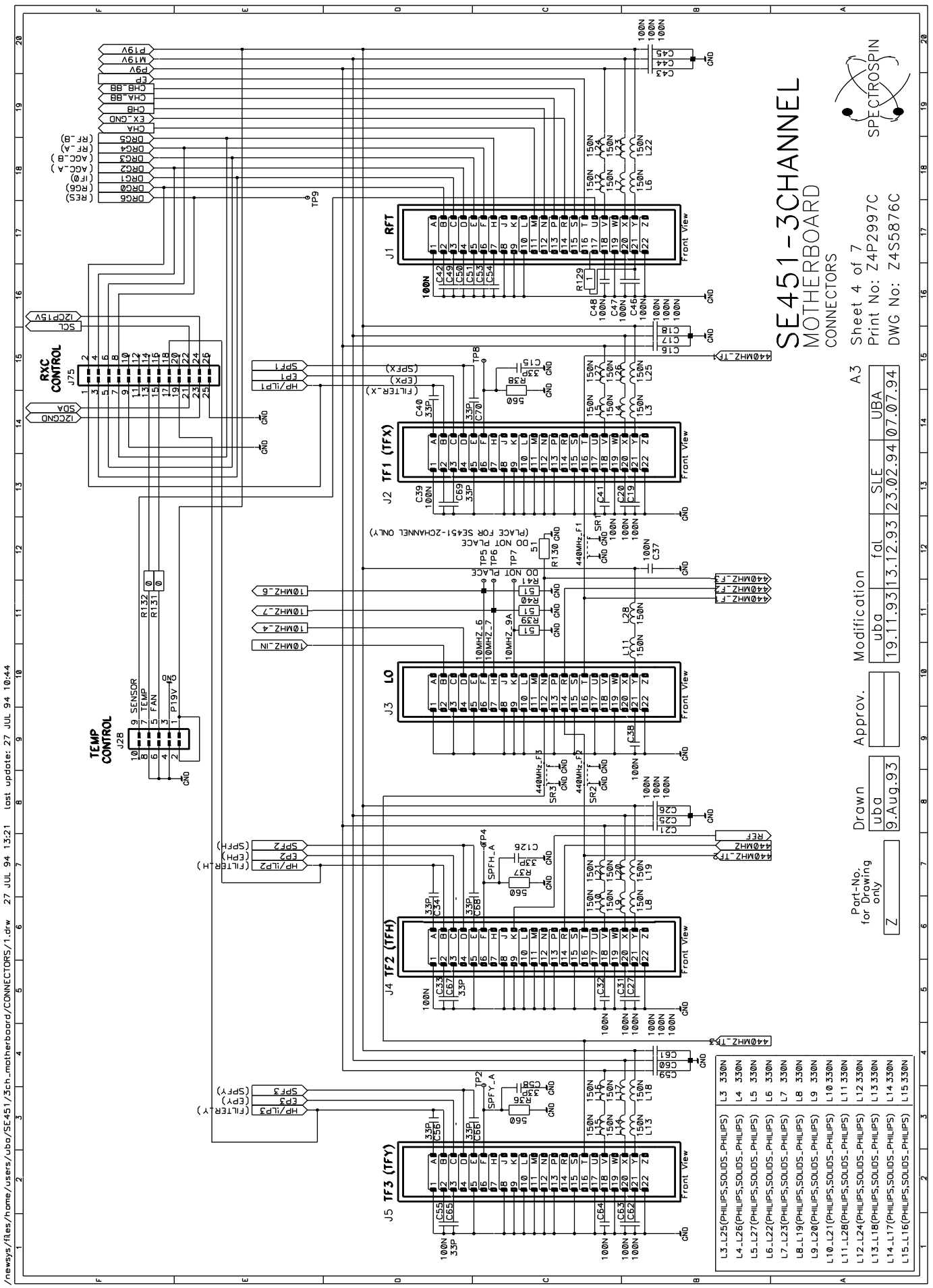
+5V_HFR
+5V_DIG
-5V_HFR
+12V
P19V
M19V
P9V
SM4004
DO NOT PLACE
IC1 7805
IC3 7812
IC8 LM337 LM237
IC6 74AS767
IC7 EP910PLCC
Z12623
BZX84C5V1
SE_RGPB
RGPA
RGPB
(TGPCH1~)
!TGPCH1
(TGPCH2~)
!TGPCH2
(TGPCH3~)
!TGPCH3
(OBSERVE_X~)
!OBS_CH1_(X)
(OBSERVE_H~)
!OBS_CH2_(H)
(OBSERVE_Y~)
!OBS_CH3_(Y)
(SPFY)
(SPFH)
(SPFX)
(EPY)
(EPH)
(EPX)
SPF3
SPF2
SPF1
EP
EP3
EP2
EP1
LO1
LO2
LO3
LO_ON
VCC=+P5V_DIG,GND=GND
NOBL
NEPL
INVEP
INVTGP
TP1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MOTHERBOARD
CONNECTORS
Sheet 4 of 7
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DWG No: Z4S5876C
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A3
Modification
uba 19.11.93
fal 13.12.93
SLE 23.02.94
UBA 07.07.94
Approv.
Drawn uba 9.Aug.93
Part-No. for Drawing only Z
RXC CONTROL J75
TEMP CONTROL J28
J1 RFT
J2 TF1 (TFX)
J3 LO
J4 TF2 (TFH)
J5 TF3 (TFY)
Front View
L3 330N (L3_L25(PHILIPS,SOLIDS_PHILIPS))
L4 330N (L4_L26(PHILIPS,SOLIDS_PHILIPS))
L5 330N (L5_L27(PHILIPS,SOLIDS_PHILIPS))
L6 330N (L6_L22(PHILIPS,SOLIDS_PHILIPS))
L7 330N (L7_L23(PHILIPS,SOLIDS_PHILIPS))
L8 330N (L8_L19(PHILIPS,SOLIDS_PHILIPS))
L9 330N (L9_L20(PHILIPS,SOLIDS_PHILIPS))
L10 330N (L10_L21(PHILIPS,SOLIDS_PHILIPS))
L11 330N (L11_L28(PHILIPS,SOLIDS_PHILIPS))
L12 330N (L12_L24(PHILIPS,SOLIDS_PHILIPS))
L13 330N (L13_L18(PHILIPS,SOLIDS_PHILIPS))
L14 330N (L14_L17(PHILIPS,SOLIDS_PHILIPS))
L15 330N (L15_L16(PHILIPS,SOLIDS_PHILIPS))
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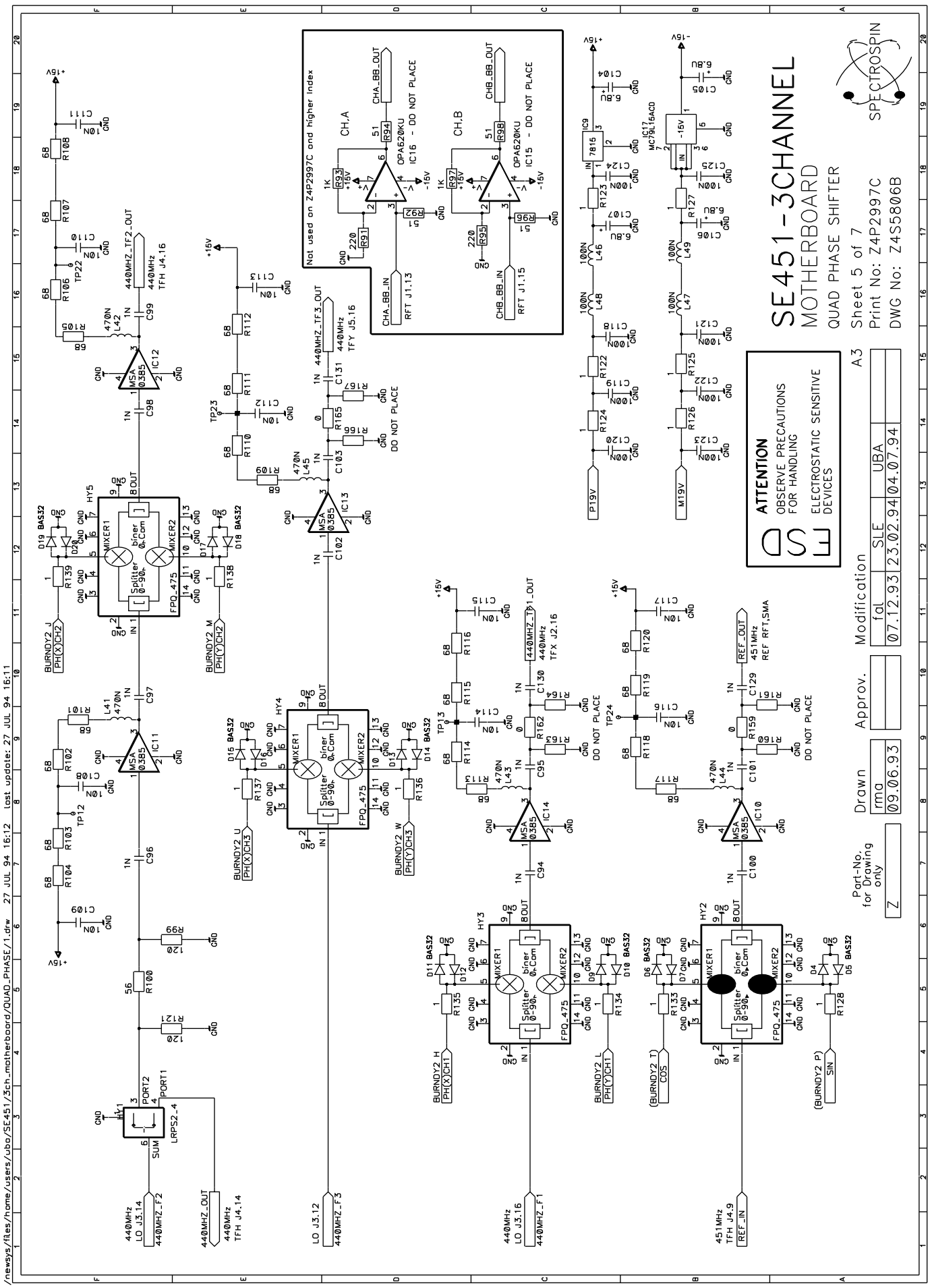
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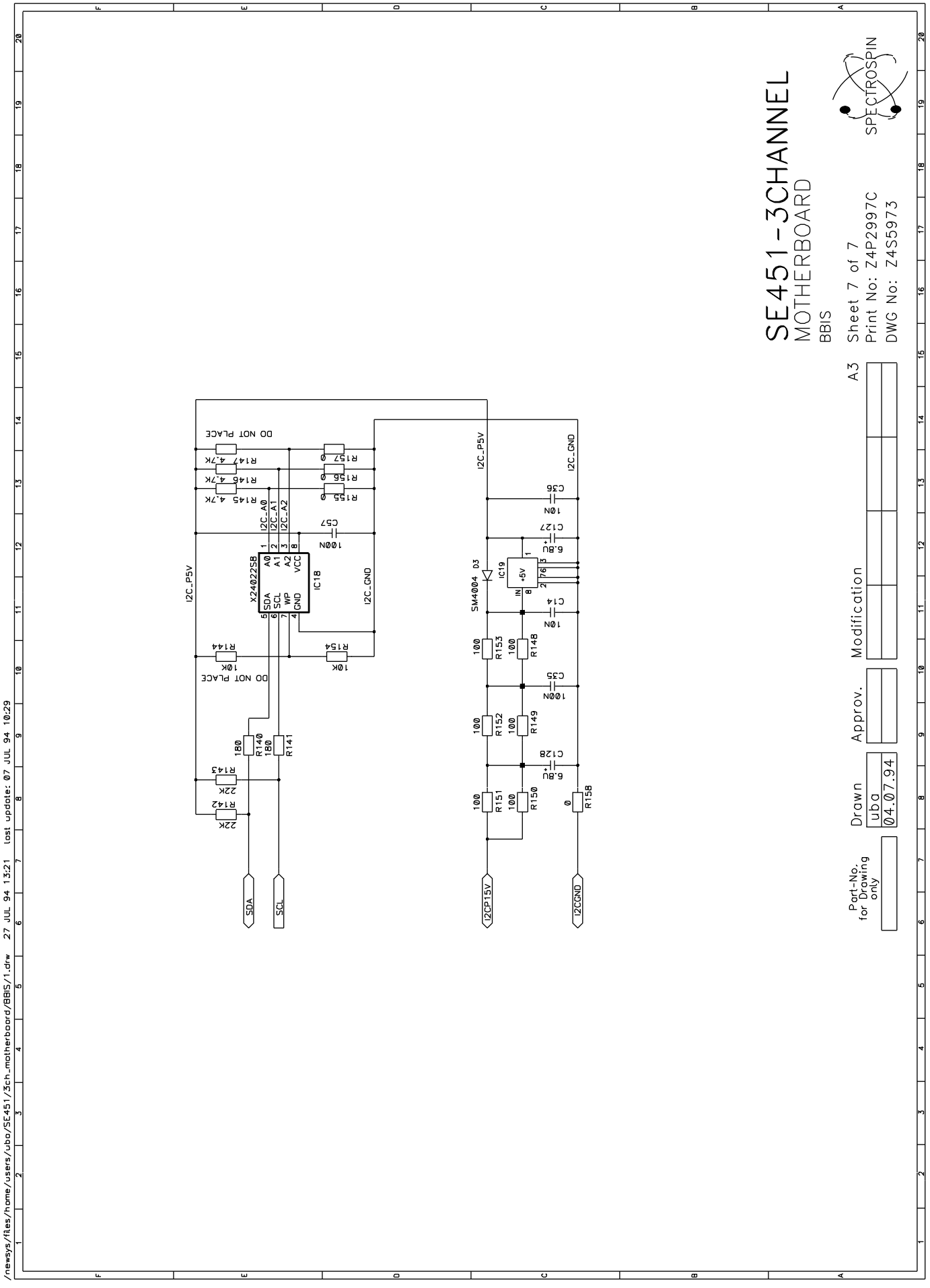
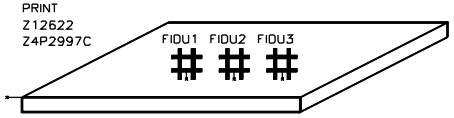
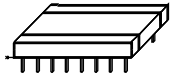
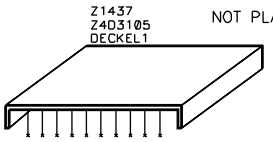
MOTHERBOARD
QUAD PHASE SHIFTER
Sheet 5 of 7
Print No: Z4P2997C
DWG No: Z4S5806B
SPECTROSPIN
ATTENTION
OBSERVE PRECAUTIONS FOR HANDLING
ELECTROSTATIC SENSITIVE DEVICES
Modification
fal 07.12.93
SLE 23.02.94
UBA 04.07.94
Drawn rma 09.06.93
Approv.
Part-No. for Drawing only
A3
Not used on Z4P2997C and higher index
CH.A
CH.B
OPA620KU
IC16 - DO NOT PLACE
IC15 - DO NOT PLACE
CHA_BB_OUT
CHB_BB_OUT
CHA_BB_IN
CHB_BB_IN
RFT J1.13
RFT J1.15
440MHZ_TF2_OUT
440MHZ_TF3_OUT
440MHZ_TF1_OUT
TFH J4.16
TFY J5.16
TFX J2.16
DO NOT PLACE
MIXER1
MIXER2
Splitter 0-90°
FPQ_475
MSA 0385
HY1
HY2
HY3
HY4
HY5
PORT1
PORT2
SUM
LRPS2_4
BURNDY2_J PH(X)CH2
BURNDY2_M PH(Y)CH2
BURNDY2_U PH(X)CH3
BURNDY2_W PH(Y)CH3
BURNDY2_H PH(X)CH1
BURNDY2_L PH(Y)CH1
BURNDY2_T COS
BURNDY2_P SIN
440MHz LO J3.14
440MHZ_F2
440MHZ_OUT
440MHz TFH J4.14
LO J3.12
440MHZ_F3
440MHz LO J3.16
440MHZ_F1
451MHz TFH J4.9
REF_IN
REF_OUT
451MHz REF RFT,SMA
+15V
-15V
P19V
M19V
/newsys/files/home/users/ubo/SE451/3ch_motherboard/QUAD_PHASE/1.drw 27 JUL 94 16:12 last update: 27 JUL 94 16:11


SE451-3CHANNEL
MOTHERBOARD
BBIS
Sheet 7 of 7
Print No: Z4P2997C
DWG No: Z4S5973
SPECTROSPIN
A3
Modification
Approv.
Drawn
uba
04.07.94
Part-No. for Drawing only
/newsys/fltes/home/users/uba/SE451/3ch_motherboard/BBIS/1.drw 27 JUL 94 13:21 last update: 07 JUL 94 10:29
DO NOT PLACE
I2C_P5V
I2C_GND
I2C_A0
I2C_A1
I2C_A2
X24022SB
IC18
SDA
SCL
WP
GND
VCC
SM4004 D3
IC19
+5V
IN
SDA
SCL
I2CP15V
I2CGND

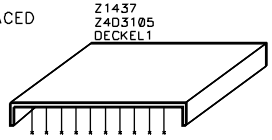
/newsys/files/home/users/uba/SE451/3ch_motherboard/MECH_PARTS/1.drw 27 JUL 94 13:22 last update: 27 JUL 94 10:34







NOT PLACED



VARIANTEN:
COILCRAFT und PHILIPS

SR1
16193
l=29mm

SR2
16193
l=33mm

SR3
16193
l=76mm

VARIANTEN:
SOLIDS_COILCRAFT und
SOLIDS_PHILIPS

SR4
16193
l=228mm

SR5
16193
l=272mm

SR6
16193
l=98mm

SR7
16193
l=97mm

SR8
16193
l=57mm

SR9
16193
l=111mm

SR10
16193
l=225mm

SR11
16193
l=221mm

SE451 3-CHANNEL

MOTHERBOARD

MECHANICAL PARTS

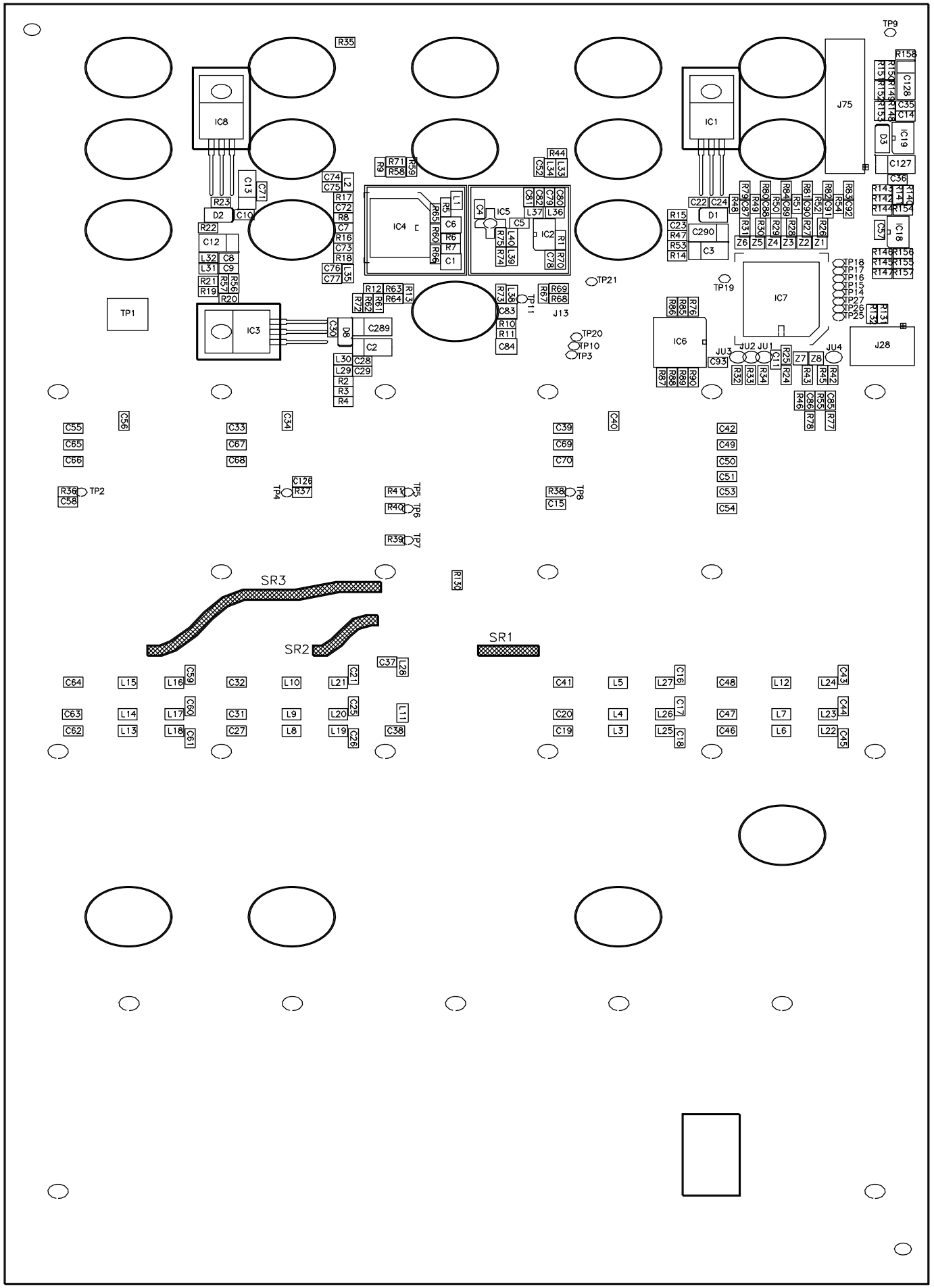
Sheet 6 of 7

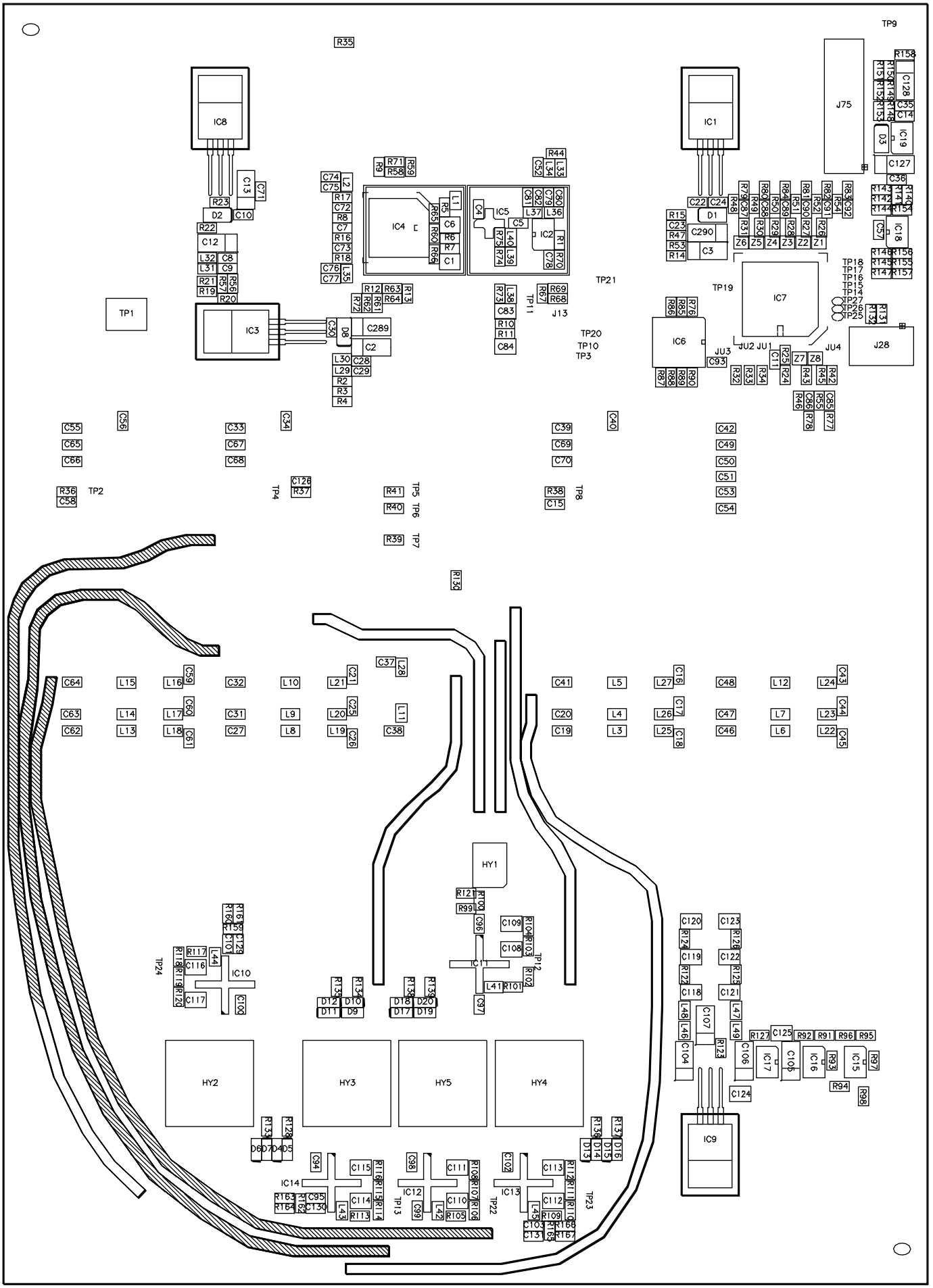
Print No: Z4P2997C

DWG No: Z4S5877B

Part-No. for Drawing only	Drawn	Approv.	Modification				A3
			SLE	UBA			
Z	uba 16.8.93		23.02.94	04.07.94			

SPECTROSPIN

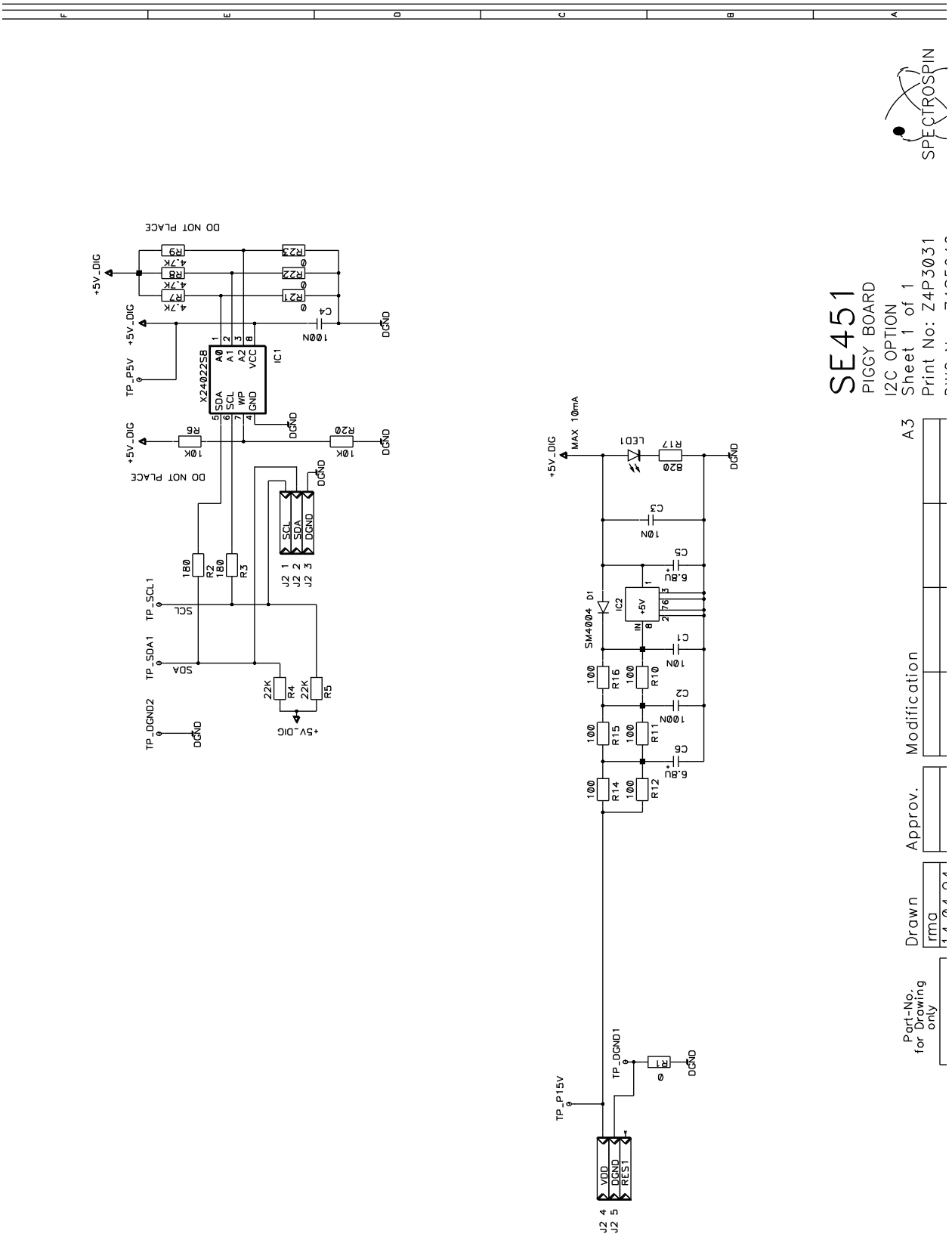

TP9
R158
R35
IC8
IC1
J75
C128
C36
C14
IC19
D3
C127
C13
C71
C74
C75
L2
R17
C72
R8
C7
R16
C73
R18
C76
C77
L35
R23
D2
C10
R22
C12
L32
C8
L31
C9
R21
R57
R56
R19
R20
R9
R71
R59
R58
R44
C52
L33
L34
IC4
L1
R5
R63
C6
R60
R6
R65
R7
C1
C4
IC5
C5
C81
C82
C80
C79
L37
L36
IC2
L40
L39
R1
R70
R73
R74
C78
C22
C24
R48
D1
R15
C25
R47
R53
R14
C290
C3
R79
C87
R31
R80
C88
R49
R30
R29
R84
C89
R51
R28
R81
C90
R52
R27
R82
C91
R54
R29
R83
C92
Z6
Z5
Z4
Z3
Z2
Z1
R143
R142
R144
R141
R140
R139
C57
IC18
R148
R149
R147
R158
R155
R157
TP18
TP17
TP16
TP15
TP14
TP27
TP26
TP25
R132
R131
J28
TP21
TP19
IC7
IC6
R86
R85
R76
R96
R88
R89
R90
R87
JU3
JU2
JU1
JU4
C93
C11
R25
R24
R43
R45
R42
R32
R33
R34
Z7
Z8
R46
C86
R78
R55
C85
R77
R12
R63
R13
R64
R61
R62
R72
R69
R67
R68
L38
R73
TP11
C83
R10
R11
C84
J13
TP20
TP10
TP3
TP1
IC3
C30
D8
C289
C2
L30
C28
L29
C29
R2
R3
R4
C55
C65
C66
C56
C33
C67
C68
C34
C39
C69
C70
C40
C42
C49
C50
C51
C53
C54
R36
C58
TP2
C126
TP4
R37
R41
TP5
R40
TP6
R39
TP7
TP8
C15
R38
R139
SR3
SR2
SR1
C37
L28
C64
L15
L16
C59
C32
L10
L21
C21
C63
L14
L17
C60
C31
L9
L20
C25
L11
C62
L13
L18
C61
C27
L8
L19
C26
C38
C41
L5
L27
C16
C48
L12
L24
C43
C20
L4
L26
C17
C47
L7
L23
C44
C19
L3
L25
C18
C46
L6
L22
C45

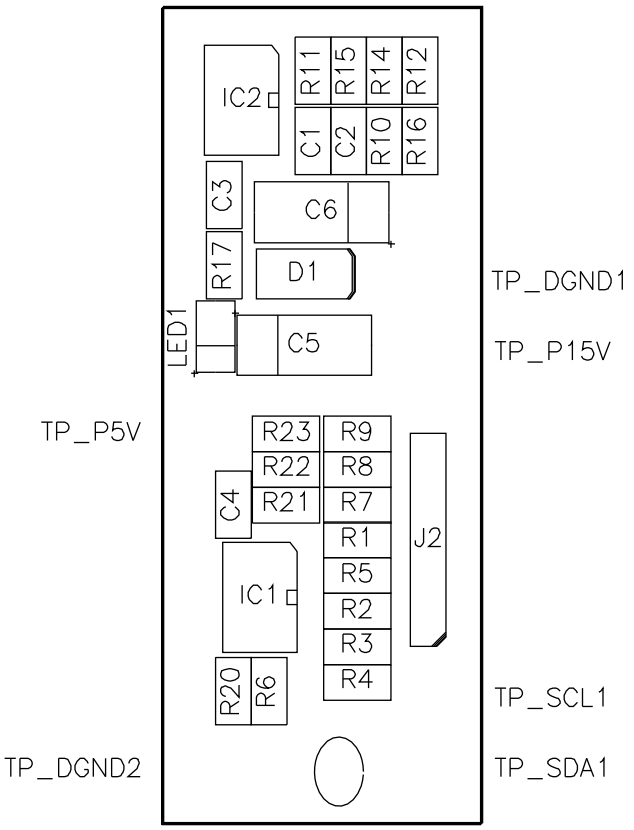

IC8
IC1
J75
IC4
IC5
IC2
IC3
IC7
IC6
J28
J13
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP11
TP12
TP13
TP18
TP19
TP20
TP21
TP22
TP23
TP24
HY1
HY2
HY3
HY5
HY4
IC9
IC10
IC11
IC12
IC13
IC14
IC15
IC16
IC17
IC18
IC19
JU1
JU2
JU3
JU4

Schematics BBIS Board 12

On the following pages you will find the schematics of the SE451-3CH I2C Piggy Back Board (Z4P3031) which implements the BBIS (BRUKER Board Information System) for motherboard versions with Index A and B (Z4P2997A and Z4P2997B).

Figure 18: BBIS Piggy-Back .


SE451
PIGGY BOARD
I2C OPTION
Sheet 1 of 1
Print No: Z4P3031
A3
Modification
Approv.
Drawn
rma
Part-No. for Drawing only
DO NOT PLACE
+5V_DIG
TP_P5V
TP_SCL1
TP_SDA1
TP_DGND2
TP_P15V
TP_DGND1
DGND
IC1
X24022SB
IC2
+5V
SM4004
D1
LED1
MAX 10mA
SCL
SDA
J2 1
J2 2
J2 3
J2 4
J2 5
VDD
DGND
RES1



SE451
I2C Option
Assembly Drawing
Sheet 1 of 1
Print No : Z4P3031
DWG No : Z4D5343

Part-No. for Drawing only	Drawn	Approv.	Modification
Z	21.04.94 mer		

SPECTROSPIN

Schematics Temp. Contr. 13

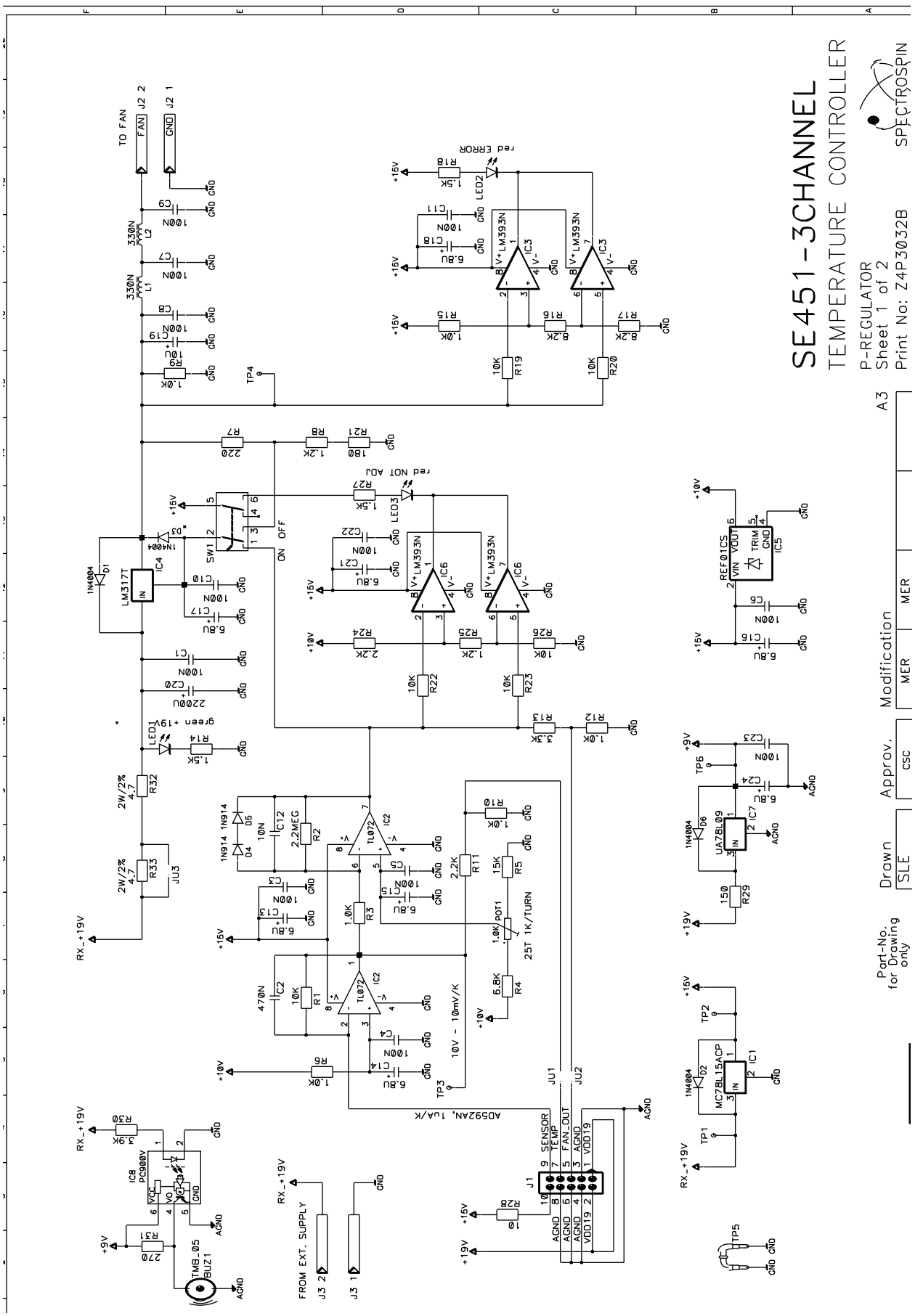
On the following pages you will find the schematics of the SE451-3CH temperature controller board Z4P3032B.

Temperature Controller Index A:

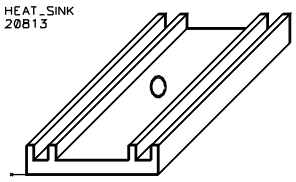
The Temp. Contr. board index A is almost identical to the index B described in this chapter. The only difference is the location of the ext. power supply monitor circuit.

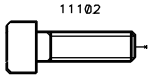
Print index Z4P3032B have the monitor circuit on board, whereas index A boards have an extra piggy-back print with the same function. The circuit itself is the same.

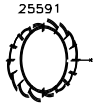
Figure 19: Temperature Controller

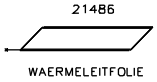

SE451-3CHANNEL
TEMPERATURE CONTROLLER
P-REGULATOR
Sheet 1 of 2
Print No: Z4P3032B
SPECTROSPIN
A3
Modification
MER
Approv.
CSC
Drawn
SLE
Part-No. for Drawing only
TO FAN
FAN
GND
J2 2
J2 1
red ERROR
red NOT ADJ
green +19V
ON OFF
SW1
LM317T
REF01CS
TRIM
VIN
VOUT
UA7BL09
MC7BL15ACP
TL072
LM393N
AD592AN, 1uA/K
10V - 10mV/K
POT1
25T 1K/TURN
PC900V
TMB_05
BUZ1
FROM EXT. SUPPLY
J3 2
J3 1
J1
SENSOR
TEMP
FAN_OUT
AGND
VDD19
JU1
JU2
JU3
TP1
TP2
TP3
TP4
TP5
TP6
RX_+19V
+19V
+15V
+10V
+9V
GND
AGND

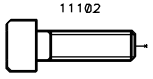
/files/home/users/mer/project/se451/temp_controller/MECH_PARTS/1.drw 22 SEP 94 16:46 last update: 22 SEP 94 16:44

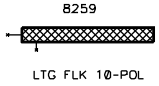


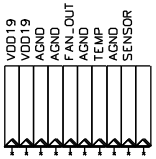


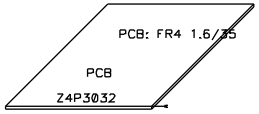












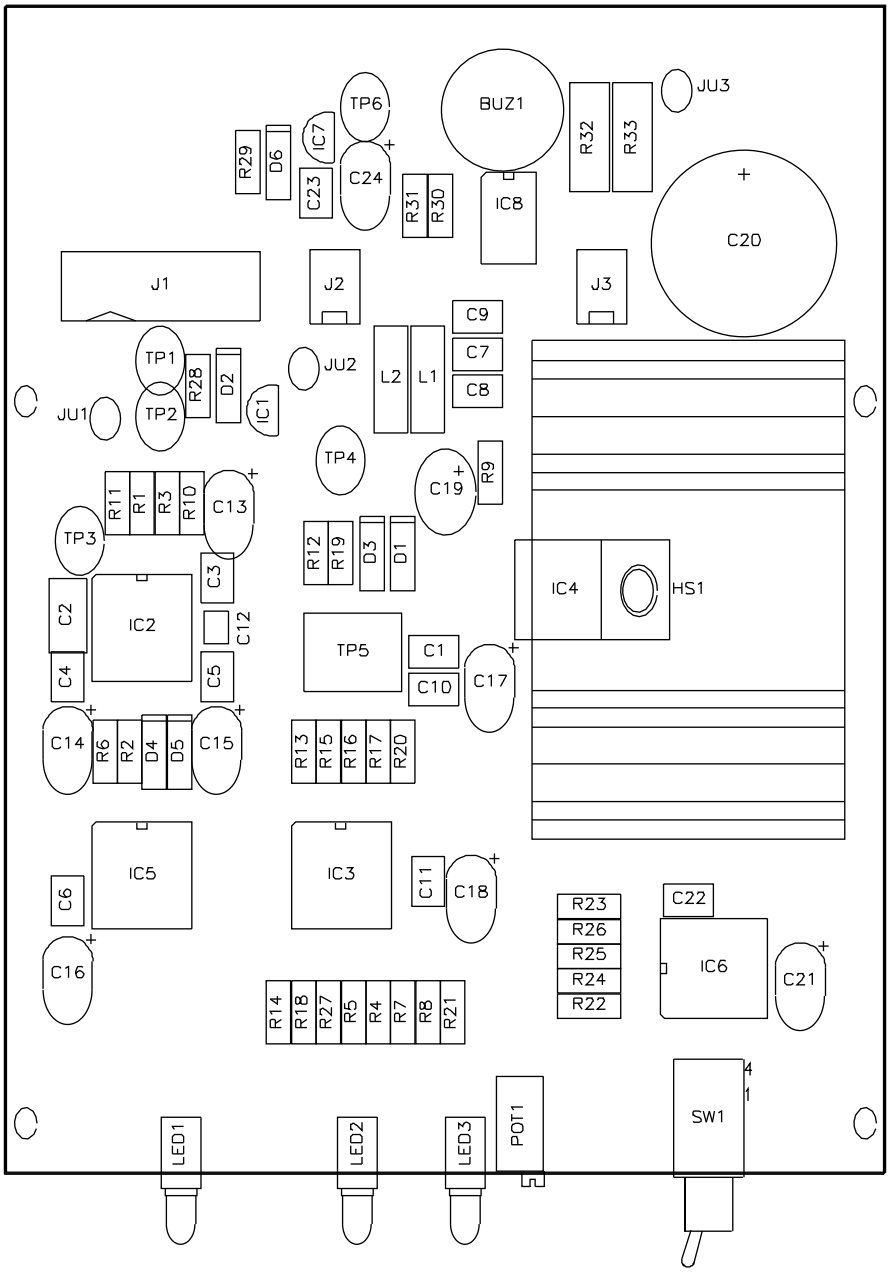
SE451-3CH

TEMPERATURE CONTROLLER

MECHANICAL PARTS
Sheet 2 of 2
Print No: Z4P3032B
DWG No: Z4S5943B

Part-No. for Drawing only	Drawn	Approv.	Modification			A3
	SLE	CSC	MER			
	21.04.94	22.09.94	22.09.94			

SPECTROSPIN



SE451-3CH

TEMPERATURE CONTROLLER

Assembly Drawing

Sheet 1 of 1

Print No : Z4P3032B

DWG No : Z4D5347B

Part-No. for Drawing only	Drawn	Approv.	Modification	
Z	04.05.94 mer	22.9.94 CSC	25.07.94 MER	22.09.94 MER

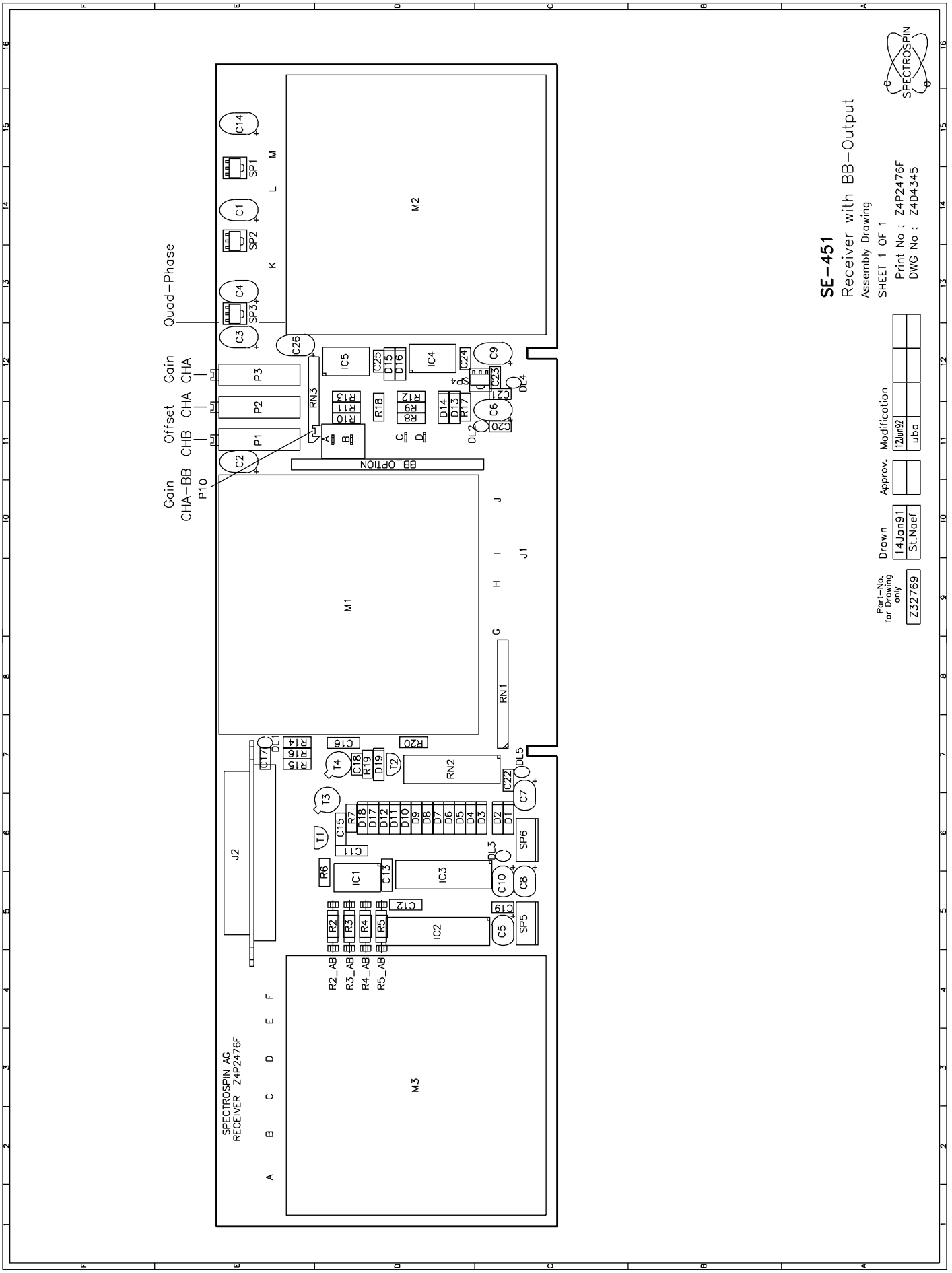
SPECTROSPIN

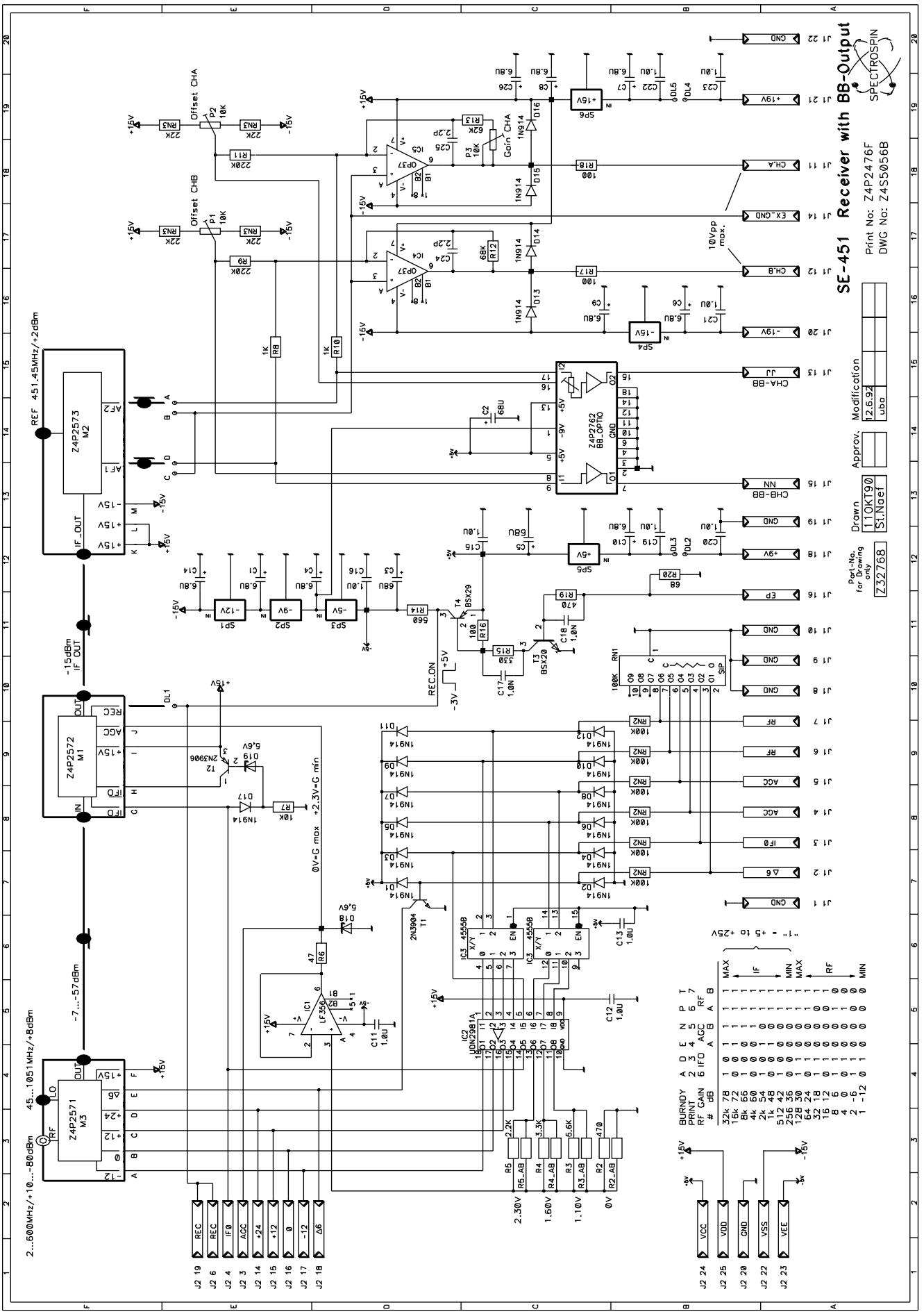
Schematics Receiver Board14

Schematics and Assembly 14.1

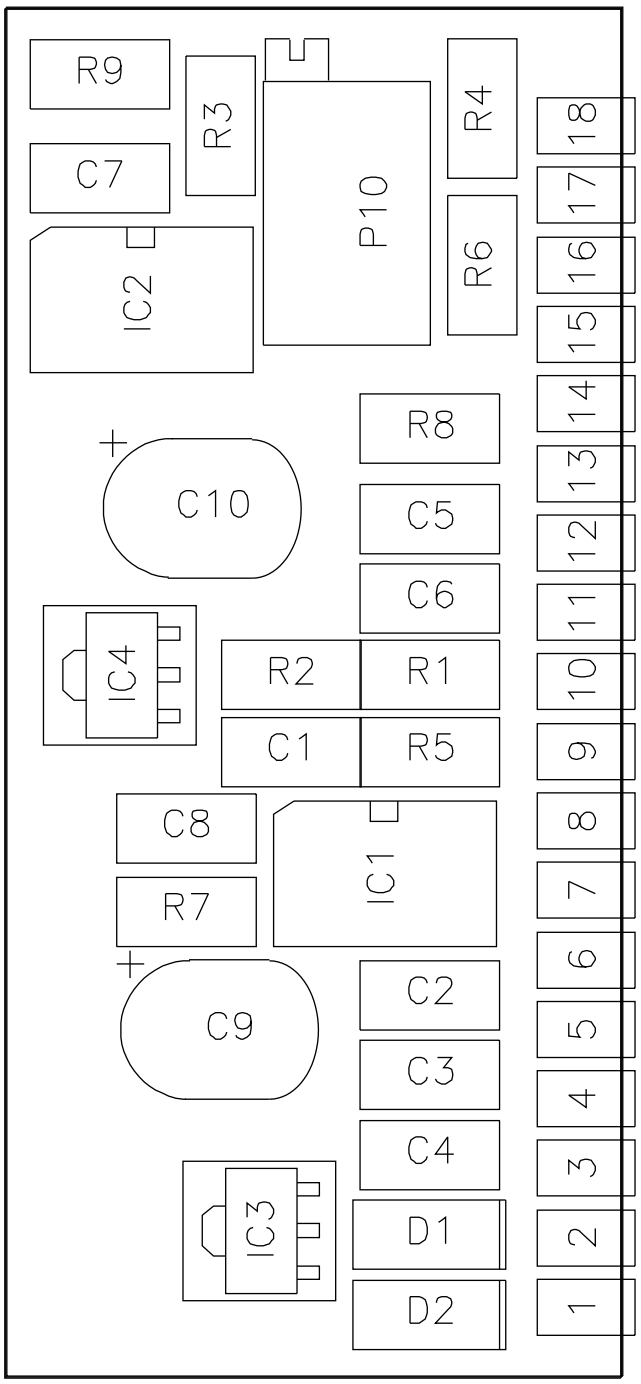
On the following pages you will find the schematics of the SE451-3CH Receiver Board (Z4P2476F) including the BB-Option (Z4P2762C), the RF-Modul (Z4P2571E) and the QD-Modul (Z4P2573F).

The schematics for the IF-Modul, which is also mounted on the Receiver Board, are not included in this chapter. However you will find the appropriate information in the appendage at the end of this manual.


SE-451
Receiver with BB-Output
Assembly Drawing
SHEET 1 OF 1
Print No : Z4P2476F
DWG No : Z4D4345
SPECTROSPIN
Modification
12Jun92 uba
Approv.
Drawn
14Jan91 St.Naef
Part-No. for Drawing only
Z32769
Quad-Phase
Gain CHA
Offset CHA
CHB
Gain CHA-BB
P10
P1
P2
P3
SP1
SP2
SP3
SP4
SP5
SP6
M1
M2
M3
J1
J2
BB OPTION
RN1
RN2
RN3
IC1
IC2
IC3
IC4
IC5
SPECTROSPIN AG
RECEIVER Z4P2476F



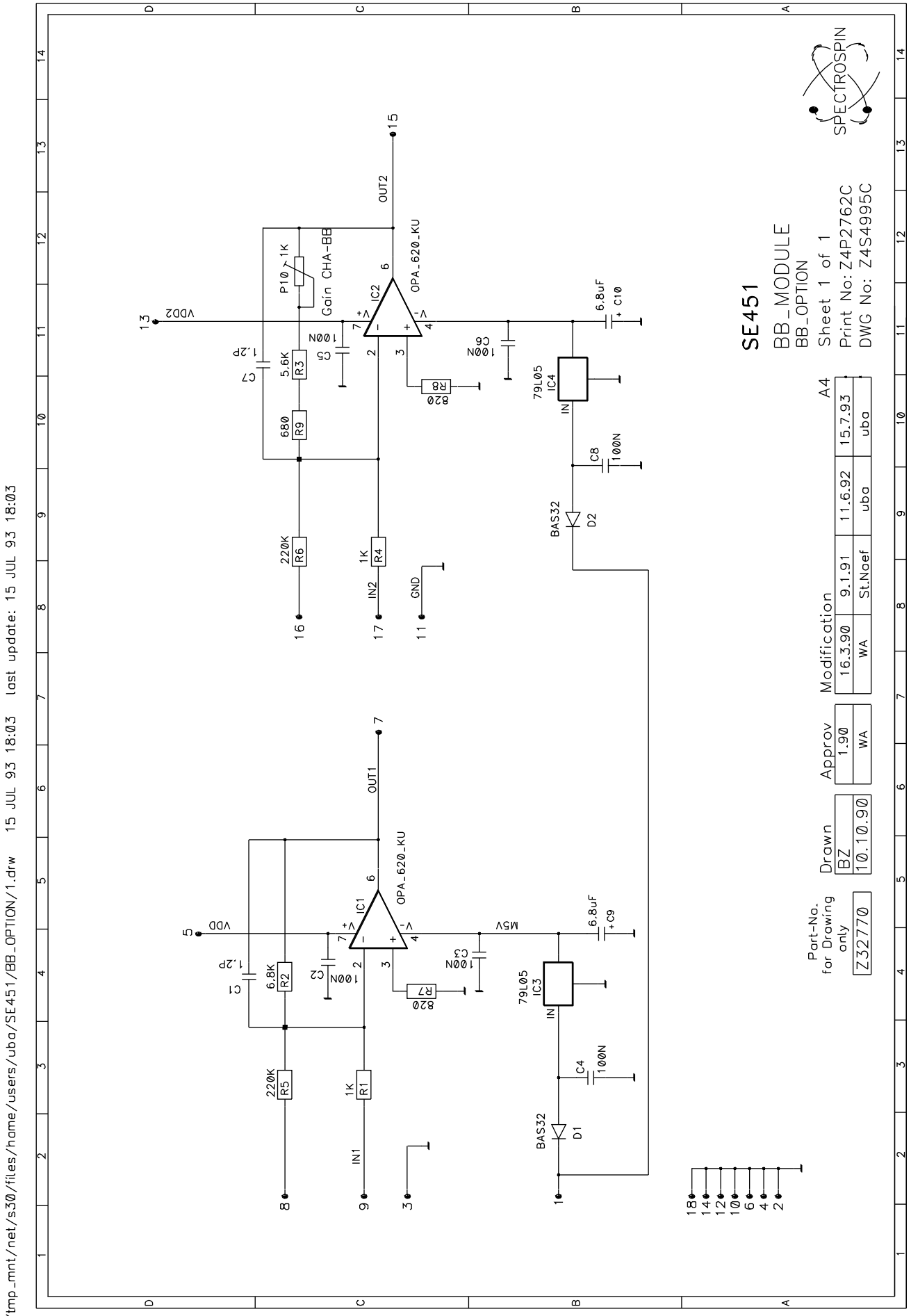
/files/home/users/ubo/se_451/RECEIVER/1.drw 16 JUN 92 16:27 last update: 16 JUN 92 16:25

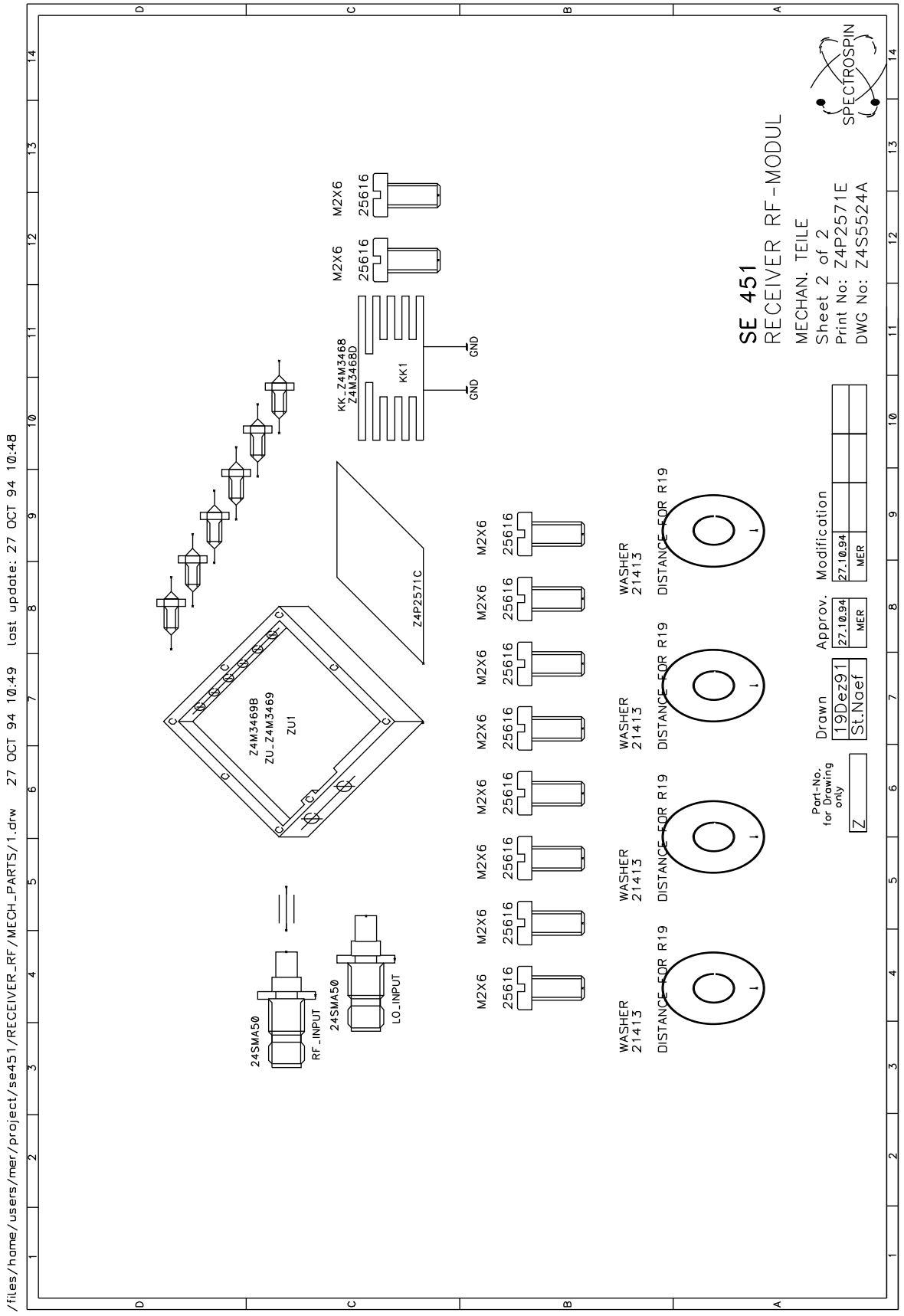


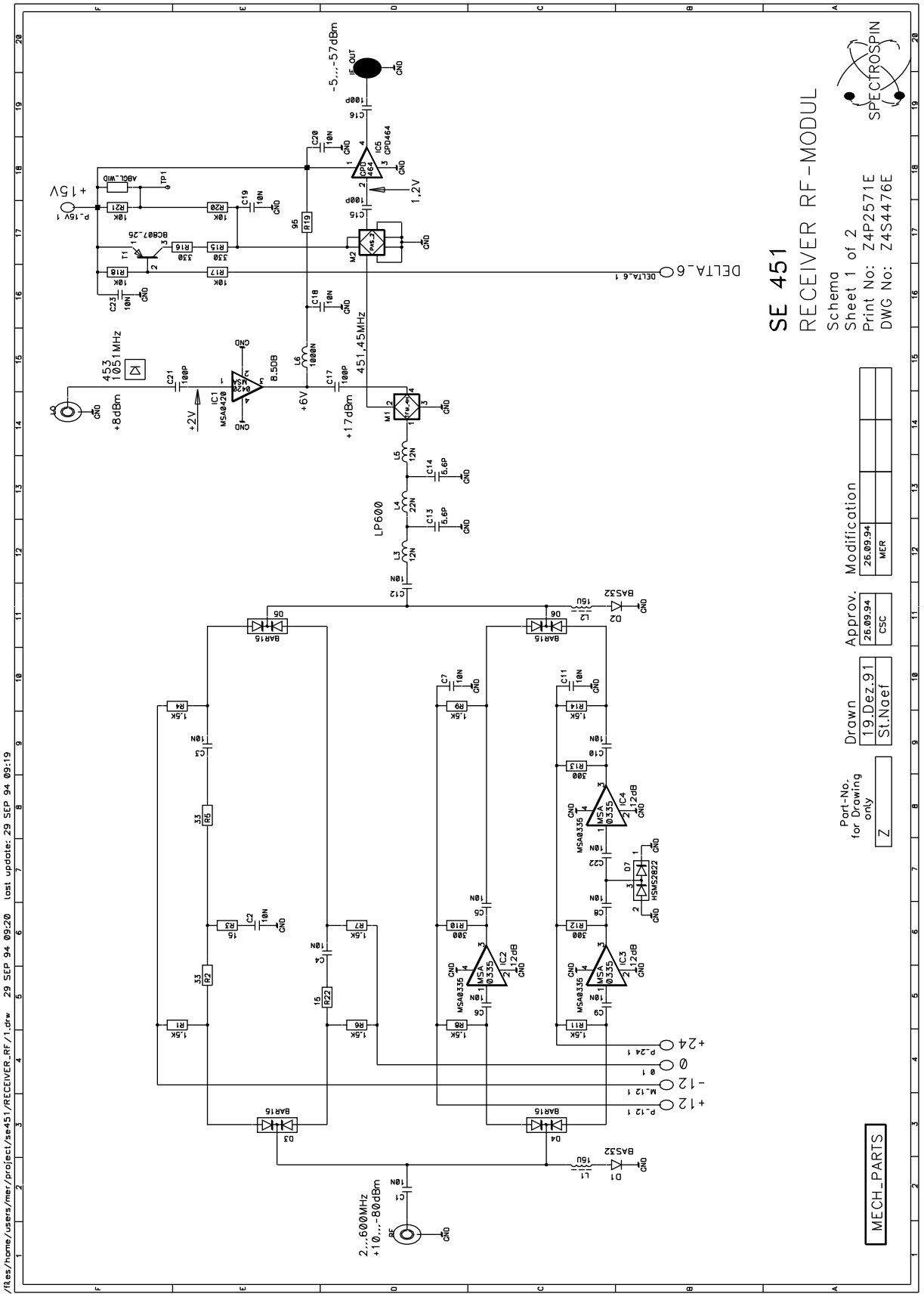
SE-451
BB-Option
Assembly Drawing
SHEET 1 OF 1
Print No : Z4P2762C
DWG No : Z4D4660A

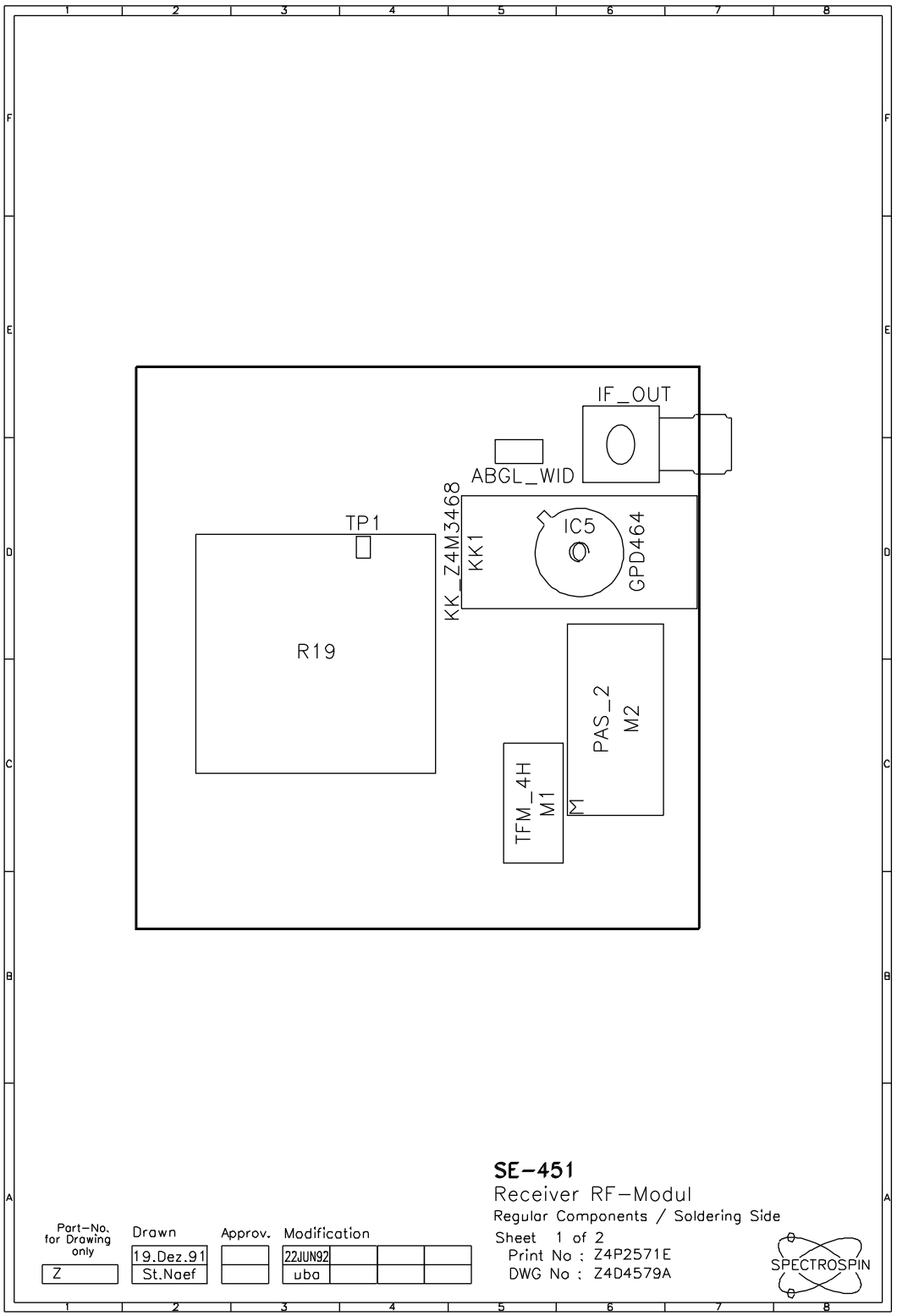
Part-No. for Drawing only	Drawn	Approv.	Modification			
Z32771	9.Jan.91 St.Naef		11.June92 uba	16.July92 uba		

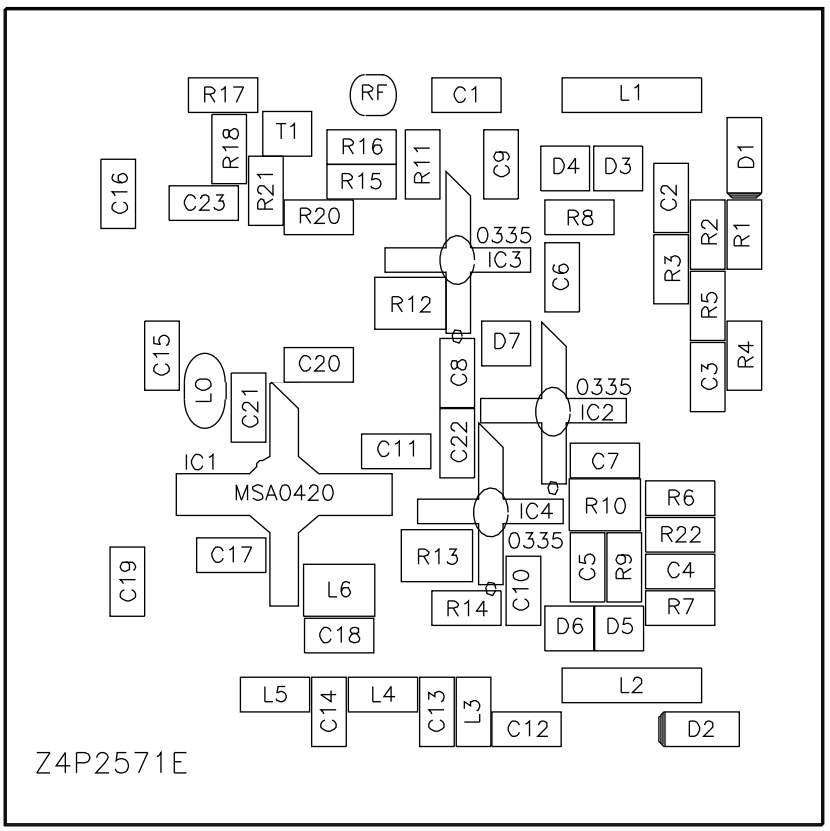
SPECTROSPIN


/tmp_mnt/net/s30/files/home/users/uba/SE451/BB_OPTION/1.drw 15 JUL 93 18:03 last update: 15 JUL 93 18:03
SE451
BB_MODULE
BB_OPTION
Sheet 1 of 1
Print No: Z4P2762C
DWG No: Z4S4995C
A4
SPECTROSPIN
Modification
16.3.90 WA
9.1.91 St.Naef
11.6.92 uba
15.7.93 uba
Drawn BZ 10.10.90
Approv 1.90 WA
Part-No. for Drawing only Z32770
VDD2
VDD
M5V
GND
IN1
IN2
OUT1
OUT2
IC1 OPA_620_KU
IC2 OPA_620_KU
IC3 79L05
IC4 79L05
P10 1K Gain CHA-BB
R1 1K
R2 6.8K
R3 5.6K
R4 1K
R5 220K
R6 220K
R7 820
R8 820
R9 680
C1 1.2P
C2 100N
C3 100N
C4 100N
C5 100N
C6 100N
C7 1.2P
C8 100N
C9 6.8uF
C10 6.8uF
D1 BAS32
D2 BAS32


/files/home/users/mer/project/se451/RECEIVER_RF/MECH_PARTS/1.drw 27 OCT 94 10:49 last update: 27 OCT 94 10:48
SE 451
RECEIVER RF-MODUL
MECHAN. TEILE
Sheet 2 of 2
Print No: Z4P2571E
DWG No: Z4S5524A
SPECTROSPIN
Drawn 19Dez91 St.Naef
Approv. 27.10.94 MER
Modification 27.10.94 MER
Part-No. for Drawing only Z
Z4M3469B ZU_Z4M3469 ZU1
Z4P2571C
KK_Z4M3468 Z4M3468D KK1
GND
GND
M2X6
25616
24SMA50
RF_INPUT
24SMA50
LO_INPUT
WASHER 21413
DISTANCE FOR R19


SE 451
RECEIVER RF-MODUL
Schema
Sheet 1 of 2
Print No: Z4P2571E
DWG No: Z4S4476E
SPECTROSPIN
Modification
26.09.94 MER
Approv. 26.09.94 CSC
Drawn 19.Dez.91 St.Noef
Part-No. for Drawing only
MECH_PARTS
/files/home/users/mer/project/se451/RECEIVER_RF/1.drw 29 SEP 94 09:20 last update: 29 SEP 94 09:19
-5...-57dBm
1,2V
+15V
DELTA_6
LP600
451,45MHz
453 1051MHz
+8dBm
+17dBm
+6V
+2V
2...600MHz +10...-80dBm
+24
0
-12
+12
MSA0335
HSMS2822
BAR15
BAS32
BC807-26
GPD464


IF_OUT
ABGL_WID
TP1
KK_Z4M3468
KK1
IC5
GPD464
R19
PAS_2
M2
TFM_4H
M1
SE-451
Receiver RF-Modul
Regular Components / Soldering Side
Sheet 1 of 2
Print No : Z4P2571E
DWG No : Z4D4579A
Part-No. for Drawing only
Z
Drawn
19.Dez.91
St.Naef
Approv.
Modification
22JUN92
uba
SPECTROSPIN



SE-451

Receiver RF-Modul

Assembly Drawing – SMD Components

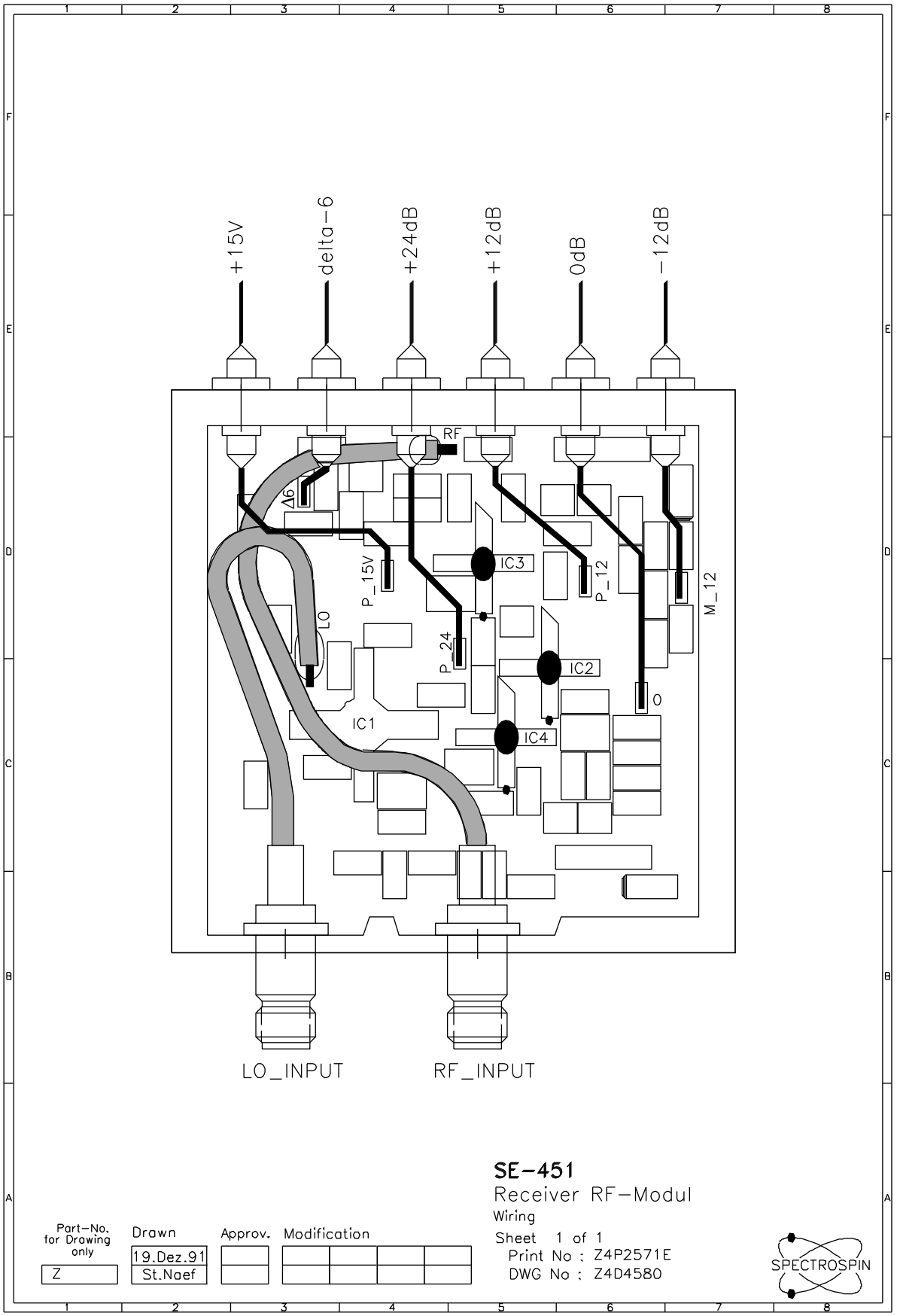
Sheet 2 of 2

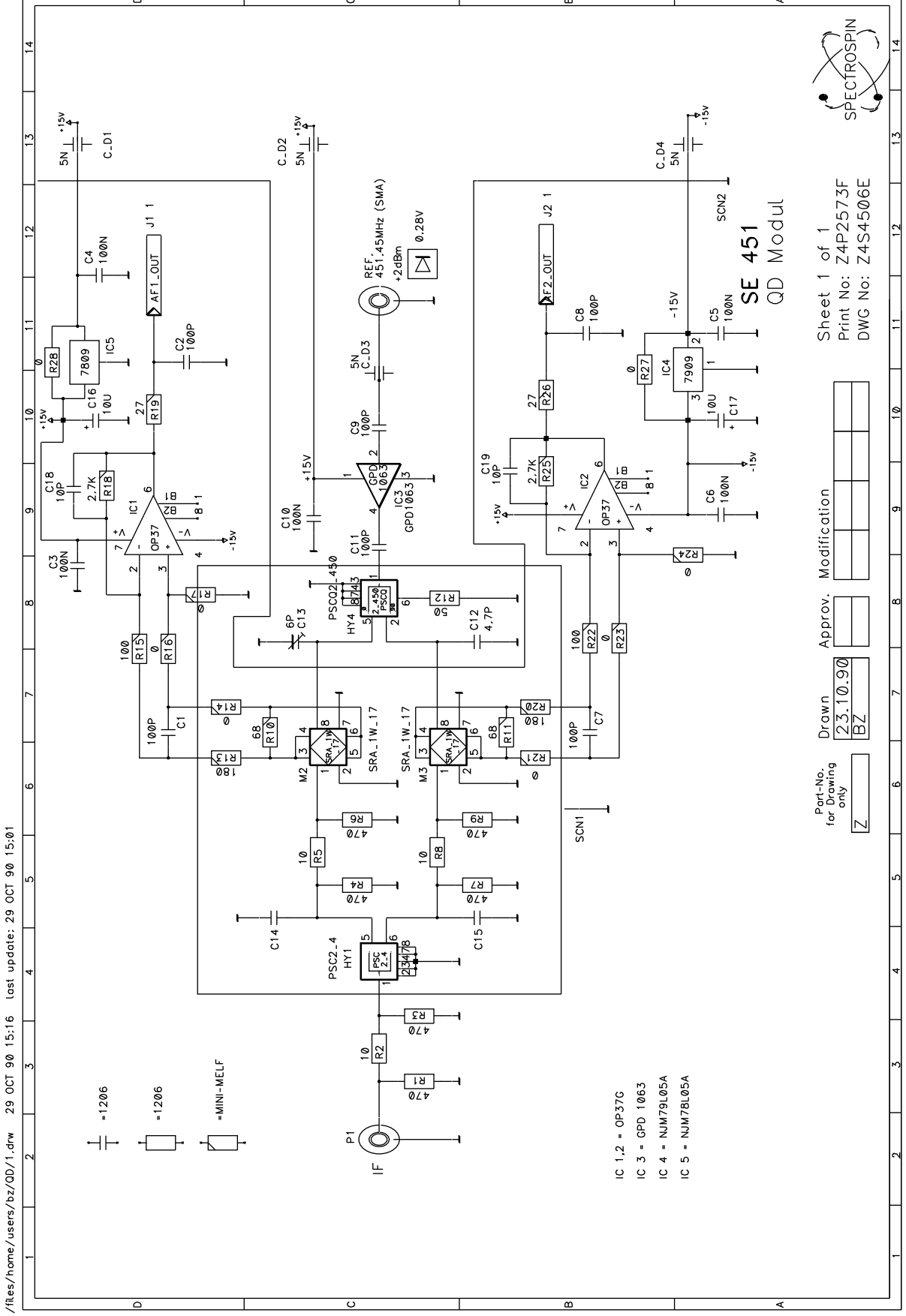
Print No : Z4P2571E

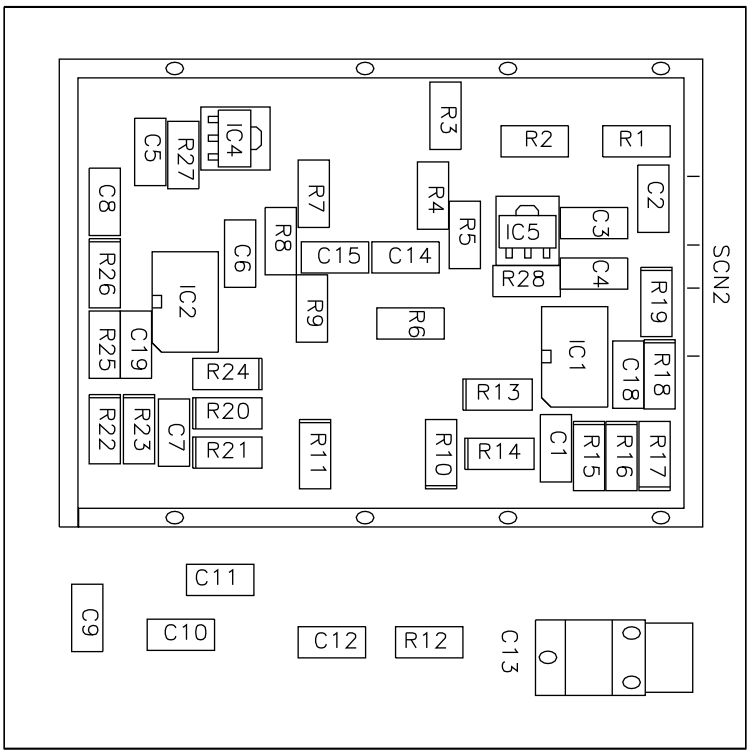
DWG No : Z4D4574A

SPECTROSPIN

Part-No. for Drawing only	Drawn	Approv.	Modification
Z	19.Dez.91 St.Naef	29.09.94 CSC	29.09.94 MER


+15V
delta-6
+24dB
+12dB
0dB
-12dB
RF
Δ6
P_15V
IC3
P_12
M_12
LO
P_24
IC2
0
IC1
IC4
LO_INPUT
RF_INPUT
SE-451
Receiver RF-Modul
Wiring
Sheet 1 of 1
Print No : Z4P2571E
DWG No : Z4D4580
Part-No. for Drawing only
Z
Drawn
19.Dez.91
St.Naef
Approv.
Modification
SPECTROSPIN


SE 451
QD Modul
Sheet 1 of 1
Print No: Z4P2573F
DWG No: Z4S4506E
SPECTROSPIN
Drawn
23.10.90
BZ
Approv.
Modification
Part-No. for Drawing only
Z
IC 1,2 = OP37G
IC 3 = GPD 1063
IC 4 = NJM79L05A
IC 5 = NJM78L05A
-1206
-1206
-MINI-MELF
/files/home/users/bz/QD/1.drw 29 OCT 90 15:16 last update: 29 OCT 90 15:01

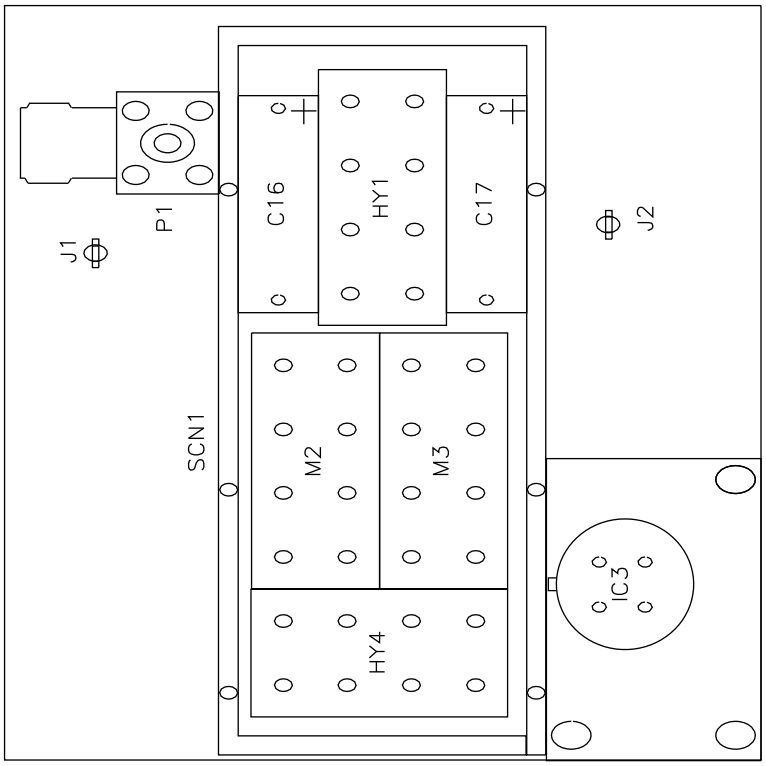


SE451
QD Modul
Bestueckungsplan

Part-No. for Drawing only	Drawn	Approv.	Modification
Z	21.11.90 BZ		

Print No : Z4P2573F
DWG No : Z4D4218

SPECTROSPIN



HYBRID–SEITE

SE451
QD Modul
Bestueckungsplan

Part–No. for Drawing only	Drawn	Approv.	Modification
Z	21.11.90 BZ		

Print No : Z4P2573F
DWG No : Z4D4219

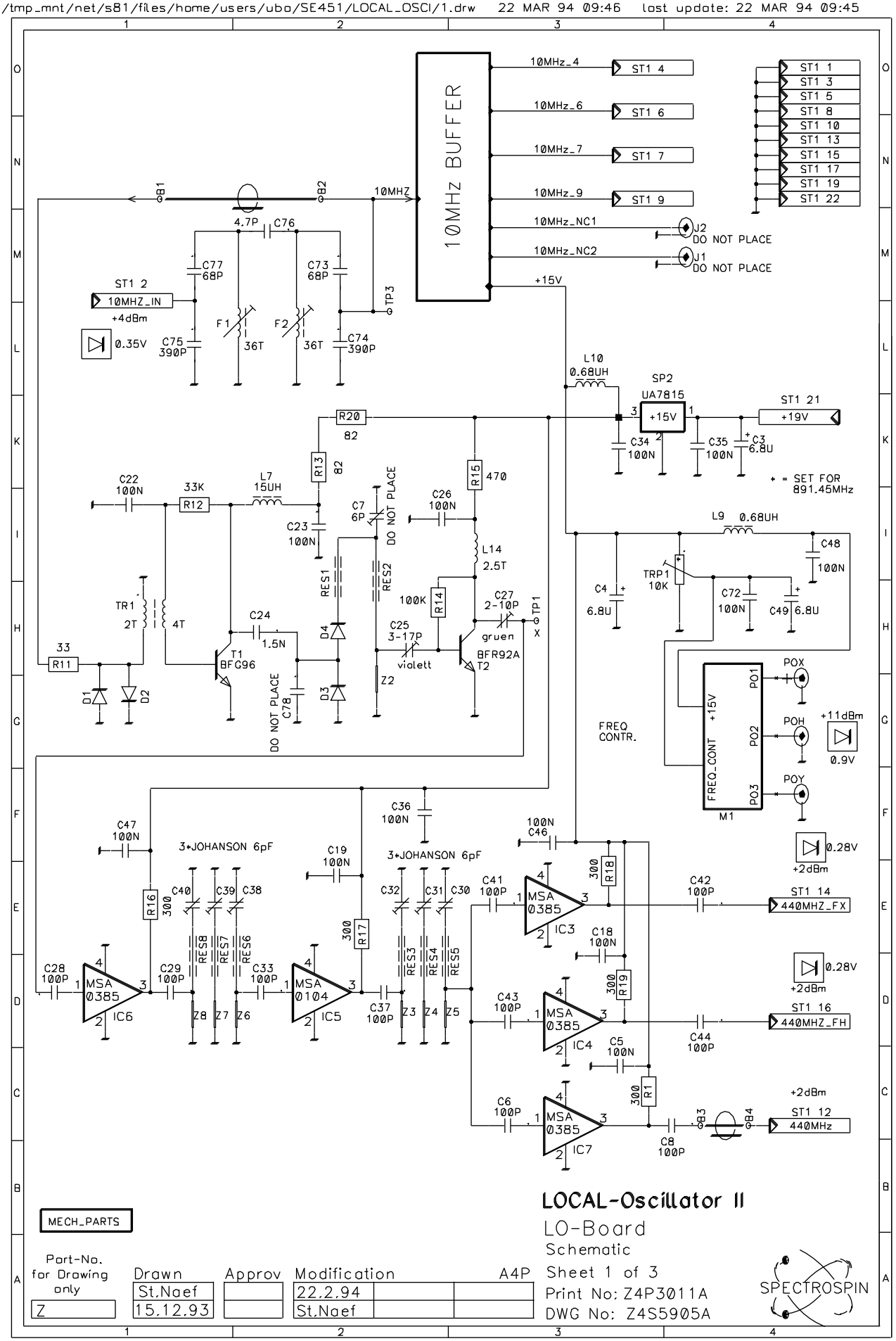
SPECTROSPIN

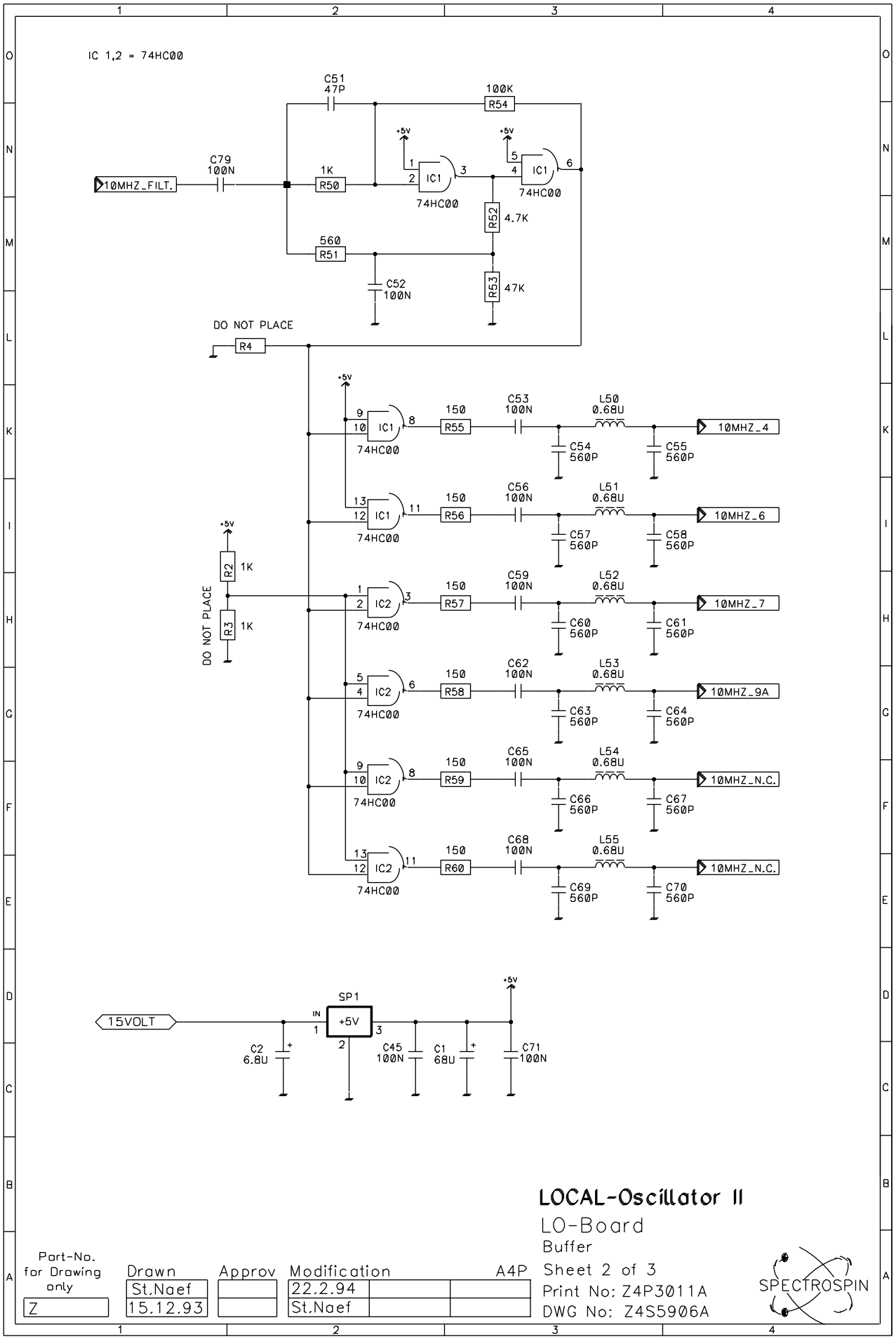
Schematics LO-Board II 15

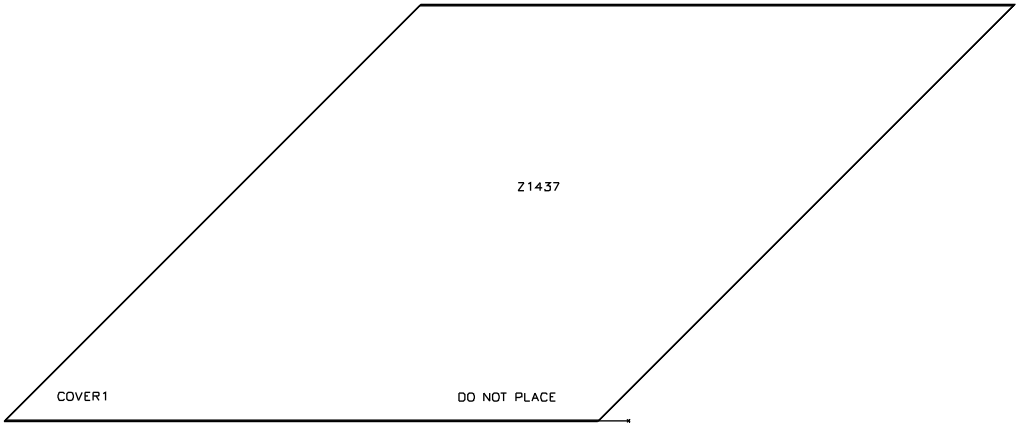
Schematics and Assembly 15.1

On the following pages you will find the schematics of the Local Oszillator Board II (Z4P3011A) including the SAW-Oszillator (Z4P3024).

The SAW-Oszillator itself contains the Oszillator (Z4P3000A), the Driver (Z4P3001A) and the 3rd Output (Z4P2998A).


10MHz BUFFER
10MHz_4
10MHz_6
10MHz_7
10MHz_9
10MHz_NC1
10MHz_NC2
+15V
ST1 4
ST1 6
ST1 7
ST1 9
ST1 1
ST1 3
ST1 5
ST1 8
ST1 10
ST1 13
ST1 15
ST1 17
ST1 19
ST1 22
J2
DO NOT PLACE
J1
DO NOT PLACE
10MHZ
B1
B2
4.7P
C76
C77
68P
C73
68P
TP3
ST1 2
10MHZ_IN
+4dBm
0.35V
C75
390P
F1
36T
F2
36T
C74
390P
L10
0.68UH
SP2
UA7815
+15V
ST1 21
+19V
C34
100N
C35
100N
C3
6.8U
* = SET FOR
891.45MHz
R20
82
R13
82
R15
470
C22
100N
33K
R12
L7
15UH
C23
100N
C7
6P
DO NOT PLACE
C26
100N
L14
2.5T
RES1
RES2
100K
R14
C27
2-10P
gruen
C25
3-17P
violett
Z2
TP1
X
BFR92A
T2
TR1
2T
4T
C24
1.5N
T1
BFG96
33
R11
D1
D2
D4
D3
C78
DO NOT PLACE
L9
0.68UH
C48
100N
TRP1
10K
C4
6.8U
C72
100N
C49
6.8U
FREQ
CONTR.
FREQ_CONT
+15V
PO1
PO2
PO3
M1
POX
POH
POY
+11dBm
0.9V
C36
100N
C47
100N
3*JOHANSON 6pF
C19
100N
3*JOHANSON 6pF
C46
100N
0.28V
+2dBm
R16
300
C40
C39
C38
RES8
RES7
RES6
R17
300
C32
C31
C30
RES3
RES4
RES5
C41
100P
MSA
0385
IC3
R18
300
C42
100P
ST1 14
440MHZ_FX
C18
100N
C28
100P
MSA
0385
IC6
C29
100P
Z8
Z7
Z6
C33
100P
MSA
0104
IC5
C37
100P
Z3
Z4
Z5
C43
100P
MSA
0385
IC4
R19
300
0.28V
+2dBm
ST1 16
440MHZ_FH
C5
100N
C44
100P
C6
100P
MSA
0385
IC7
R1
300
C8
100P
B3
B4
+2dBm
ST1 12
440MHz
LOCAL-Oscillator II
LO-Board
Schematic
Sheet 1 of 3
Print No: Z4P3011A
DWG No: Z4S5905A
MECH_PARTS
Part-No.
for Drawing
only
Z
Drawn
St.Naef
15.12.93
Approv
Modification
22.2.94
St.Naef
A4P
SPECTROSPIN


IC 1,2 = 74HC00
C51
47P
100K
R54
C79
100N
10MHZ_FILT.
1K
R50
IC1
74HC00
+5V
R52
4.7K
560
R51
C52
100N
R53
47K
DO NOT PLACE
R4
150
C53
100N
L50
0.68U
10MHZ_4
C54
560P
C55
560P
C56
L51
10MHZ_6
C57
C58
R2
R3
1K
DO NOT PLACE
IC2
C59
L52
10MHZ_7
C60
C61
C62
L53
10MHZ_9A
C63
C64
C65
L54
10MHZ_N.C.
C66
C67
C68
L55
10MHZ_N.C.
C69
C70
15VOLT
SP1
IN
C2
6.8U
C45
100N
C1
68U
C71
100N
LOCAL-Oscillator II
LO-Board
Buffer
Sheet 2 of 3
Print No: Z4P3011A
DWG No: Z4S5906A
Part-No. for Drawing only
Z
Drawn
St.Naef
15.12.93
Approv
Modification
22.2.94
St.Naef
A4P
SPECTROSPIN



21421
l=165mm
LTG SEMI-RIGID

21421
l=45mm
LTG SEMI-RIGID

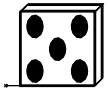
20438
FERRIT_PERLE

20438
FERRIT_PERLE

WIRE
20695
30cm
LTG DRAHT Ø,7mm

SCHLAUCH
21530
SCHLAUCH PTFE

ZUB_UNTERLAGE
21413
TRANS ZUB UNTERL.



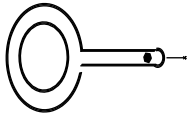
ZUB_UNTERLAGE
21413
TRANS ZUB UNTERL.

ZUB_UNTERLAGE
21413
TRANS ZUB UNTERL.

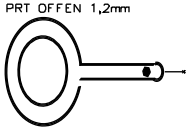
FIDU1 FIDU2 FIDU3

LOETBUEGEL

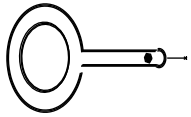
VERDR
20707
GESCH M3x18
VERDR LOETOESE



VERDR
21323
1,2mm
PRT OFFEN 1,2mm



VERDR
21323
1,2mm
PRT OFFEN 1,2mm



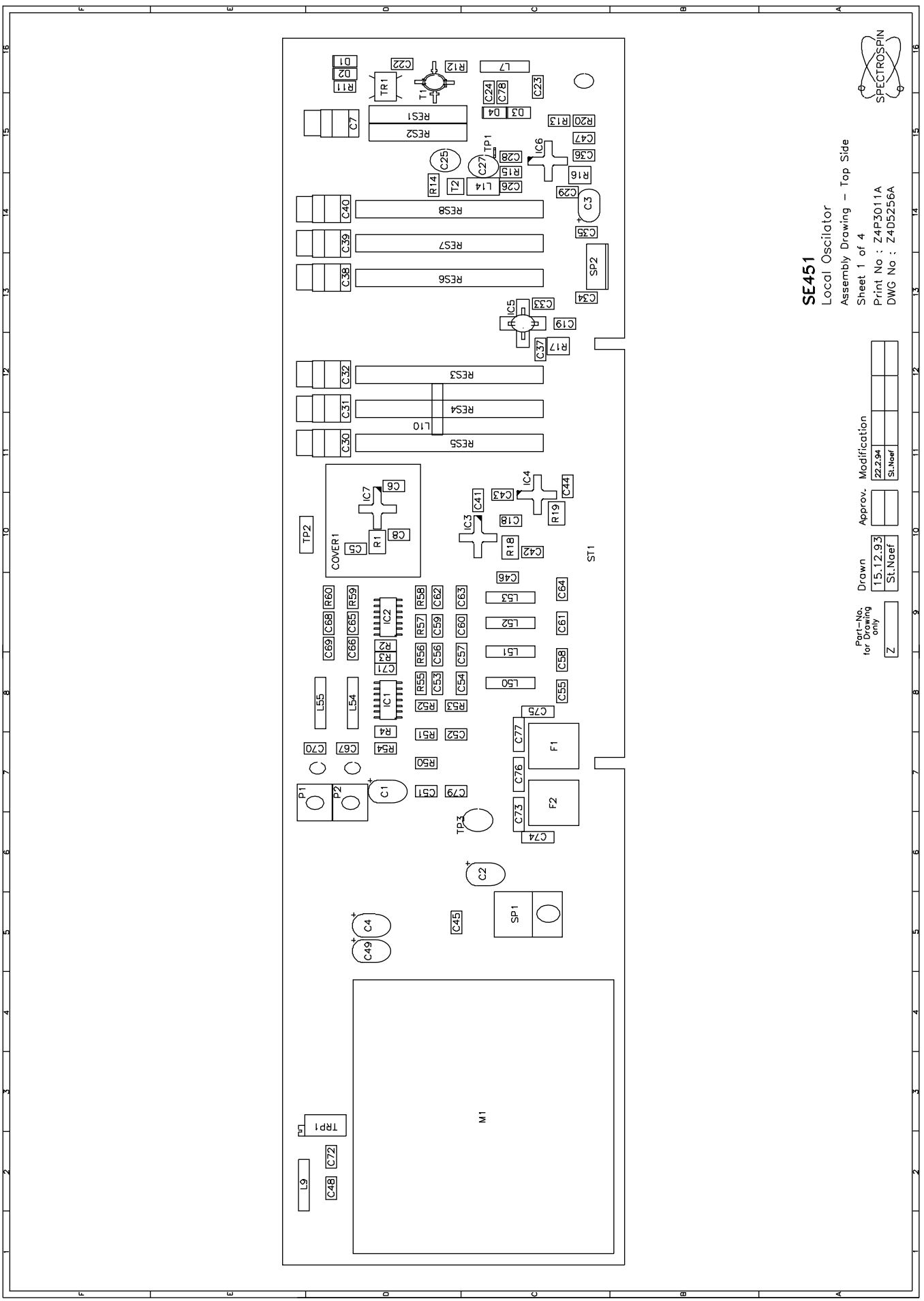
Part-No. for Drawing only	Drawn	Approv.	Modification				A3
Z	St.Naef 15.12.93		22.2.94 St.Naef				

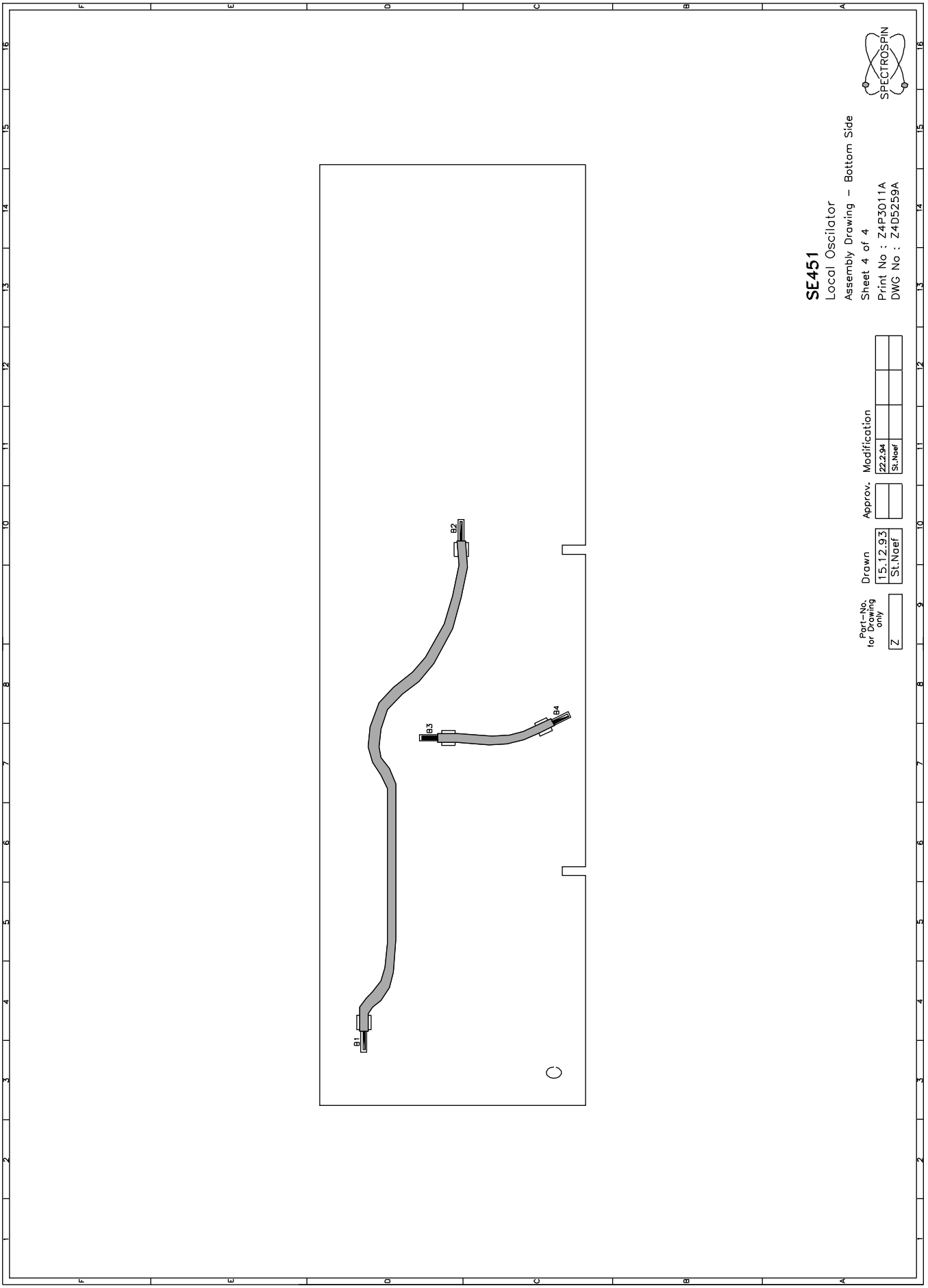
SE451

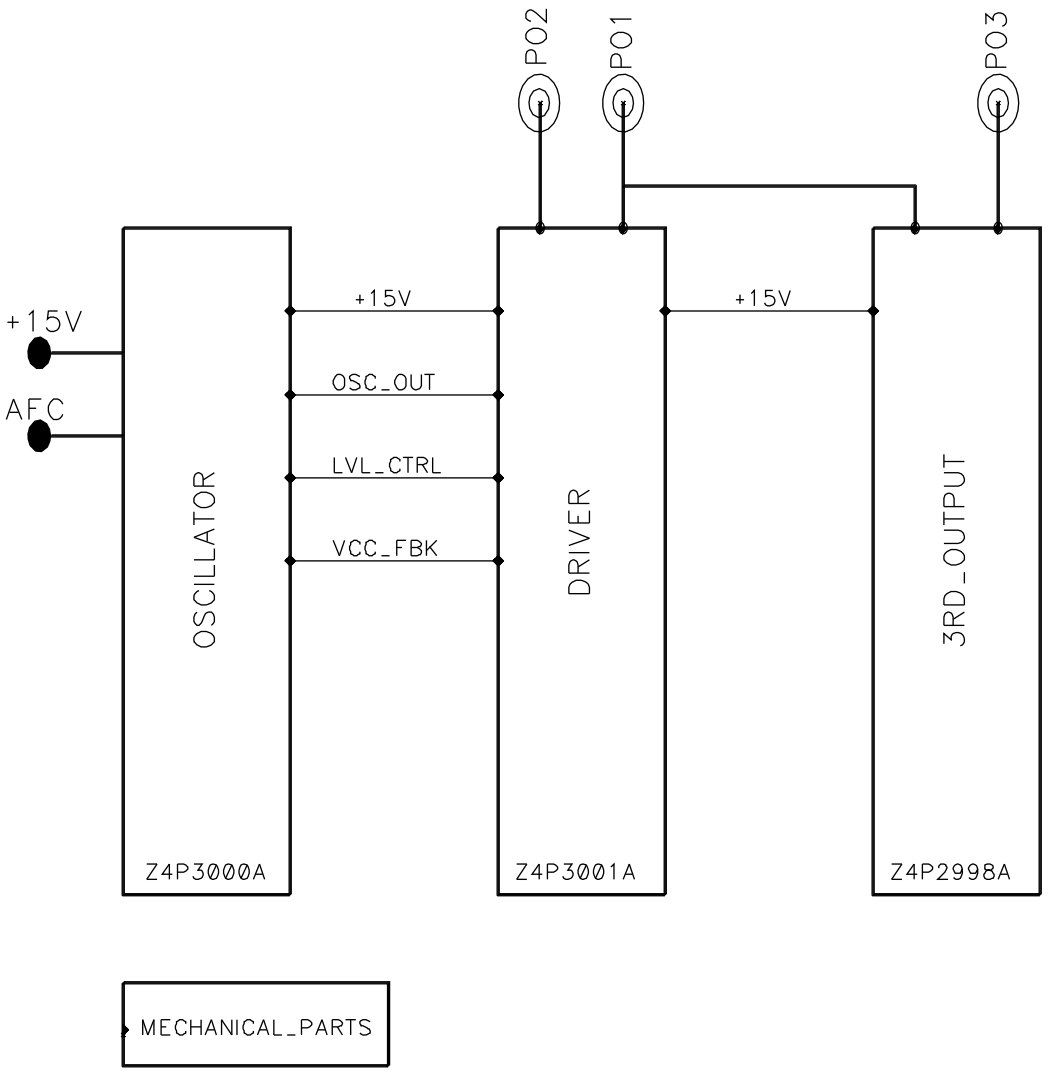
Local-Oscillator II

Mechanical-Parts
Sheet 3 of 3
Print No: Z4P3011A
DWG No: Z4S5907A

SPECTROSPIN


SE451
Local Oscilator
Assembly Drawing – Top Side
Sheet 1 of 4
Print No : Z4P3011A
DWG No : Z4D5256A
SPECTROSPIN
Modification
Approv.
Drawn
15.12.93
St.Naef
Part-No. for Drawing only
Z
TR1
T1
T2
IC1
IC2
IC3
IC4
IC5
IC6
IC7
TP1
TP2
TP3
COVER1
ST1
M1
TRP1
SP1
SP2
F1
F2
L10
L54
L55


SPECTROSPIN
SE451
Local Oscilator
Assembly Drawing – Bottom Side
Sheet 4 of 4
Print No : Z4P3011A
DWG No : Z4D5259A
Modification
Approv.
Drawn
15.12.93
St.Naef
Part-No. for Drawing only
Z
B1
B2
B3
B4
C



SE 451 3-CHANNEL

SAW-Oscillator

Top Sheet

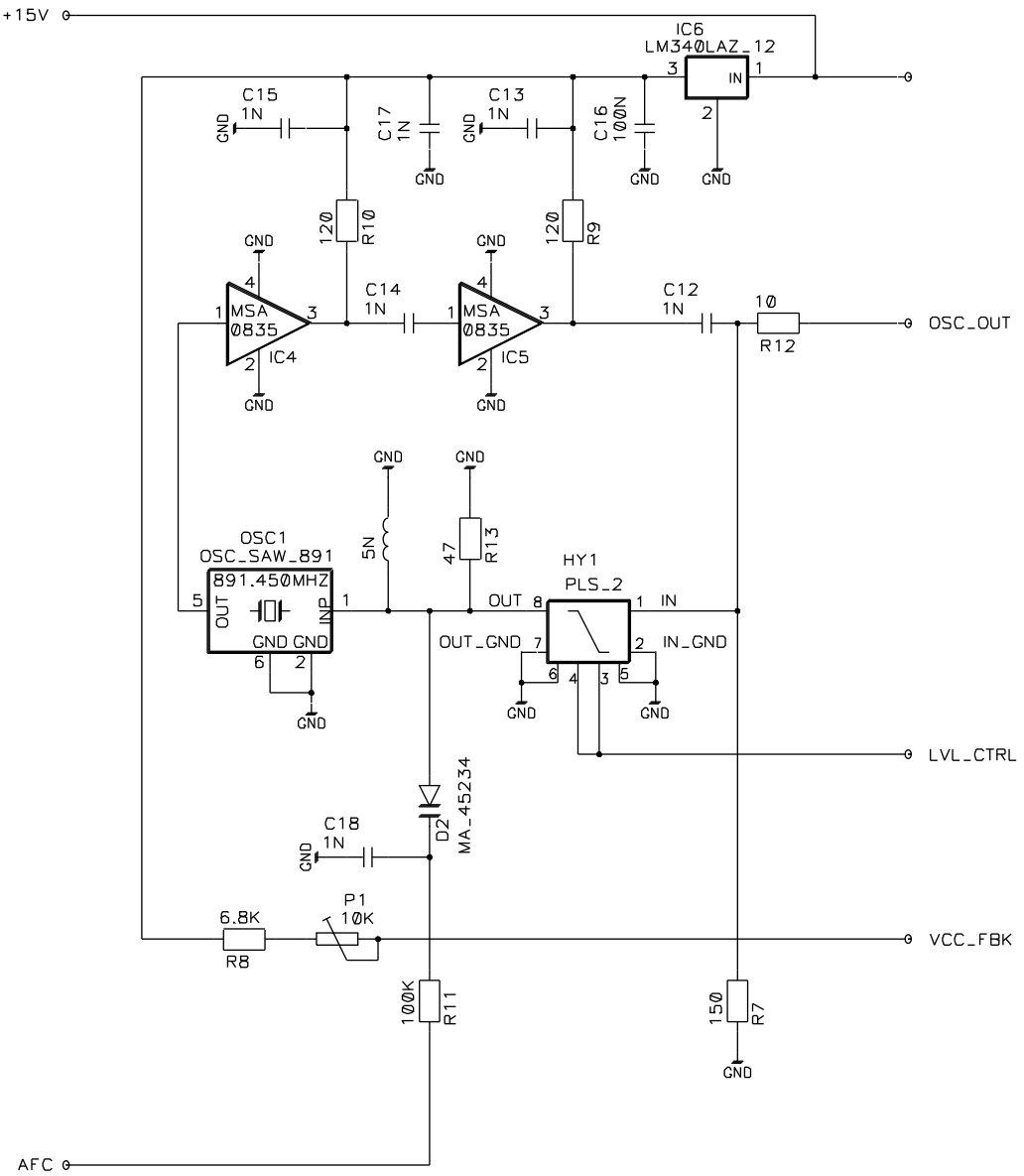
Sheet 1 of 2

Print No: Z4P3024

DWG No: Z4S5871A

Part-No. for Drawing only	Drawn	Approv	Modification		A4P
Z	St.Naef		uba		
	7.12.93		4.3.94		

SPECTROSPIN



OSC_MECH_PARTS

Part-No. for Drawing only: Z

Drawn	Approv	Modification	A4P
St.Naef 7.12.93			

SE451 3-CHANNEL

SAW-Oscillator

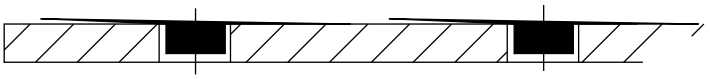
Oscillator Part

Sheet 1 of 2

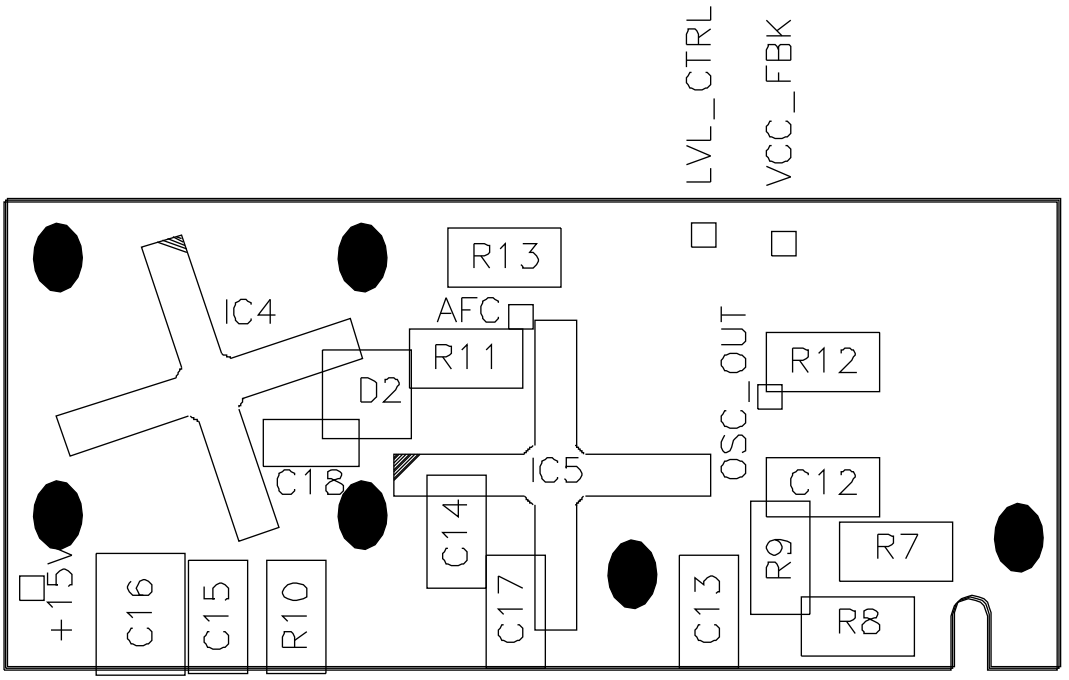
Print No: Z4P3000A

DWG No: Z4S5867

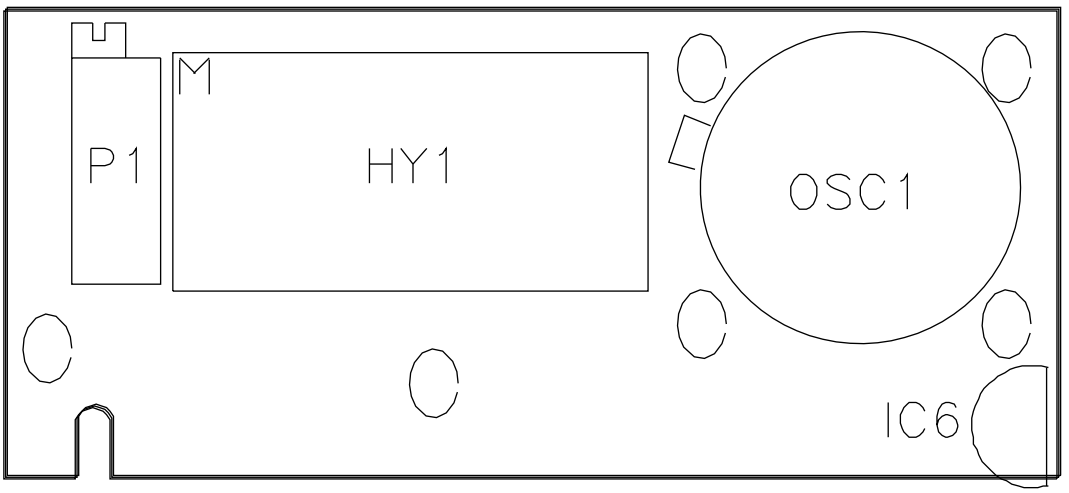
SPECTROSPIN



Koerper des MSA im Print versenken



Top side



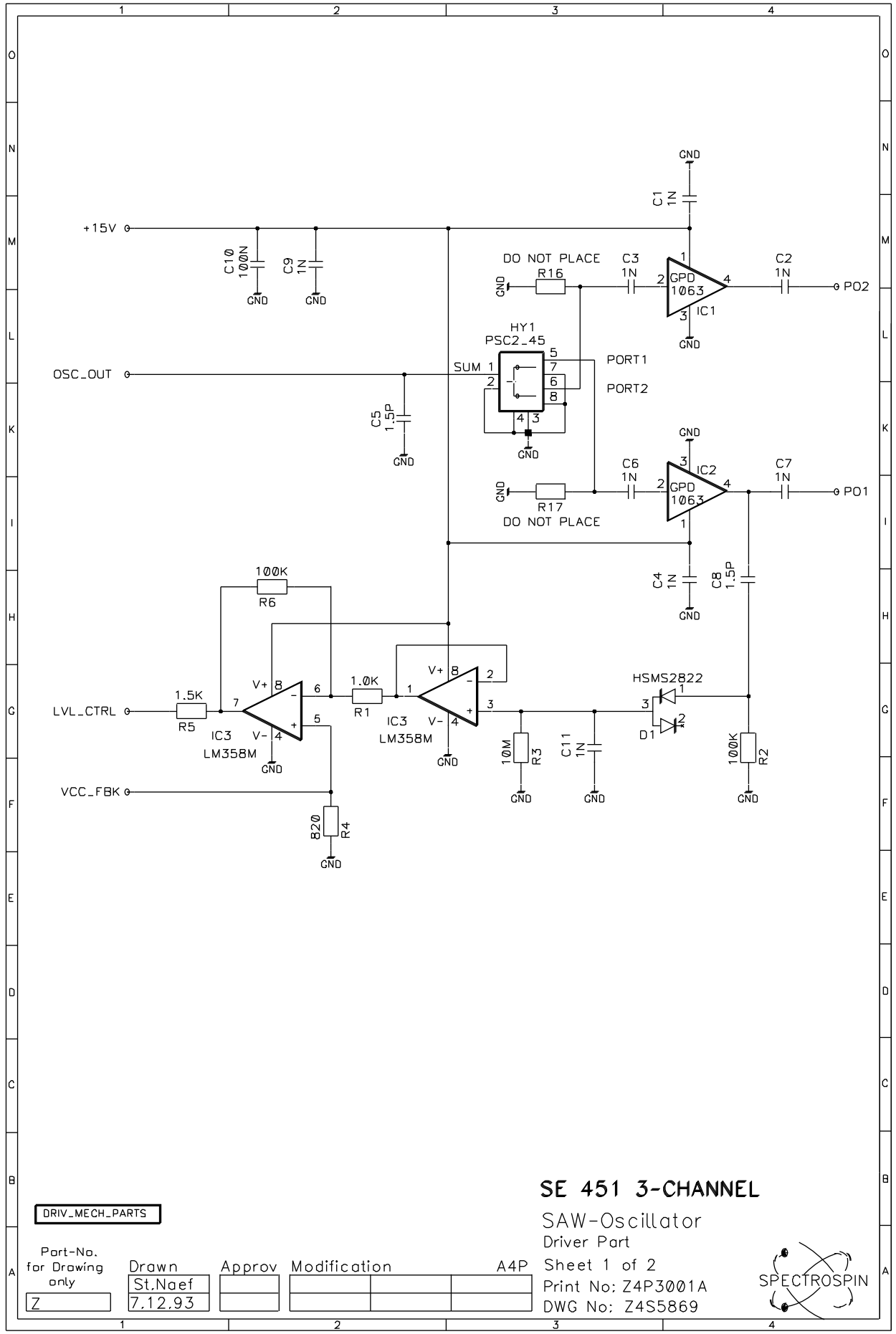
Bottom side

SE451 3-CHANNEL
Oscillator
Assembly Drawing

Part-No. for Drawing only	Drawn	Approv.	Modification
Z	9.Dez.93 St.Naef		18.3.94 uba

Print No : Z4P3000A
DWG No :

SPECTROSPIN



DRIV_MECH_PARTS

Part-No. for Drawing only: Z

Drawn	Approv	Modification	A4P
St.Naef 7.12.93			

SE 451 3-CHANNEL

SAW-Oscillator

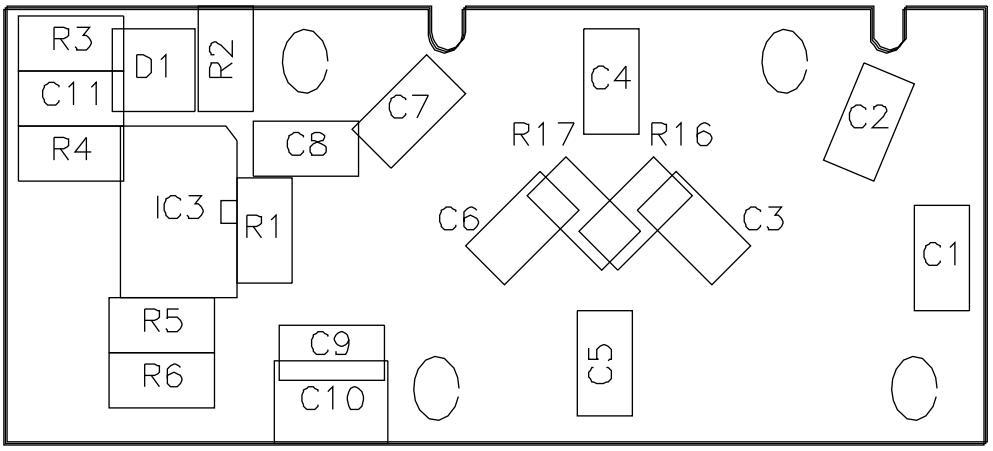
Driver Part

Sheet 1 of 2

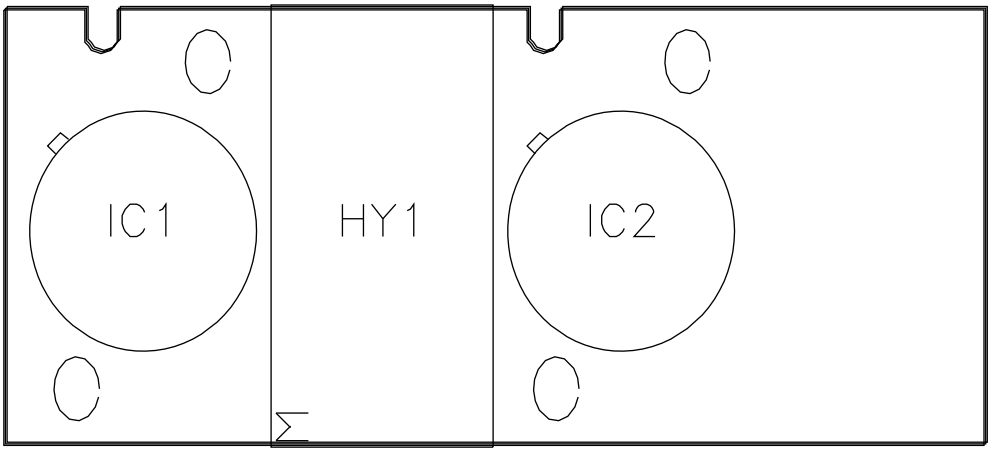
Print No: Z4P3001A

DWG No: Z4S5869

SPECTROSPIN



Top side



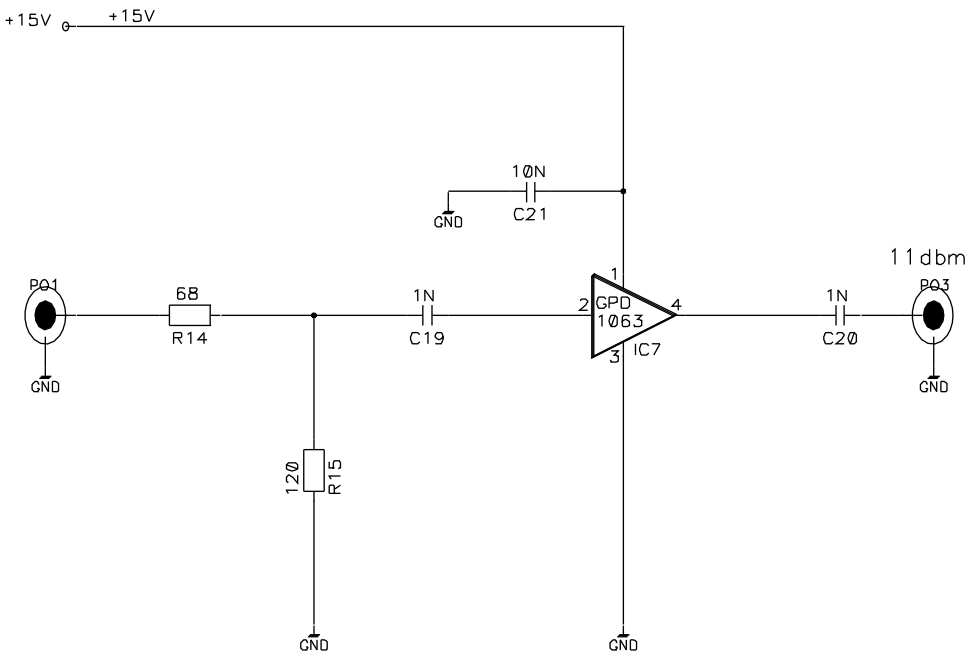
Bottom side

SE451 3-CHANNEL
Driver
Assembly Drawing

Part-No. for Drawing only	Drawn	Approv.	Modification
Z	9.Dez.93 St.Naef		18.3.94 uba

Print No : Z4P3001A
DWG No :

SPECTROSPIN



SE451 3-CHANNEL

SAW-Oscillator

3rd Output

3RD_MECH_PARTS

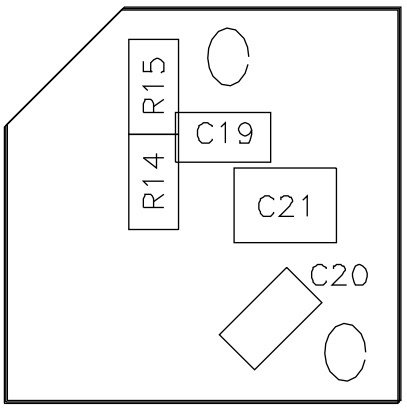
Part-No. for Drawing only	Drawn	Approv	Modification	A4P
Z	St.Naef 7.12.93			

Sheet 1 of 2

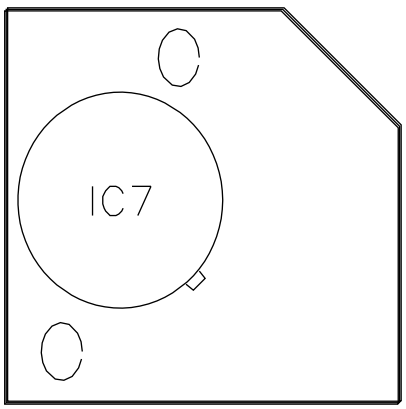
Print No: Z4P2998A

DWG No: Z4S5847

SPECTROSPIN



Top side



Bottom side

SE451 3-CHANNEL
3RD-Output
Assembly Drawing

Part-No. for Drawing only	Drawn	Approv.	Modification
Z	7.Dez.93 St.Naef		18.3.94 uba

Print No : Z4P2998A
DWG No :

SPECTROSPIN

SE451_DECKEL
Z1925
Z4M4012A
SE-451_DECKEL

SE451_DECKEL
Z12604
Z4M7712
SE-451_DECKEL

SCHILD_PL_KLAR

SCHILD_SAW-OSCI

SCREW_COUNT_SINK
28444
M2,5x6
SENKSCHR_KR

SCREW_CYL_HEAD
25616
M2x6
ZYLINDERSCHR_KR

SCREW_CYL_HEAD
25632
UNF10-32x1/4"
ZYLINDERSCHRAUBE

VERDR_DURCHFUEHRUNG
21578
093/093P

HF-DICHTUNG
Z12370
31mm

KOND-Durchfuehr'g
21434
PI_FILTER

ST_KOAX_ADAPT
SMA-I_BU-BU
34SMA

ST_KOAX
SMA-SFT G LOET
UT85

WASHER
21574
SMA_U-SCH
UNTERLAGSCHEIBE

21576
SMA SFT G
ST_KOAX_TESTPIN

Z2M4011H
SE451_GEHAEUSE

KOAX SUCOFORM 86
KOAXKABEL_SUCO-FORM-86
l=95mm
KOAXKABEL_SEMI-RIGID_GELOETET

20894
FERRIT_PERLE

KOAX SUCOFORM 86
KOAXKABEL_SUCO-FORM-86
l=30mm
KOAXKABEL_SEMI-RIGID_GELOETET

21572
FERRIT_PERLE

Z12601
Z4P2998A
PRINT 3RD-OUTPUT

Z12602
Z4P3000A
PRINT 891MHZ-OSCI

Z12603
Z4P3001A
PRINT DRIVER

TREAD_PIN
28442
M2,5x6
GEWINDESTIFT

WIRE
21706
l=51mm
WIRE-WARP ROT

WIRE
20695
50cm
LTG DRAHT Ø,7mm

WIRE
21707
l=51mm
WIRE-WARP BLAU

Se451 3-CHANNEL

SAW Oscillator

Mechanical-Parts
Sheet 2 of 2
Print No: Z4P3024
DWG No: Z4S5872A

Part-No. for Drawing only	Drawn	Approv.	Modification				A3
Z	St.Naef		uba				
	24.11.93		4.3.94				

SPECTROSPIN

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3.Motherboard Z4P2997 **17**

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