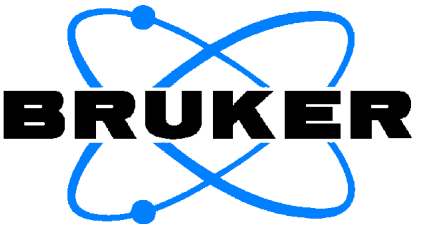

AQR / AQS

SADC Technical Manual

Version 004

BRUKER

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General Description 1

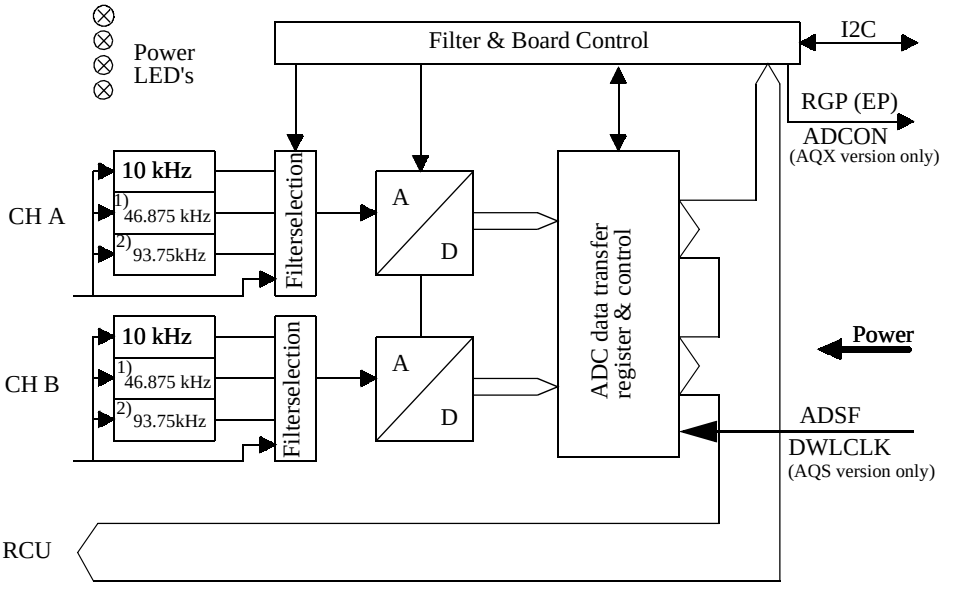
Introduction 1.1

The present analog to digital converter board, called Standard ADC (SADC), is a 16 Bit system for low spectral width (5 kHz) and 14 Bit for the whole specified spectral width of 150 kHz. Because of quadrature detection method in NMR, this system is composed of 2 identical channels. Each channel has an own antialiasing filterbank and AD converter, so no switching between channel A and B is necessary. The throughput rate for each channel is 150 kSPS, resulting in a total of 300 kSPS and allowing oversampling techniques. Therefore only a reduced set of antialiasing filters are required.

Functional description 1.2

In the following a short overview over the SADC is given.

Figure 1.1. Block Diagram SADC



1) 45KHz up to ECL03 (AQR_type) 2) 62.5KHz up to ECL03(AQR_type)

The converter system has two channels (CHA&CHB), which in NMR represent the same FID (Free Induction Decay) signal, one as real (CHA) and one as imaginary (CHB). This is due to the quadrature detection method. These signals pass each a four pole Butterwoth-Filter with cutoff frequencies of 10 kHz, 46.875 kHz or 93.75kHz (45kHz and 62.5kHz up to ECL03). These filters are used to eliminate

noise and to prevent from aliasing of signals over the nyquist frequency. If needed, there exists the possibility to bypass the filter in order to install a external filter or to use the filter characteristic of the receiver.

After being filtered, the signal is converted by an analog to digital converter (ADC). It converts the analog signal into a digital signal with 16 bits resolution. The full analog signal input range is +/-5V and the throughput rate for each channel is 150 kSPS. Even that the ADC has 16 Bit digital resolution, its spurious free dynamic specification is not true 16 Bit over the full spectral width. Thatfor it is qualified as 14 Bit ADC over the full spectral width. For small spectral width (i.e. 5kHz) the 16 Bit resolution can be achieved. The start of the conversion is determined by rising edge of the Dwell-Clock (DWCLK) from the data acquiring unit (DAU). In ‘qsim’ mode the system works in simultaneous quadrature-mode, this means both channels are holding and converting simultaneously. In the single-mode or quadrature-off (‘qf’) mode, only channel A converts. The ‘alternating’ mode also know as ‘sequential’ mode is not possible.

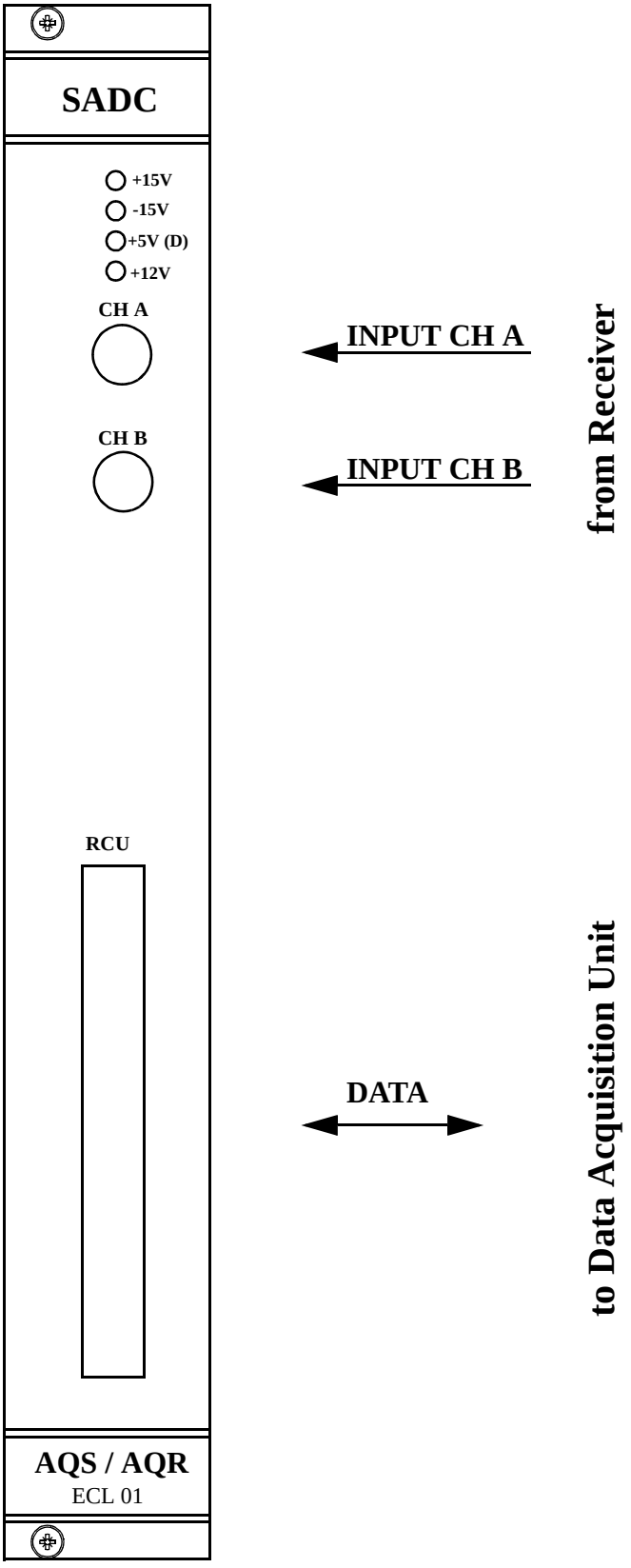
After the conversion stage the data will be latched into a memory (D-flip-flop) to remain until the data can be transferred to the DAU. This transfer is overlapping the next conversation started with the next Dwell clock. In fact the data transfer is changed from 32 Bits (2x16 bits) into 4x8 Bits. The first byte is the low byte of channel A, the second byte the high byte from channel A. In quadrature mode the channel B is tranferred in the same manner following the channel A data.

For the control purpose an I2C bus (Philips) is implemented. Either the DAU or the Receiver (with restriction) can control this bus. Via this bus the SADC can be reseted, the antialiasing filter can be selected and the acquisitions mode is set. All these settings are coupled to the acquisition software (i.e. in UXNMR FW = filter-width and AQMode = QSIM ‘simultaneous acquisition’).

The SADC is located in a rf cage showing at the front end the channel A & B input, the DAU interface connector and the power led’s. At the rear there is only a connector suitable for the AQR and AQR/P (ADC slot) or AQS rack. The power is primarly drawn from the AQR or the AQS rack.

Board	Compatibility
SADC AQR	only AQR Systems
SADC AQS	AQR and AQS Systems (auto detection)

Figure 1.2. Front view of SADC



Connectors *1.3*

Table 1.1. DAU-SADC Connector

J1	Signal-Name	J1	Signal-Name	J1	Signal-Name
1	VPWRGND	18	DATA 6~	35	TU0IN
2	VPWRGND	19	DATA 7	36	TU0IN~
3	DATA 0	20	DATA 7~	37	XVDD 12
4	DATA 0~	21	VPWRGND	38	XVDD 12
5	DATA1	22	VPWRGND	39	DWCLKIN
6	DATA 1~	23	DST 1	40	DWCLKIN~
7	DATA 2	24	DST 1~	41	VPWRGND
8	DATA 2~	25	UNIT 0	42	VPWRGND
9	DATA 3	26	UNIT 0~	43	ADC IN
10	DATA 3~	27	SRT 1	44	
11	XVDD 12	28	SRT 1~	45	SDATA IN
12	XVDD 12	29	RES RT	46	SDATA IN~
13	DATA 4	30	RES RT~	47	SERCLK
14	DATA 4~	31	XVDD 12	48	SERCLK~
15	DATA 5	32	XVDD 12	49	SERDIR
16	DATA 5~	33	EP IN	50	SERDIR~
17	DATA 6	34	EP IN~		

Table 1.2. AQR-SADC Connector

J 6	A	B	C
1			
2			
3			
4			
5			
6	SDA 1		SCL 1
7	SDIR 1		I2C GND
8	ADC ON	ADC ON GND	EP~
9			EPGND
10	RX +9V	RX +9V	RX +9V
11	DGND	DGND	DGND
12			
13			
14	XP 19V	XP 19V	XP 19V
15	PWGND	PWGND	PWGND
16	XM 19V	XM 19V	XM 19V

Table 1.3. AQS-SADC Connector

J 6	A	B	C
1			
2			
3			
4		SEL_AQX_AQS	ADC_SEL_AQS
5			DWLCLK_AQS
6	SDA 1		SCL 1
7	SDIR 1		I2C GND
8	ADC ON	ADC ON GND	EP~
9			EPGND
10	RX +9V	RX +9V	RX +9V
11	DGND	DGND	DGND
12			
13			RGP_ADC_AQS
14	XP 19V	XP 19V	XP 19V
15	PWGND	PWGND	PWGND
16	XM 19V	XM 19V	XM 19V

AQS SADC

SEL_AQX_AQS = 0 => AQS Mode

SEL_AQX_AQS = 1 => AQR Mode

Power supply *1.4*

The power supply is derived from +/- 19V for the analog section and from +/- 9V for the digital section. Analog and digital voltages are generated on board. The analog voltages are +/- 15V and +/- 5V. The digital voltage is +5V. The digital power supply is divided in two parts, the reason for that is the galvanic insulation tage between the DAU and the ADC.

ln fact the board has six different voltages and four are shown at the front of the ADC. The +/- 5V which are not shown, are derived from +/- 15V (both analog voltages).

Troubleshooting 2

General 2.1

Before starting to check the system, it should be mentioned, that the board has been thoroughly checked for malfunction or wrong assembly at the factory. For this reason it is prohibited to change or remove components. The board should be sent back to the factory for all modifications. The ADC board should only be opened by service personnel.

No LED is lighting 2.2

If no light-emitting diode (LED) is lighting, check if power is present at the AQR/ AQS and if the DAU connector is connected.

Check all voltages at their respective testpoint:

1. +/-15V analog to AGND1
2. +/-5V analog to AGND1
3. +5V (VCC) digital to DGND
4. +5V (VPWR_P) digital to VPWRGND (supplied from the DAU, derived from +12V).

No signal / No conversion 2.3

Check if the cables of CH A and CH B are connected to the receiver.

Start a reset procedure via the acquisition software (i.e. ‘ii’ = initialize interface) or switch power off and on again, in order to start a new power up sequence.

Check for correct jumper settings AQR type:

ECL01/02: JU1,JU4,JU7-JU12

ECL03/04: JU1,JU4,JU10-JU12

Jumper settings AQS type:

ECL00: JU1,JU4,JU10-JU12

Technical Data 3

Table 3.1. DC specification

Parameter Conditions	min.	typ	max	Units
Supply current (+19V)		170		mA
Supply current (-19V)		170		mA
Supply current (+9V)		215		mA
Supply current (+12V)		480		mA

Table 3.2. System specification

Parameter Conditions	min.	typ	max	Units
Resolution		16		Bits
No Missing Codes		16		Bits
Integral Nonlinearity		+/-0.003	+/- 0.006	% FSR
Noise		120		µV rms
Spectral Noise (Size 8k / sampling rate 150 kSPS)		-120		dB
Signal to (Noise + Distortion) Ratio (10Vpp / 1 kHz)	84	86		dB
Total Harmonic Distortion (10Vpp / 1 kHz)		-94	-88	dB
Peak Harmonic or Spurious Noise (10Vpp / 1 kHz)		-94	-88	dB
Conversion Time per channel			5,3	µs
Acquisition Time per channel			2,5	µs
Throughput Rate for each channel (overlap between conversion and acquisition)			150	kSPS
Analog Input Voltage Range			+/- 5	V
Crosstalk CH A : 10 Vpp @ f < 50kHz CH B input shorted		100		dB

Assembly map SADC *3.1*

Figure 3.1. Assembly map AQR SADC ECL01/02

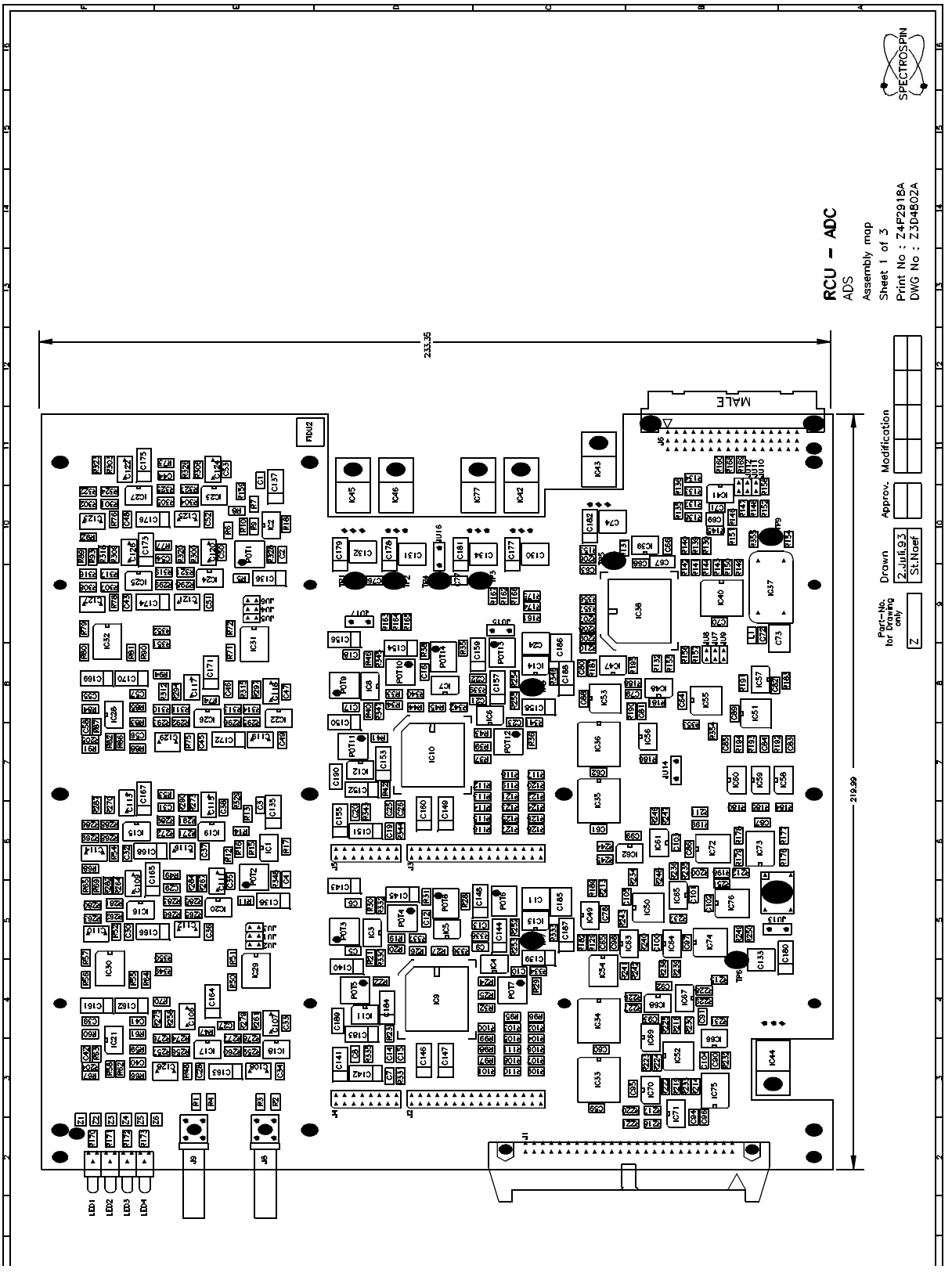
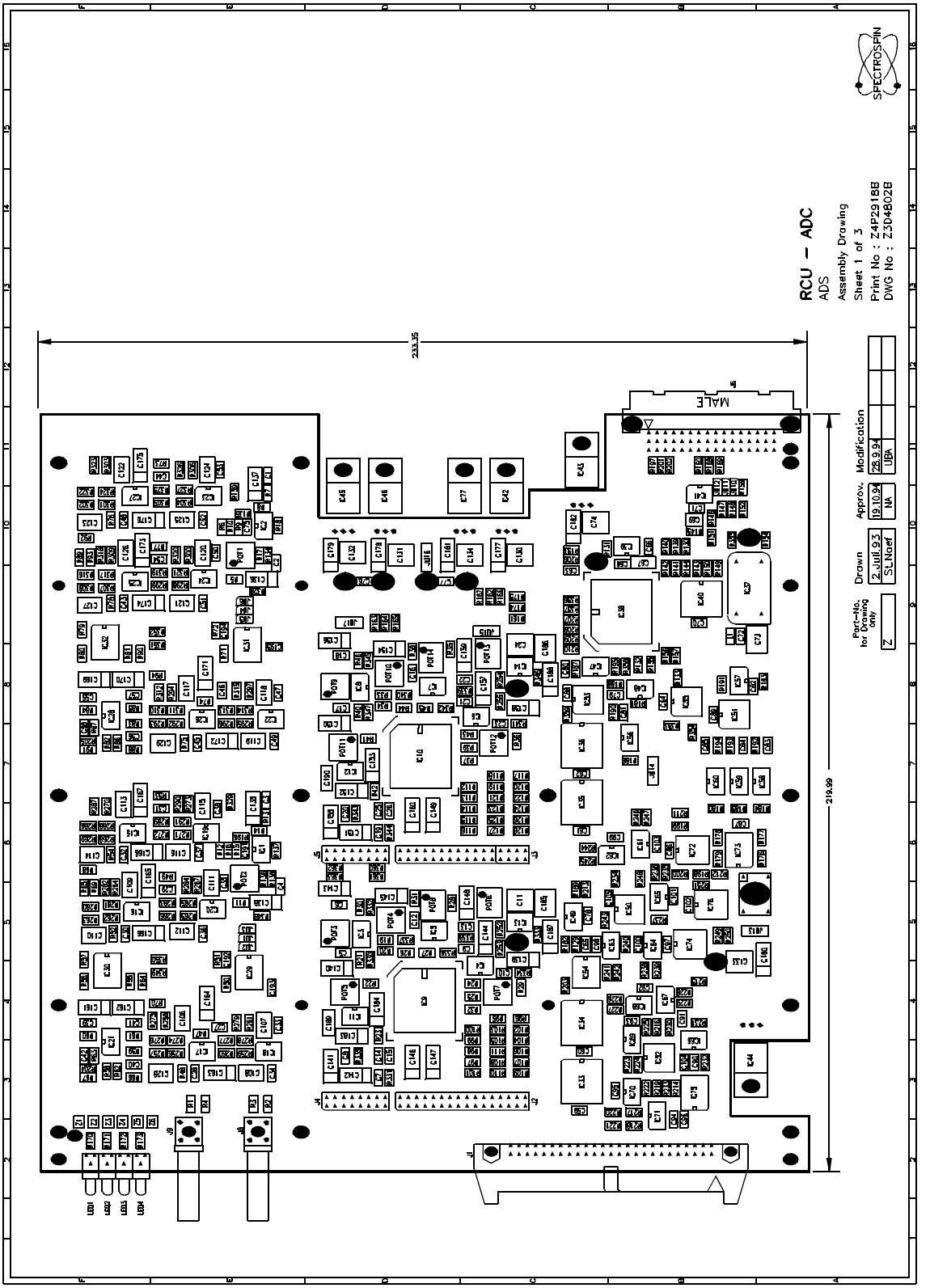
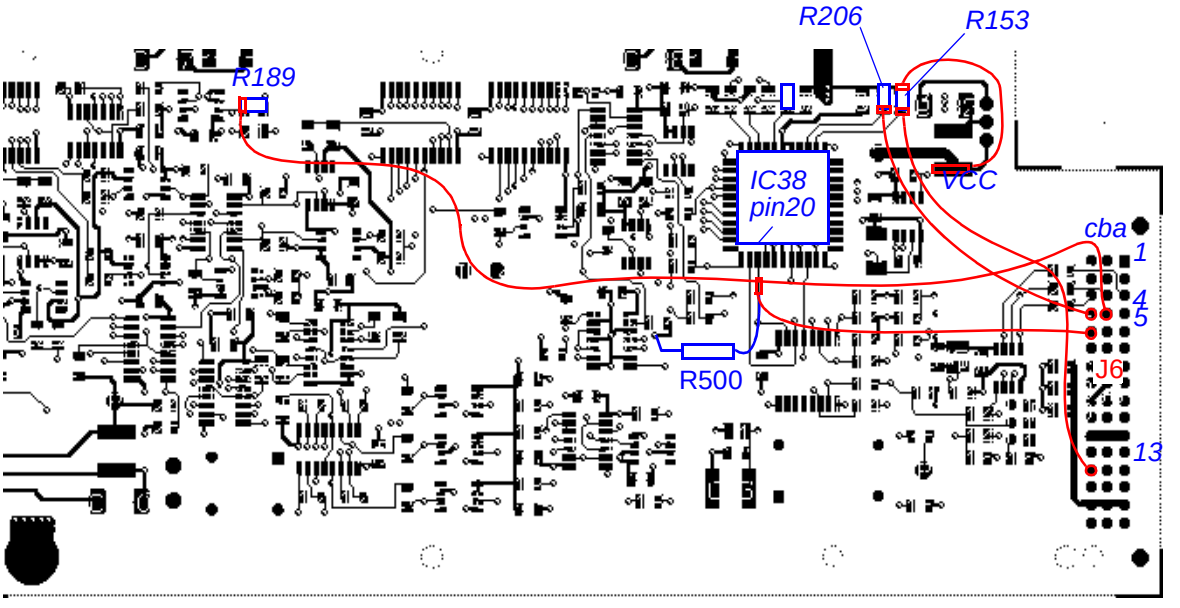


Figure 3.2. Assembly map AQR SADC ECL03/04



Attention: The assembly map may not be consistent with the implementation, because of second source component evaluation and varied use of the board (see AQR HADC).

Figure 3.3. Assembly map AQS SADC ECL01



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