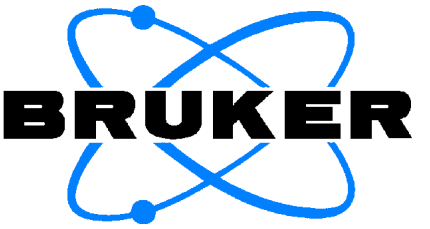

AQX / AQS

RCU Technical Manual

Version 005

BRUKER

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Contents

Contents

General Infos 1

Abbreviation 1.1

- AQBUS --> **Ac**q**u**isition **Bus**
- AQS --> **Ac**q**u**isition **S**tart ; **Ac**q**u**isition **S**ystem
- AQX --> **Ac**q**u**isition **U**nit
- AQR --> **Ac**q**u**isition **R**ack
- ASU --> **A**mplitude **S**etting **U**nit
- BB--> **B**road **B**and
- CCU --> **C**ommunication **C**ontrol **U**nit
- DDS --> **D**irect **D**igital **S**ynthesizer
- DSP --> **D**igital **S**ignal **P**rozessor
- DRAM --> **D**ynamic **R**andom **A**ccess **M**emory
- EP --> **E**mpfänger **P**ulse
- EPHD --> **E**mpfänger **P**uls **H**omo **D**ecoupling
- EPROM --> **E**rasable **P**rogrammable **R**ead **O**nly **M**emory
- FADC --> **F**ast **ADC**
- FCU --> **F**requency **C**ontrol **U**nit
- FID--> **F**ree **I**nduction **D**ecay
- FIFO --> **F**irst **I**n **F**irst **O**ut
- FTLP/4M --> **F**ilter **L**ow **P**ass / **4M**Hz
- GCU --> **G**radient **C**ontrol **U**nit
- HADC/2-->**H**igh resolution **ADC** / 2 (AQR / AQS)
- HR--> **H**igh **R**esolution
- MCI--> **M**ulti **C**hannel **I**nterface
- PAL--> **P**rogrammable **A**rray **L**ogic
- PTS--> **P**rogram **T**est **S**ource
- RCP--> **R**ealtime **C**lock **P**uls
- RCU --> **R**eceive **C**ontrol **U**nit
- SADC --> **S**tandard **ADC**
- SCI --> **S**erial **C**ommunication **I**nterface
- SPHD --> **S**ende **P**ulse **H**omo **D**ecoupling

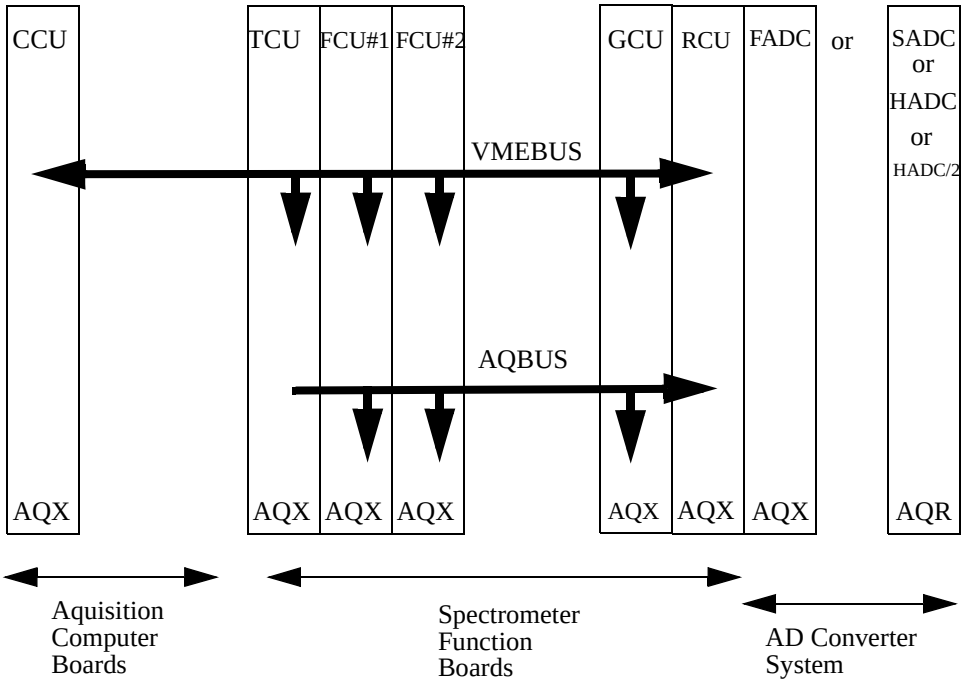
- SRAM --> **S**tatic **R**andom **A**ccess **M**emory
- TCU--> **T**iming **C**ontrol **U**nit
- XDWCLK --> E**x**tern **DWCLK**
- XEP --> E**x**tern **EP**

Introduction AQX 2

General AQX Version 2.1

The Receiver Control Unit (RCU) is a member of the aquisition computer AQX. The AQX includes a complete aquisition computer system (i.e. CPU/4 or CCU and the spectrometer specific function boards TCU (Timing Control Unit), FCU (Frequency Control Unit) and the mentioned RCU. The CCU includes also the fast memory and the SIO unit.

Figure 2.1. Aquisition system

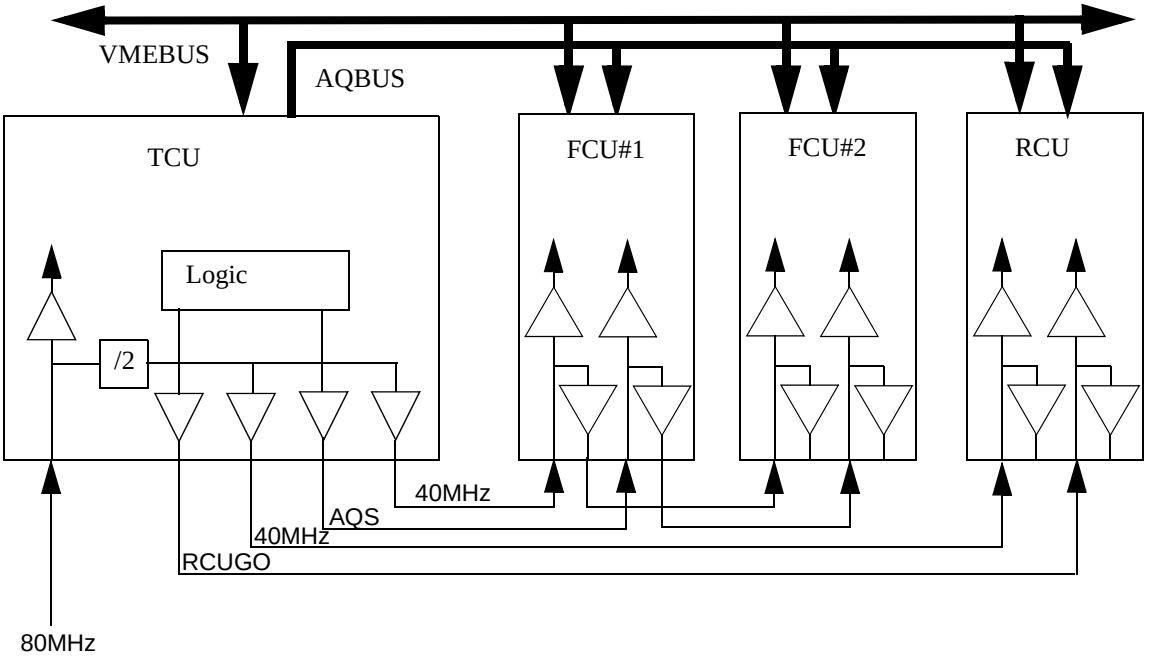


An aditional AQBUS for the spectrometer function boards is used parallel to the VMEBUS. The RCU is the logical master for the AD converter system. It is the receiver of the data from the ADC System.

System overview AQX Version *2.2*

The aquisition computer is based on a VME system that uses a 32Bit Processor. So do all spectrometer function boards. Most spectrometer function boards have memory and local processors on board.

Figure 2.2. Spectrometer synchronisation



TCU:

The TCU generates most RCP's (realtime clock pulses) for the spectrometer. The main clock for the TCU is 80MHz and is normally feed by a PTS. Based on this clock, the FCU's and the RCU realtime system run synchronous with 40MHz. So the time relation between the transmitter system (TCU, FCU) and the receiver system (RCU) is maintained. In special there are two strobe signals (AQS and RCUGO), triggering the spectrometer boards.

1. **80MHz:** This input signal comes directly from the PTS620 and is the clocking frequency for the TCU. The voltage level is 0dBm (0,65Vpp at 50Ω).This signal is used to generate the 40MHz signal.
2. **40MHz:** The output signal are TTL (3Vpp at 50Ω) and operate on a 50% duty cycle. One is used to clock the FCU's the other to clock the RCU.
3. **RCUGO:** This pulse is used to start the RCU at every scan. It goes high for 50ns.
4. **AQBUS:** Various instructions are sent from TCU to the FCU's (and GCU if fitted) via the Acquisition Bus. This TTL strobe pulse is used to synchronise the timing of the bus. The strobe pulse goes low for a minimum of 25ns.

FCU:

1. It generates the DDS input for the PTS (frequency and phase).
2. It controls the frequency setting of the PTS output.
3. It generates MOD, MULT, AT20 and AT40 signals used for power regulation in the ASU boards.
4. It controls the phase of the 4 Phase Modulator using ph1 and ph2 signals. In many respects the FCU takes the place of the MCI board.

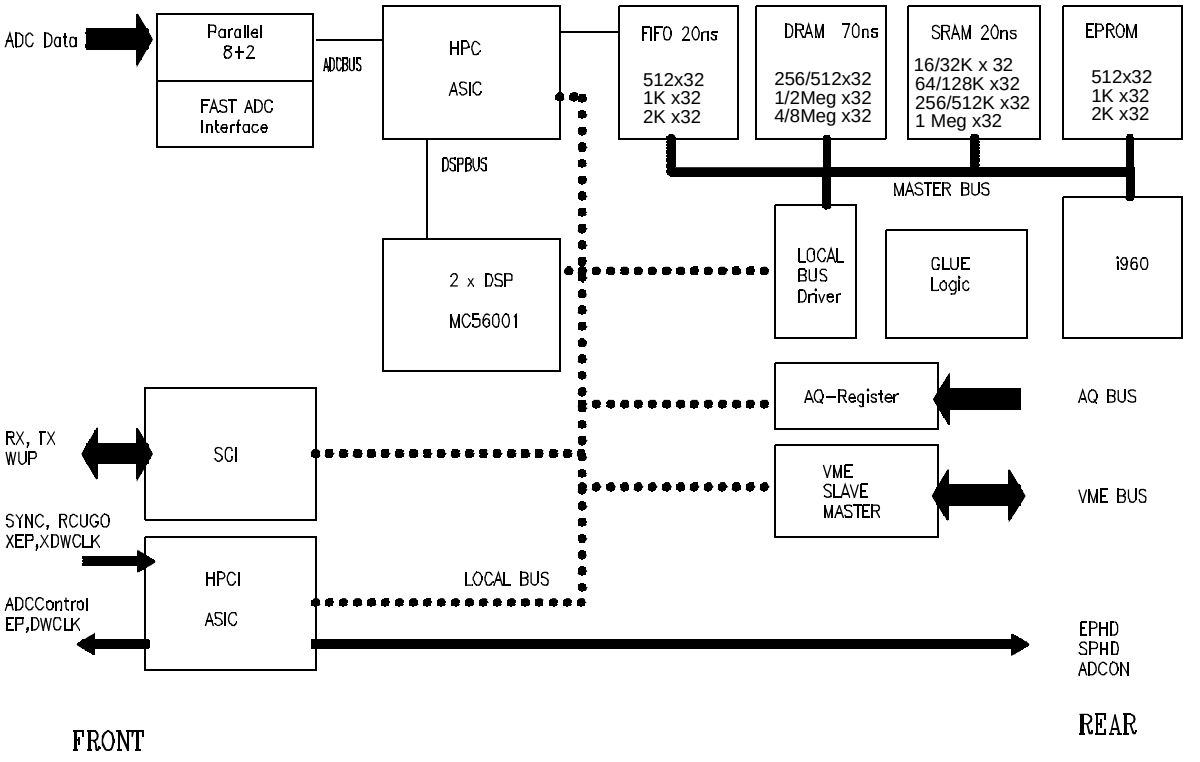
RCU:

1. The RCU takes complete control of the acquisition. During the current scan it will operate autonomously until the end of the scan. To perform a second scan however the RCU must wait for a second RCUGO signal from the TCU. The RCUGO signal is synchronised with the 40MHz clock, both are received from the TCU.
2. As part of the acquisition control the RCU generates the DWELL CLOCK (DWCLK) as well as the EP and the ADCON signals.
3. It is possible to deactivate the internal DWCLK and EP and connect an external DWCLK (XDWCLK) and an EP (XEP) to the RCU.
4. The RCU is responsible for processing the acquired data (e.b. digital filtering) as well as accumulation and DMA transfer of processed data to the CCU.
5. The RCU is master of all digitizers (SADC, HADC, HADC/2, FADC and HRD16) and all digitizers functions. Also the filter settings (SADC, HADC, HADC/2, FLTP/4M and HRD16) and Quad Mode (qsim, qf) are controlled by the RCU. For the SADC, HADC, HADC/2 and HRD16 the information is sent directly over the 50 way digitizer cable. For the FLTP/4M the information is sent through the SADC, HADC or HADC/2 to the FLTP/4M via the I2C Bus of the AQR backplane.
6. For homodecoupling the timing of the decoupling pulses is set by the RCU. The RCU generates two signals SPHD and EPHD.

AQX RCU overview 2.3

The RCU is a VMEBUS Board. All main functions are placed on the motherboard. In general the RCU is a VME Slave but it can also do some VME master DMA functions (transfer of FIDs to the acquisition computer).

Figure 2.3. RCU Blockdiagram



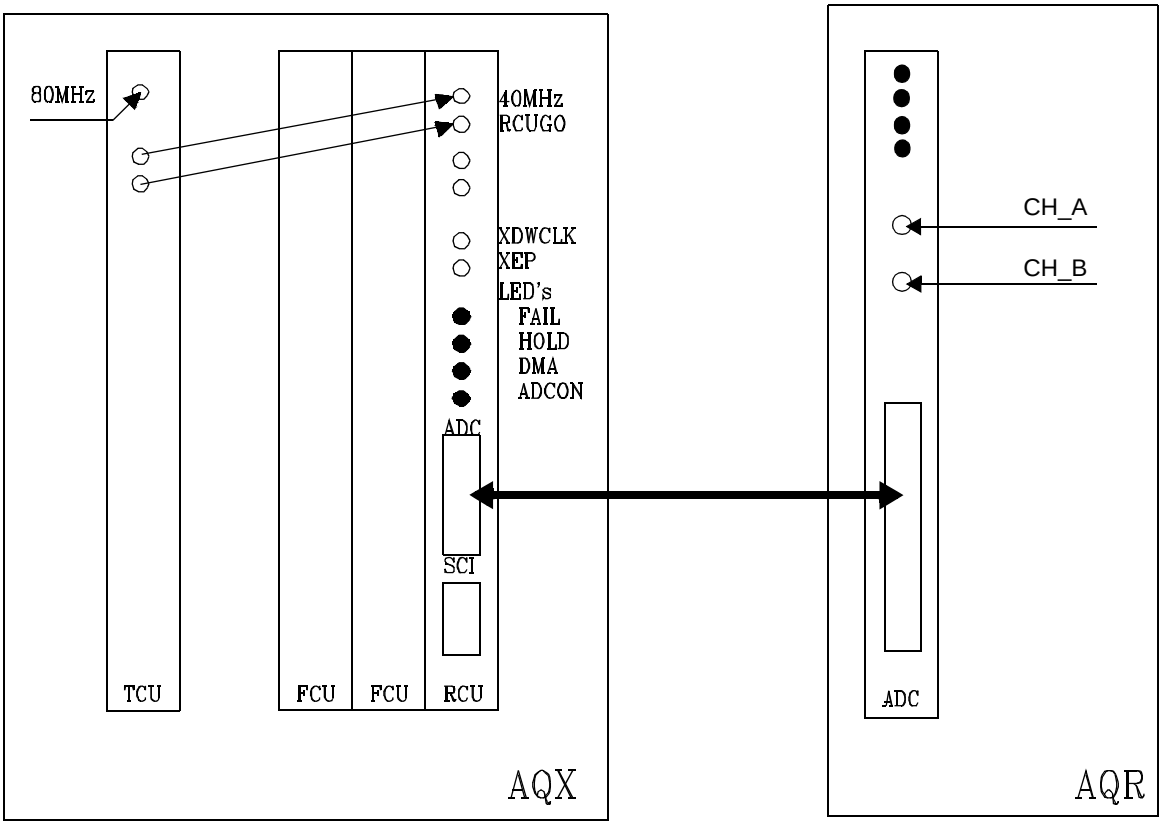
The board consists of a i960 RISC CPU processor system with a boot eprom, a fast SRAM (0 Wait States, Pipelined) a larger DRAM (aquisition data memory) and a FIFO (data synchronisation). The so called masterbus section is exremly fast. The lower speed section (localbus) gives access to the VMEBUS, digital signal processors, DWELL clock generator (HPCI) and the debugging port (SCI). The interface to the ADC is done by a RS422 interface for low sampling (1MHz) AD converter system or an adequate fast ADC interface. The HPC checks the connection to the AD converter system and prepares the incomming data. A special communication register (AQ-Register) is placed on this board to get realtime instructions from the TCU (dummy scan, channel A & B function, ..).

The software for the RCU is downloaded by the aquisition computer system, and may be placed in SRAM or/and DRAM. The DSP software is then downloaded by the i960 to the DSP system.

AQX Connection to SADC and HADC 2.4

For high resolution NMR purpose two AD converter systems called HADC and SADC have been designed. They differ only in AD converter specification and max. DWELL clock, but they have the same interface to the RCU (RS422). This interface is galvanically isolated from the analog part on the AD converter system. For immunity reasons, the RS422 twisted pair concept was chosen. So one signal is physically transferred by two wires and galvanically isolated at the HADC or SADC.

Figure 2.4. HR - System

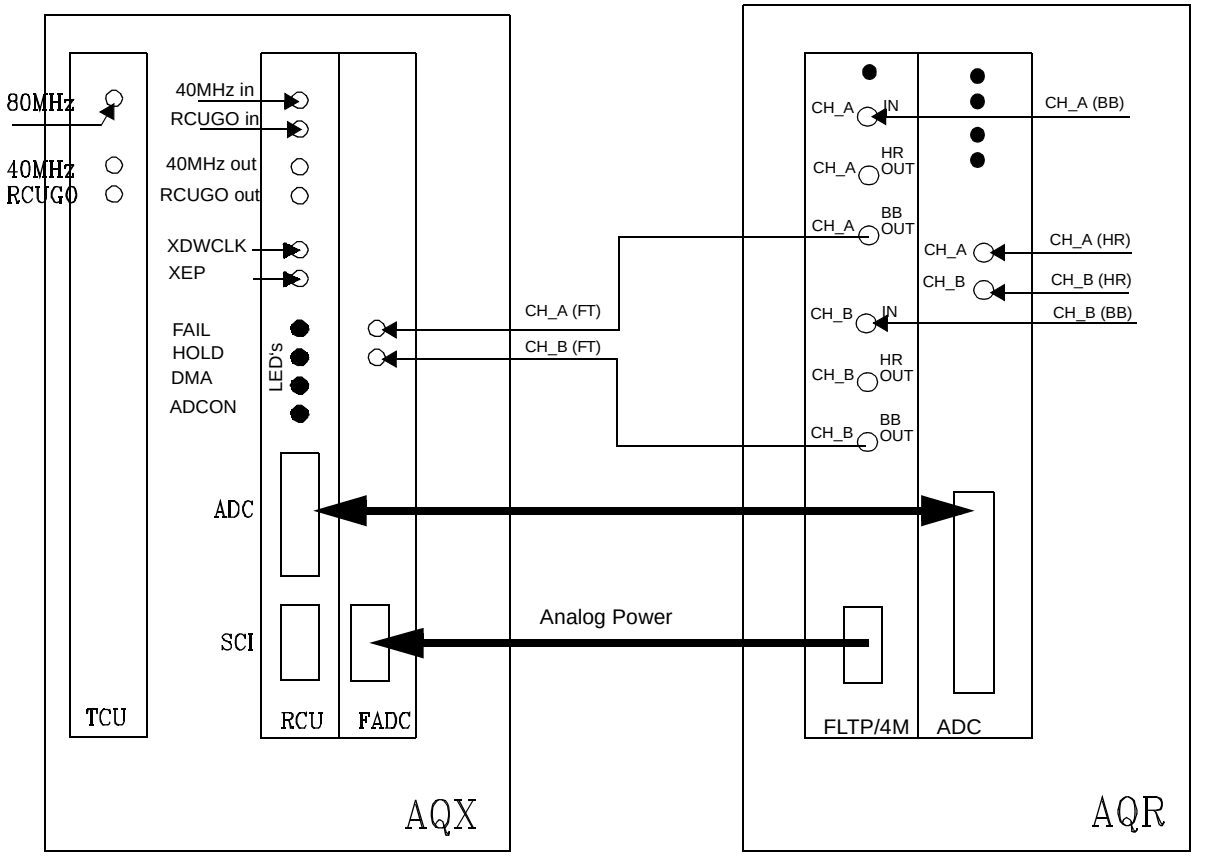


As shown above, the RCU is located in the computer rack called AQX and the AD converter system (with the antialiasing filters) is located in the AQR rack. The only required connection is a 50 wire cable, that can be several meters long. The connection to TCU is made with the 40MHz and the RCUGO signal. For special purpose it is possible to connect an external DWELL CLOCK (XDWCLK) and external EP (XEP = Extern Empfaenger Puls) to the RCU.

AQX Connection to FADC 2.5

For solids purpose an AD converter system called FADC has been designed. It is plugged directly onto the RCU. This interface is galvanically isolated from the analog part of the AD converter system. For technical reasons, the FADC is located in the computer rack AQX and not in the AQR. So the digitized signal is physically transferred by a short wire and galvanically isolated at the FADC.

Figure 2.5. Solid - NMR



As shown above, the FADC is located in the computer rack AQX but the corresponding antialiasing filter is located in the AQR rack. The power for the analog part of the FADC is supplied by the filterboard. A HADC or SADC must be placed to the system because the RCU controls the filterboard (FLTP/4M) via SADC or HADC. The filterboard delivers a analog signal based on the broadband input signals (BB) for the SADC/HADC (HR) high resolution input, if a direct HR signal from the receiver ist not available.

Note: The BB signals of the receiver are connected to the filterboard, and its BB output is connected to the FADC. The HR output of the receiver is always connected to the HADC or SADC directly. The HR output of the filterboard is optional and for testing purpose.

The SCI connector is an RS485 interface which can be used for debugging purposes. It is normally not used.

Introduction AQS 3

General AQS Version 3.1

The Receiver Control Unit (RCU) is a member of the aquisition computer AQS. The AQS includes a complete aquisition computer system (i.e. CCU and the spectrometer specific function boards TCU3 (Timing Control Unit), FCU3 (Frequency Control Unit) and the mentioned RCU. The CCU includes also the fast memory and the SIO unit.

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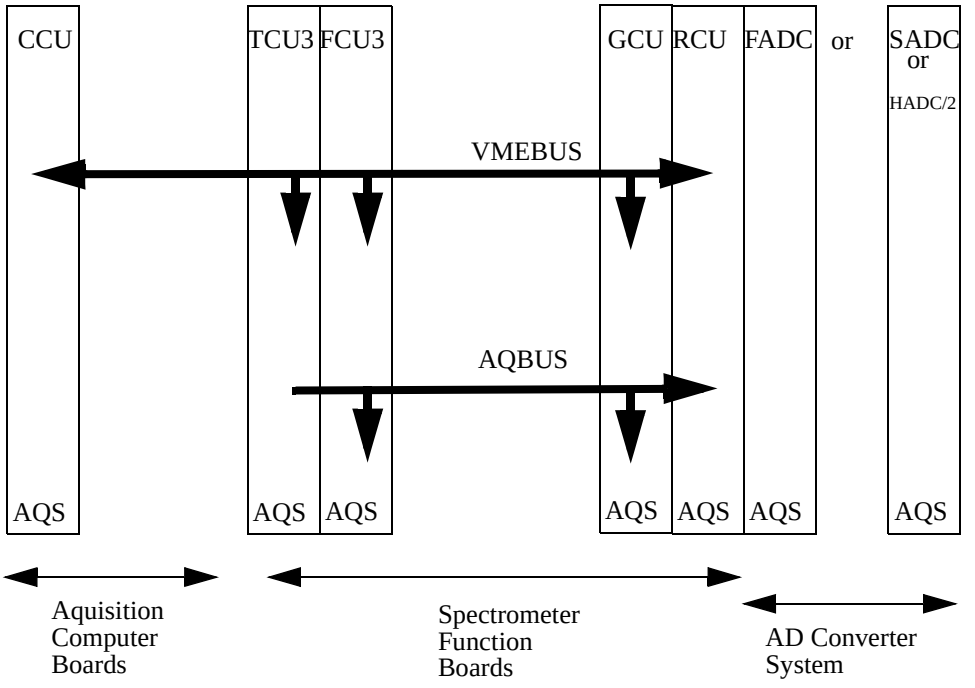

An aditional AQBUS for the spectrometer function boards is used parallel to the VMEBUS. The RCU is the logical master for the AD converter system. It is the receiver of the data from the ADC System.

System overview AQS Version *3.2*

The aquisition computer is based on a VME system that uses a 32Bit Processor. So do all spectrometer function boards. Most spectrometer function boards have memory and local processors on board.

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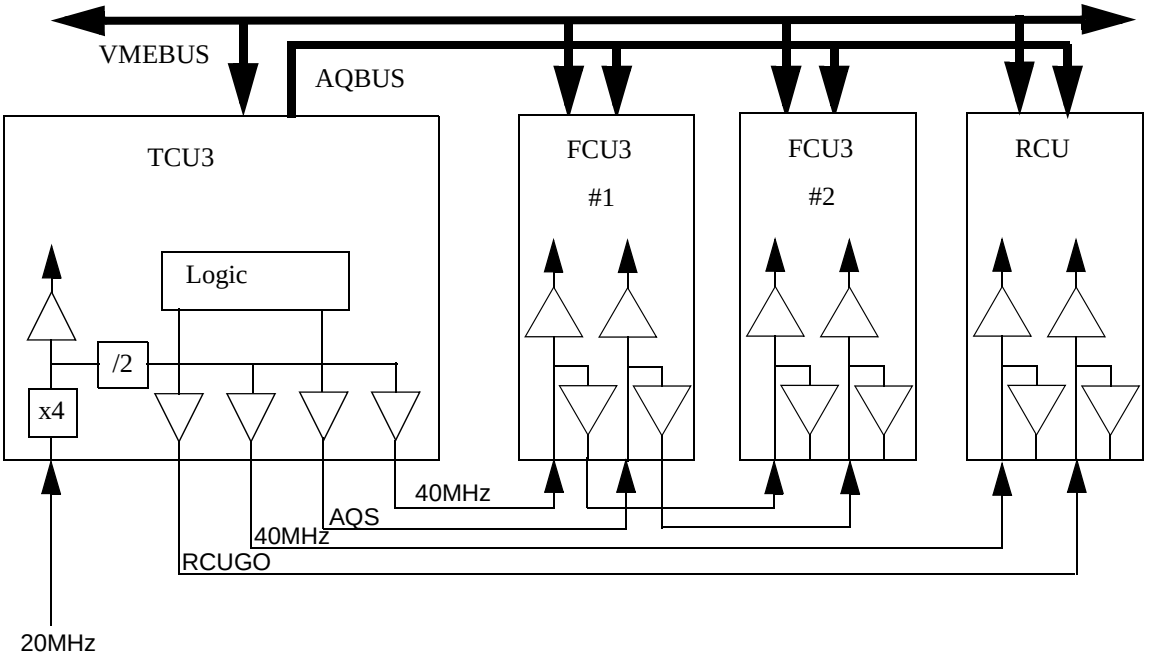

TCU:

1. The TCU3 generates most RCP's (internal clock pulses) for the spectrometer. The main clock for the TCU3 is 80MHz derived from a 20MHz signal normally fed by a AQS REF RX22. Based on this clock, the FCU3's and the RCU real-time system run synchronous with 40MHz. So the time relation between the transmitter system (TCU3, FCU3) and the receiver system (RCU) is maintained. In special there are two strobe signals (AQS and RCUGO), triggering the spectrometer boards.
2. **20MHz:** This input signal comes directly from the AQS REF RX22 and is the clocking frequency for the TCU3. The voltage level is 0dBm (0,65Vpp at 50Ω).This signal is used to generate the 40MHz signal.
3. **40MHz:** These output signals are TTL (3Vpp at 50Ω) and operate on a 50% duty cycle. One is used to clock the FCU3's the other to clock the RCU.
4. **RCUGO:** This pulse is used to start the RCU at every scan. It goes high for 50ns.
5. **AQBUS:** Various instructions are sent from TCU3 to the FCU3's (and GCU if fitted) via the Acquisition Bus. This TTL strobe pulse is used to synchronise the timing of the bus. The strobe pulse goes low for a minimum of 25ns.

RCU:

1. The RCU takes complete control of the data acquisition. During the current scan it will operate autonomously until the end of the scan. To perform a second scan however the RCU must wait for a second RCUGO signal from the TCU3. The RCUGO signal is synchronised with the 40MHz clock, both are received from the TCU3.

2. The RCU is responsible for processing the acquired data (e.g. digital filtering) as well as accumulation and DMA transfer of processed data to the CCU.

3. The RCU is master of all digitizers (SADC, HADC/2 and FADC) and all digitizers functions. Also the filter settings (SADC, HADC/2 and FLTP/4M) and Quad Mode (qsim, qf and dqd) are controlled by the RCU. For the SADC and HADC/2 the information is sent directly over the 50 way digitizer cable. For the FLTP/4M the information is sent through the SADC or HADC/2 to the FLTP/4M via the I2C Bus of the AQS Adapter (Z003348).

AQS RCU overview 3.3

The RCU is a VMEBUS Board. All main functions are placed on the motherboard. In general the RCU is a VME Slave but it can also do some VME master DMA functions (transfer of FIDs to the acquisition computer).

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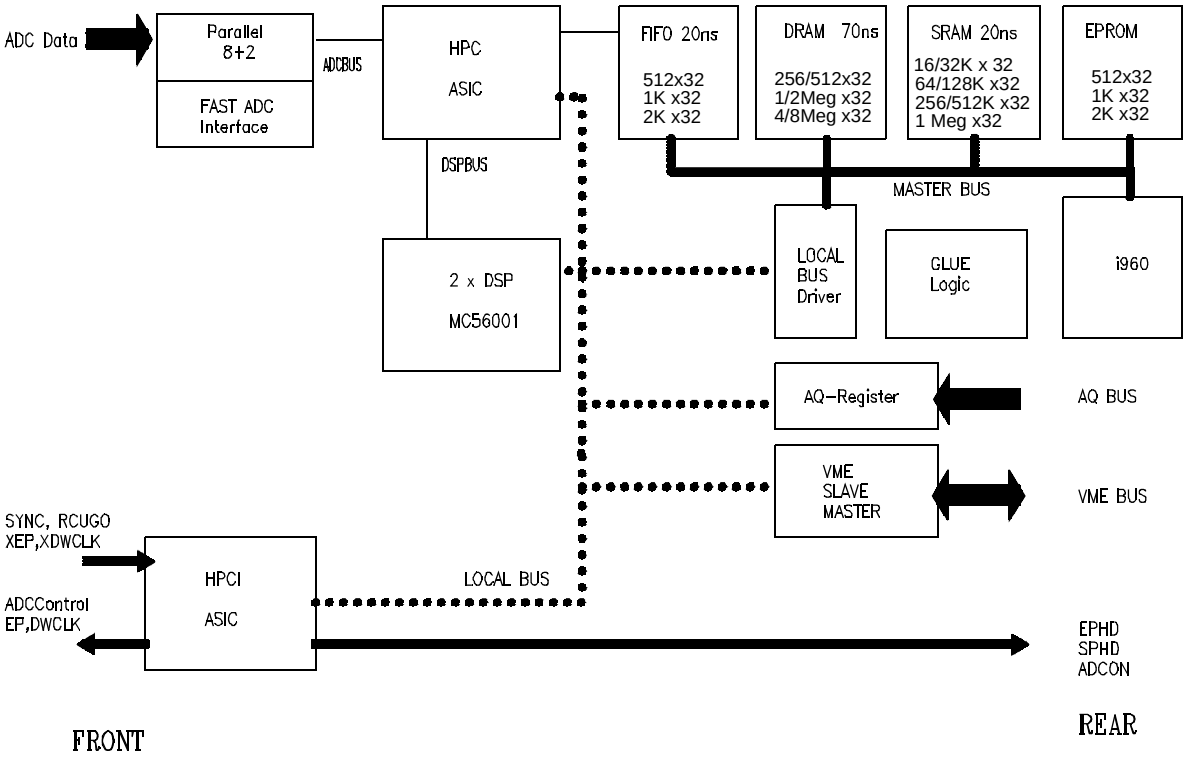

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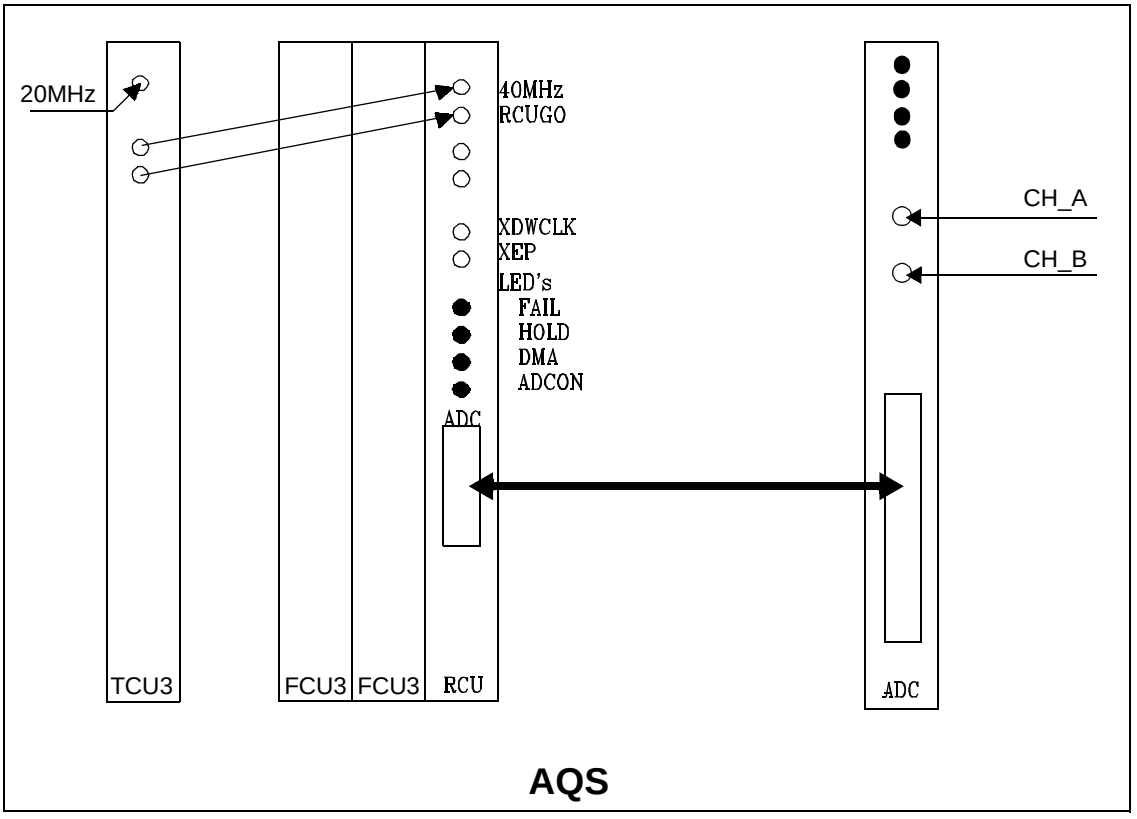
The software for the RCU is downloaded by the aquisition computer system, and may be placed in SRAM or/and DRAM. The DSP software is then downloaded by the i960 to the DSP system.

AQS Connection to SADC and HADC *3.4*

For high resolution NMR purpose two AD converter systems called HADC/2 and SADC have been designed. They differ only in AD converter specification and max. DWELL clock, but they have the same interface to the RCU (RS422). This interface is galvanically isolated from the analog part on the AD converter system. For immunity reasons, the RS422 twisted pair concept was chosen. So one signal is physically transferred by two wires and galvanically isolated at the HADC/2 or SADC.

Figure 3.4. HR - System

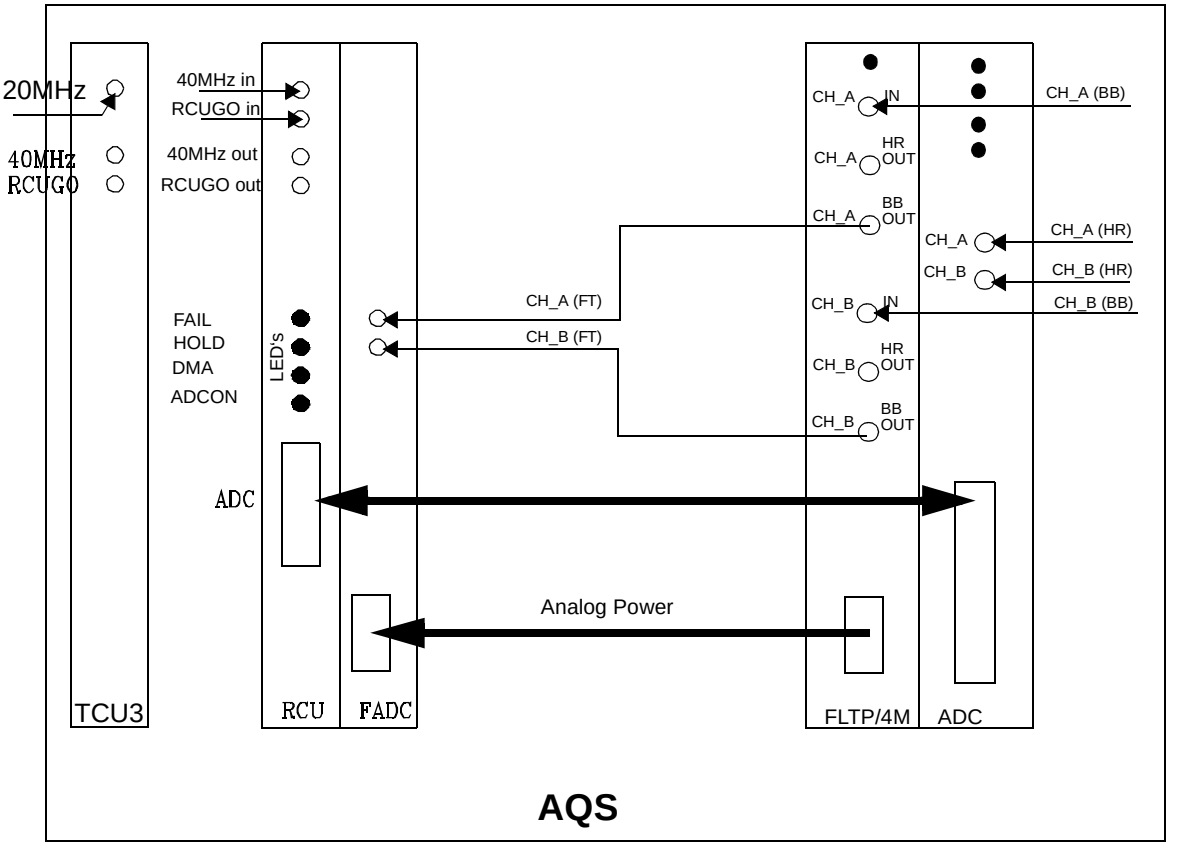


As shown above, the RCU is located in the computer rack called AQS and the AD converter system (with the antialiasing filters) is located in the same AQS rack. The only required connection is a 50 wire cable, that can be several meters long. The connection to TCU3 is made with the 40MHz and the RCUGO signal.

AQS Connection to FADC 3.5

For solids purpose an AD converter system called FADC has been designed. It is plugged directly onto the RCU. This interface is galvanically isolated from the analog part of the AD converter system. So the digitized signal is physically transferred by a short wire and galvanically isolated at the FADC.

Figure 3.5. Solid - NMR



The power for the analog part of the FADC is supplied by the filterboard. A HADC/2 or SADC must be placed to the system because the RCU controls the filterboard (FLTP/4M) via SADC or HADC/2. The filterboard delivers a analog signal based on the broadband input signals (BB) for the SADC / HADC/2 (HR) high resolution input, if a direct HR signal from the receiver ist not available.

Note: The BB signals of the receiver are connected to the filterboard, and its BB output is connected to the FADC. The HR output of the receiver is always connected to the HADC/2 or SADC directly. The HR output of the filterboard is optional and for testing purpose.

Installation 4

General 4.1

The RCU is delivered with its factory settings. Under normal condition there is no need to modify anything. In case of troubles, the following information may be checked. There is also a testprogram (UNIX, aquisition computer) see also Chapter ***4.9***.

This installation guide is adequate for P/N Z002488 ECL01..ECL06 and for Z003678 ECL00..01

(see separate Engineering Changes for details)

Technical data 4.2

The RCU motherboard may be configured. The standard version is highlighted.

Aquisition Memory (DRAM) :1MByte/2MByte, **4MByte**/8Mbyte,16MByte/32MByte

Fast Memory (SRAM) : **256/**512kByte, 1/2MByte, 4MByte

FIFO Memory: **1kx9Bit**, 2kxBit, 4kxBit, 8kxBit

Sampling Rate: max. 40MHz

Power: 2.5A @ 5V

Mechanical size: VMEBUS Board 6HE, Double extended (280mm), 4TE+

Factory settings 4.3

The board is configured at factory as follows (see Jumper settings):

EPROM: 27C512

Clock Jumper: Inserted

DRAM: 4MByte

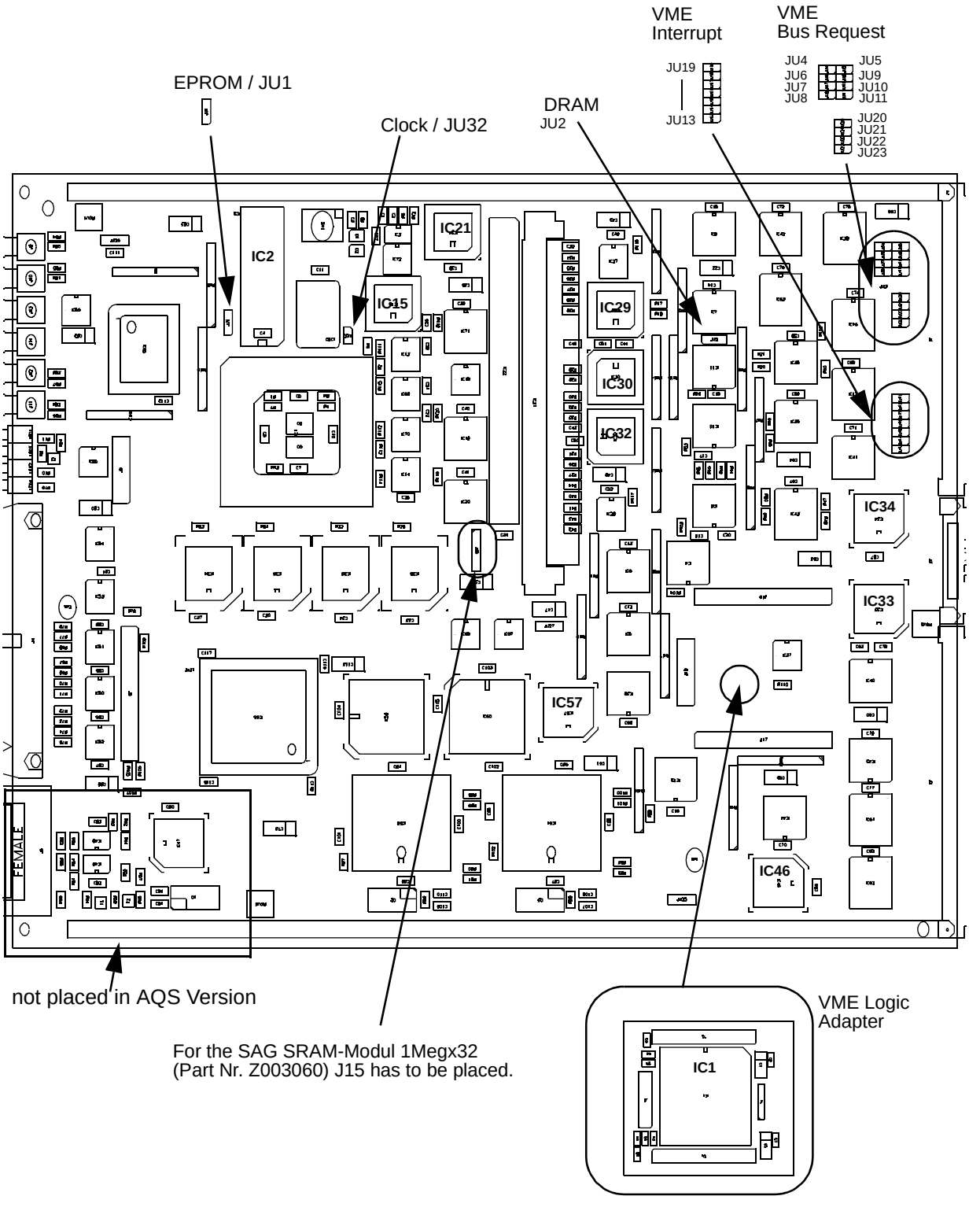
SRAM: 256KByte

VME Interrupt: IRQ 3

VME Bus Request: BR3

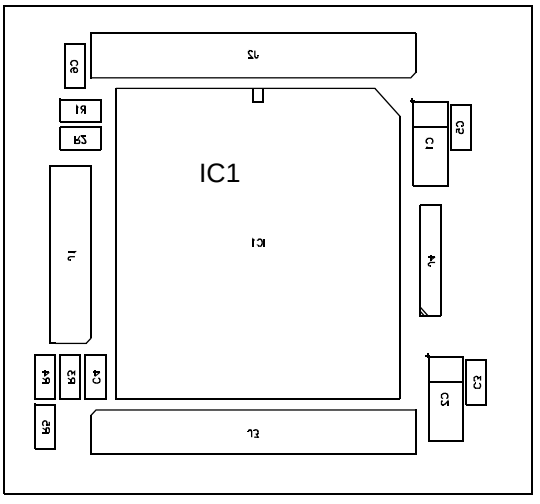
Assembly motherboard Z3P2886A *4.4*

Figure 4.1. motherboard assembly



Assembly VME logic board Z4P2925B 4.5

Figure 4.2. VME logic assembly



This board contains a complex logic device and controls the VME interface. It can be detached from the motherboard for exchange.

Jumpersetting 4.6

EPROM: 4.6.1

The RCU supports in general two types of EPROM. JEDEC32 format (32 pin) and JEDEC format (28 pin). The EPROM must be inserted with upper boarder adjusted (*not pin 1*). At the moment there are two EPROMs defined.

Table 4.1. EPROM configuration

EPROM	SIZE/Type	JU1
RCU0AA01	256k	up 
RCU0BB01	512k	up 
	1M	down 

Clock: *4.6.2*

The Jumper JU32 has to be inserted. 

DRAM: *4.6.1*

The RCU supports four types of DRAM SIMM modules:

Table 4.2. DRAM configuration / Jumper settings

DRAM	SIZE	JU2
256K / 512K x 32	1MByte / 2MByte	right 
1M / 2M x 32	4MByte / 8MByte	left 
4M / 8M x 32	16MByte / 32MByte	not used 

VME Interrupt: *4.6.2*

Changing of interrupt level needs a change in PAL RCU0AA09.

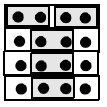
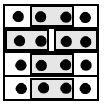
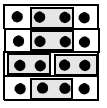
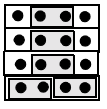
Table 4.3. VME Interrupt configuration / Jumper settings

LEVEL	JUMPER		
IRQ1	JU13 / Out		
IRQ2	JU14 / Out		
IRQ3	JU15 / Out		default
IRQ4	JU16 / Out		
IRQ5	JU17 / In		
IRQ6	JU18 / Out		
IRQ7	JU19 / Out		

VME Bus Request: *4.6.3*

The VME Bus request can be choosen to 4 different levels. They are all implemented the same way, so only one level is explained. The BUS Request BR is granted by the VME Bus master with BGIN. If the board didn't request it, it has to propagate this grant with BGOUT. So there are 3 signals to handle. In the table the '*' means to put one jumper between both jumper positions, the '&' to put each jumper.

Table 4.4. VMEBUS Request configuration / Jumper settings

LEVEL	BR	BG to RCU	BG not to RCU	
0	JU20	JU4 & JU5	JU6*9, JU7*10, JU8*11	
1	JU21	JU6 & JU9	JU4*5, JU7*10, JU8*11	
2	JU22	JU7 & JU10	JU4*5, JU6*9, JU8*11	
3 / default	JU23	JU8 & JU11	JU4*5, JU6*9, JU7*10	

Programmable logic *4.7*

The RCU contains several programmable logic devices.

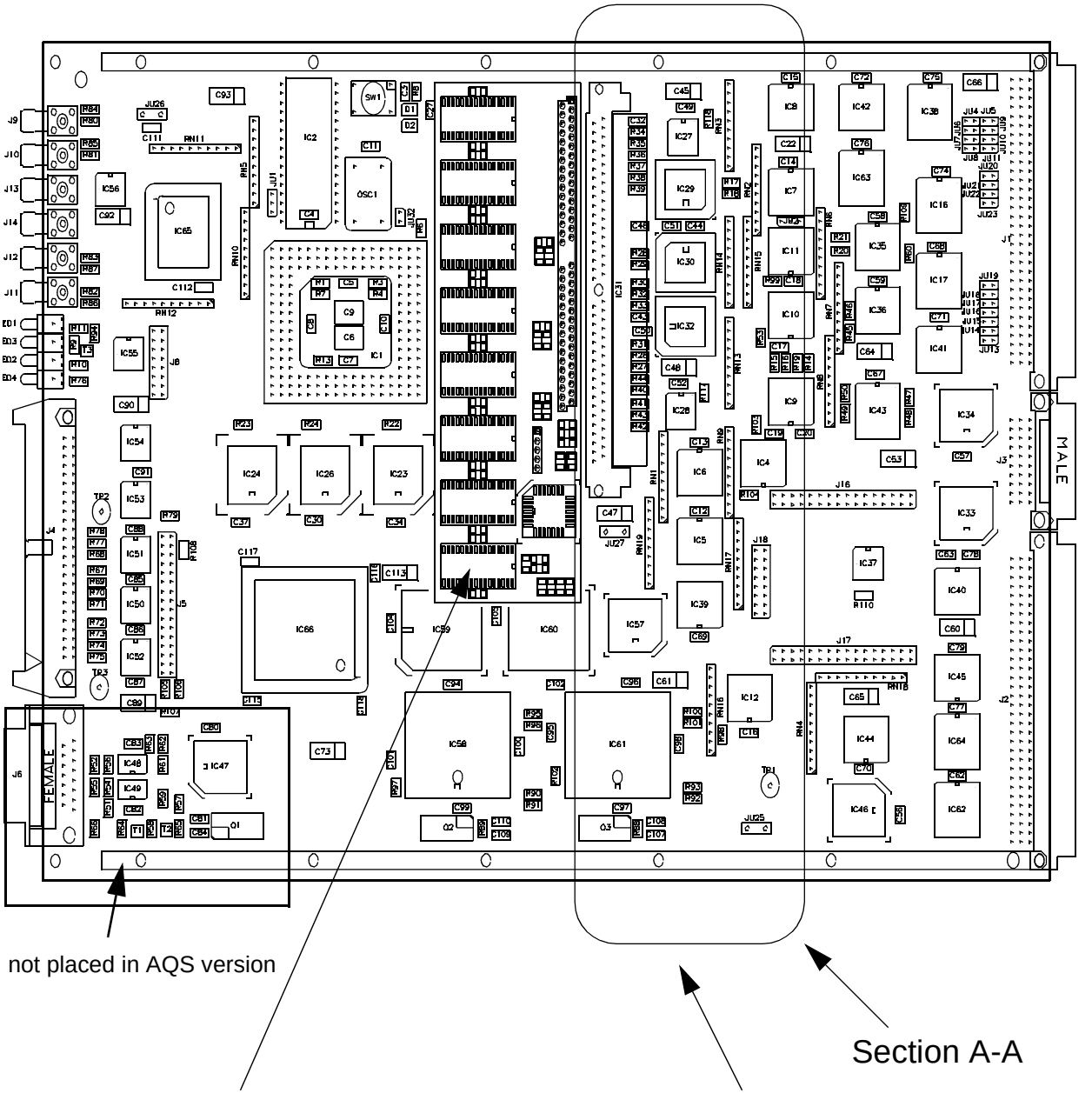
Table 4.5. Programmable logic configuration

Name	Type	IC	Remarks
RCU0xx01	EPROM 512k	IC2	BOOT ROM CPU /4
RCU0xx02	85C220	IC15	Fast- & Reset
RCU0xx03	85C220	IC21	SRAM/FIFO
RCU0xx04	85C220	IC29	DRAM RAS
RCU0xx05	85C220	IC30	DRAM ADR
RCU0xx06	85C220	IC32	DRAM CAS
RCU0xx07	plsi1032	IC1*	VME (VME Logic Adapter)
RCU0xx08	20L8A	IC33	VME Address decode high CPU/4
RCU0xx09	20L8A	IC34	VME Address Low
RCU0xx10	22V10	IC46	AQ-Register control
RCU0xx11	20L8A	IC57	DSP Address decode

Assembly motherboard with extended Memory *4.8*

Extended Memory means: SRAM 1/2Meg x 32Bit / DRAM 4/8Meg x 32Bit

Figure 4.3. Assembly motherboard with extended memory



Modification on the motherboard becauce of 4/8Megx32 DRAM *4.8.1*

Figure 4.4. Modification on the motherboard (4/8Megx32 DRAM)

——— Wire on Layer 1

– — – Wire on Layer 6

What is to do for the modification :

1) Remove the solder-spring JU27.

2) The additional IC 74F157 is placed on IC28. Pin 1 / 8 / 15 / 16 are direct solderd to the same Pins of IC28 (1/8/15/16).

3) Fix the additional resistor (22Ω) with glue onto the RCU board.

4) Connect:

a) Hole1 (MAB22) to the new IC 74F157/pin11.

b) Hole2 (MAB23) to the new IC 74F157/pin10.

c) R=22Ω to the new IC 74F157/pin 9.

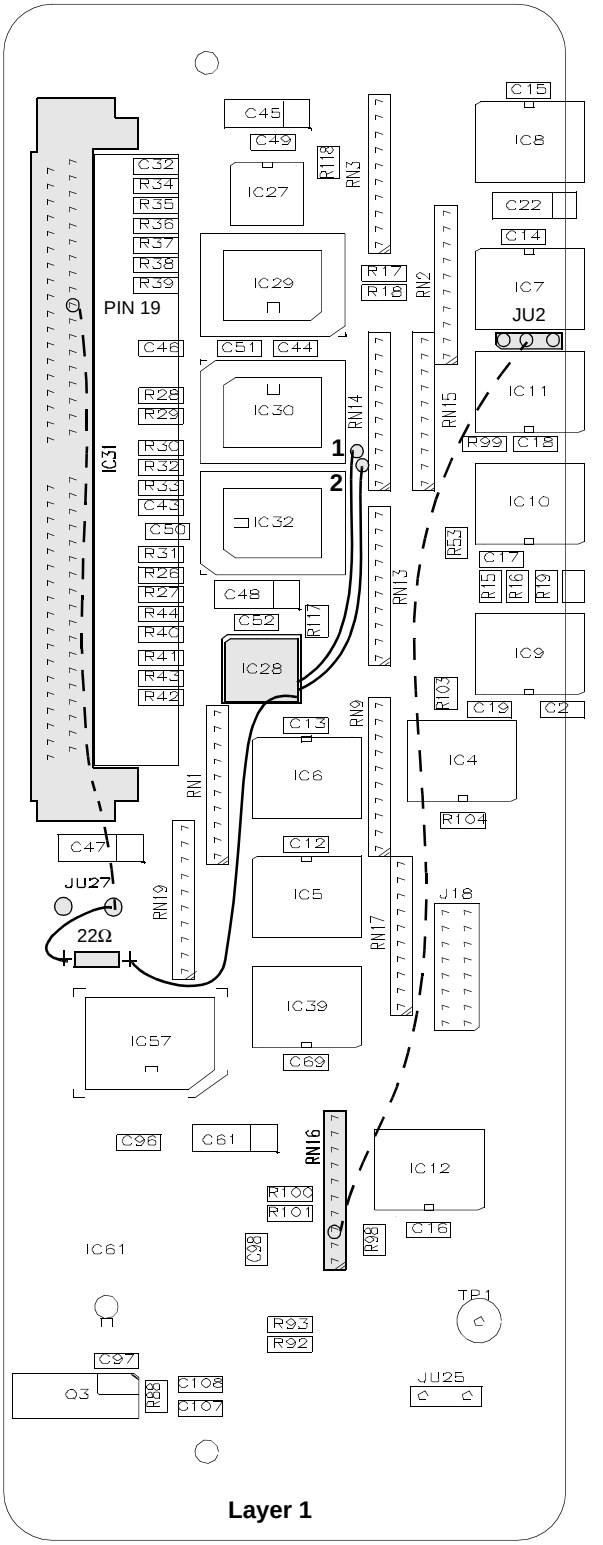
d) Solder a wire on the other side of the new R=22Ω and put the wire through the free hole of the JU27 (to layer6) to the DRAM Modul IC31, pin 19.

e) MAB24 (RN16,Pin3) to JU2 middle Pin.

5) Fix all wire with glue.

6) Put the DRAM Modul (8Megx32) into the SIMM Socket.

Important: Do not insert the jumper JU2.



Testprogram 4.9

For the CPU/4, CCU aquistion computer a testprogram has been developed, which is on the standard BRUKER NMR (DMX, DRX,...series) software package. To use this, the following procedure is to be used:

1. Open a X Window
2. Connect to aquisition computer '*telnet spect*'
3. Login as '*root*'
4. Change to '*/etc/rcu*' (for older UXNMR versions) or to *'/u/systest/rcu'*
5. start testprogram with './rcutest'
6. Use help function '*h*' or autotest 'auto'

! ***Useful commands are:***

„h" = help and prints a list of the commands

„res" = performs a software reset of the RCU

„auto" = starts the automatic self test

Configuration Test 4.10

1. Open a X Window
2. Start UXNMR
3. Type : cf

Answer different questions and finally check the configuration information of the RCU. Technical data about the memory size see chapter***4.2***.

Table 4.6. Memory check list

RCU	memory size {KByte}
DRAM	XXXX
SRAM	XXXX
FIFO	XXXX
ADC	installed or not installed

Figures

Figures

Tables

Tables